

DMMT5401

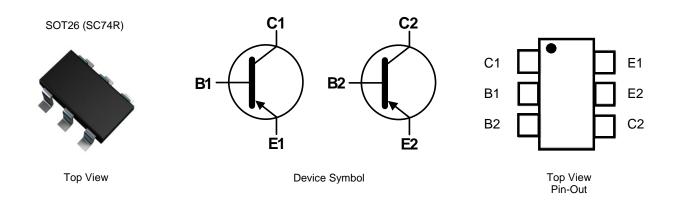
150V DUAL PNP SMALL SIGNAL SURFACE MOUNT TRANSISTOR

Features

- $BV_{CEO} > -150V$
- I_C = -200mA High Collector Current
- Pair of PNP Transistors that are Intrinsically Matched (Note 1)
- 2% Matched Tolerance, hFE, VCE(SAT), VBE(SAT)
- Ideal for Medium Power Amplification and Switching
- Fully Internally Isolated in a Small Surface Mount Package
- **Epitaxial Planar Die Construction**
- Totally Lead-Free & Fully RoHS Compliant (Notes 2 & 3)
- Halogen and Antimony Free. "Green" Device (Note 4)
- Qualified to AEC-Q101 for High Reliability

Mechanical Data

- Case: SOT26 (SC74R)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Plated Leads. Solderable per MIL-STD-202. Method 208 @3
- Weight: 0.018 grams (Approximate)



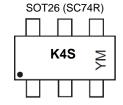
Ordering Information (Note 5)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
DMMT5401-7-F	AEC-Q101	K4S	7	8	3,000

Notes:

- 1. Intrinsically matched pair as this is built with adjacent die from the same wafer.
 2. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 3. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 4. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.
- 5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



K4S = Part Marking (See Ordering Information)

YM = Date Code Marking Y = Year (ex: F = 2018)M = Month (ex: 9 = September)

Date Code Kev

Year	2017		2018	2	2019	202	20	2021		2022	2	023
Code	E		F		G	Н				J		K
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D

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Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-160	V
Collector-Emitter Voltage	V _{CEO}	-150	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	Ic	-200	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Power Dissipation Total Device	(Notes 6 & 7)	P _D	300	mW	
Thermal Resistance, Junction to Ambient	(Note 6)	$R_{ heta JA}$	417	°C/W	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C	

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Collector-Base Breakdown Voltage	BV _{CBO}	-160		_	V	$I_{\rm C} = -100 \mu A, I_{\rm E} = 0$	
Collector-Emitter Breakdown Voltage	BV _{CEO}	-150	_		V	$I_{C} = -1 \text{mA}, I_{B} = 0$	
Emitter-Base Breakdown Voltage	BV _{EBO}	-5			V	$I_E = -10\mu A, I_C = 0$	
Collector-Base Cutoff Current	I _{CBO}	_	_	-50	nΑ μΑ	V _{CB} = -120V, I _E = 0 V _{CB} = -120V, I _E = 0, T _A = +100°C	
Emitter-Base Cutoff Current	I _{EBO}	_		-50	nA	$V_{EB} = -3V, I_B = 0$	
ON CHARACTERISTICS (Note 8)							
DC Current Gain (Note 9)	h _{FE}	50 60 50	_	240	_	$I_{C} = -1mA, V_{CE} = -5V$ $I_{C} = -10mA, V_{CE} = -5V$ $I_{C} = -50mA, V_{CE} = -5V$	
Collector-Emitter Saturation Voltage	V _{CE(SAT)}	_	_	-0.2 -0.5	V	$I_C = -10\text{mA}, I_B = -1\text{mA}$ $I_C = -50\text{mA}, I_B = -5\text{mA}$	
Base-Emitter Saturation Voltage	V _{BE(SAT)}	_	_	-1	V	$I_C = -10\text{mA}, I_B = -1\text{mA}$ $I_C = -50\text{mA}, I_B = -5\text{mA}$	
SMALL SIGNAL CHARACTERISTICS							
Current Gain-Bandwidth Product	f⊤	100	—	300	MHz	$V_{CE} = -10V, I_{C} = -10mA, f = 100MHz$	
Output Capacitance	C _{OBO}		—	6	pF	$V_{CB} = -10V$, $f = 1.0MHz$, $I_E = 0mA$	
Small Signal Current Gain	h _{fe}	40		260	_	$V_{CE} = -10V, I_{C} = -1mA, f = 1.0kHz$	
Noise Figure	NF	_	_	8	dB	V_{CE} = -5V, I_C = -200 μ A, R_S = 10 Ω , f = 1.0kHz	

Notes:

- 6. For a device mounted on minimum recommended pad layout with 1oz copper that is on a single-sided 1.6mm FR-4 PCB; the device is measured under still air conditions whilst operating in a steady-state.
- 7. Maximum combined dissipation.
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. The DC Current Gain, h_{FE}, (matched at I_C = -10mA and V_{CE} = -5V) Collector Emitter Saturation Voltage, V_{CE(SAT)}, and Base Emitter Saturation Voltage, V_{BE(SAT)} are matched with typical matched tolerances of 1% and maximum of 2%.

March 2018



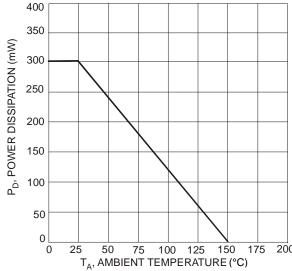


Fig. 1 Power Dissipation vs. Ambient Temperature

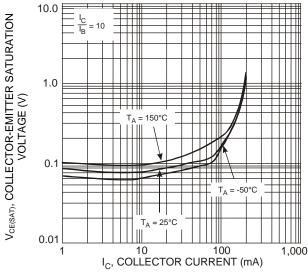


Fig. 3 Typical Collector-Emitter Saturation Voltage vs. Collector Current

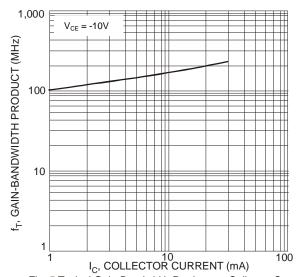


Fig. 5 Typical Gain-Bandwidth Product vs. Collector Current

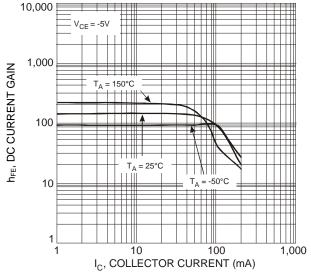
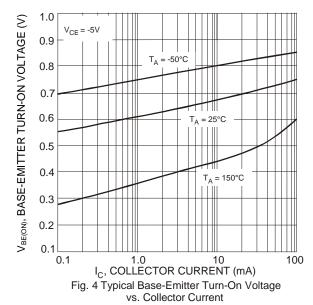


Fig. 2 Typical DC Current Gain vs. Collector Current

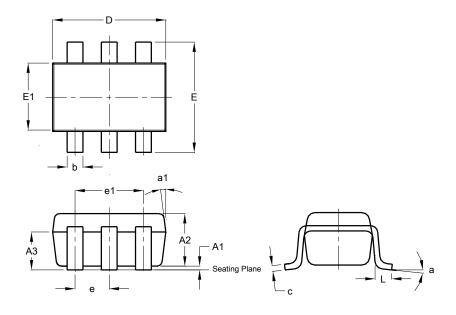




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (SC74R)

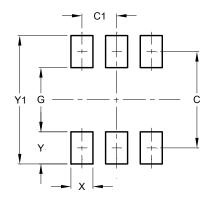


SOT26 (SC74R)							
Dim	Min	Max	Тур				
A1	0.013	0.10	0.05				
A2	1.00	1.30	1.10				
A3	0.70	0.80	0.75				
b	0.35	0.50	0.38				
C	0.10	0.20	0.15				
D	2.90	3.10	3.00				
e	-	-	0.95				
e1	-	-	1.90				
Е	2.70	3.00	2.80				
E1	1.50	1.70	1.60				
L	0.35	0.55	0.40				
а	-	-	8°				
a1	-	-	7°				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (SC74R)



Dimensions	Value (in mm)
С	2.40
C1	0.95
G	1.60
Х	0.55
Y	0.80
Y1	3.20



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