

**450V DUAL N-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D$ $T_A = +25^{\circ}C$
450V	4Ω @ $V_{GS} = 10V$	0.85A

**Description**

This new generation complementary MOSFET features low on-resistance and fast switching, making it ideal for high efficiency power management applications.

**Applications**

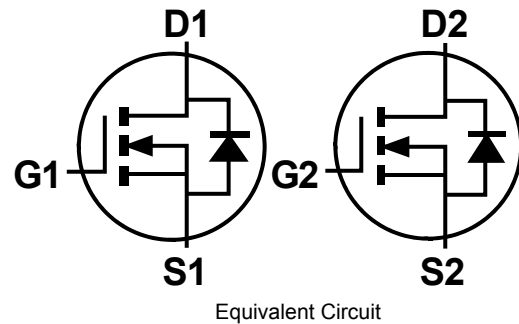
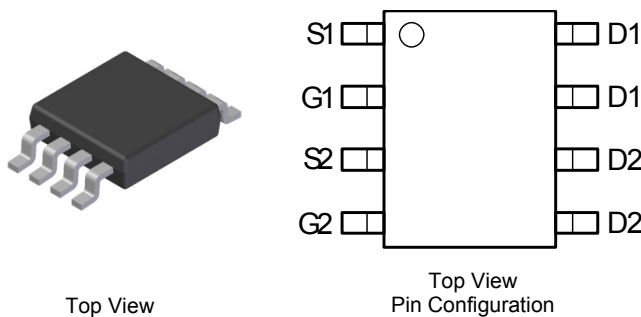
- Motor Control
- Backlighting
- DC-DC Converters
- Power Management Functions

**Features**

- Low Input Capacitance
- High BVDSS Rating for Power Application
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 ③
- Weight: 0.074 grams (approximate)

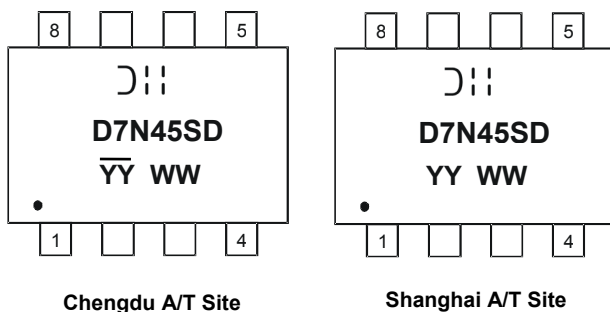


**Ordering Information** (Note 4)

Part Number	Compliance	Case	Packaging
DMGD7N45SSD-13	Standard	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



- ⌋⌋ = Manufacturer's Marking
- D7N45SD = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Year (ex: 14 = 2014)
- WW = Week (01 - 53)
- YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
- YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	450	V
Gate-Source Voltage	V <sub>GSS</sub>	±30	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	I <sub>D</sub>	Steady State	0.5
		t < 10s	0.62
		t < 1s	0.85
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	2.2	A
Maximum Body Diode Forward Current (Note 5)	I <sub>S</sub>	1.7	A
Avalanche Current (Note 6)	I <sub>AS</sub>	L = 60mH	1.4
		L = 10mH (Note 8)	2.2
Avalanche Energy (Note 6)	E <sub>AS</sub>	L = 60mH	56
		L = 10mH (Note 8)	25

**Thermal Characteristics**

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	1.64	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	Steady state	78
		t < 10s	20.2
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	13.3	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	450	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 10mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 450V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	3.5	—	4.5	V	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1mA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	3	4	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.4A
Forward Transfer Admittance	Y <sub>fs</sub>	0.55	1.1	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 0.4A
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 0.7A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	256	—	pF	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	22.5	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	0.83	—		
Gate Resistance	R <sub>G</sub>	—	2.3	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	6.9	—	nC	V <sub>DS</sub> = 360V, I <sub>D</sub> = 0.7A, V <sub>GS</sub> = 10V
Gate-Source Charge	Q <sub>gs</sub>	—	1.4	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	3.4	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	7	—	nS	V <sub>GS</sub> = 10V, R <sub>L</sub> = 562Ω, R <sub>G</sub> = 10Ω, I <sub>D</sub> = 0.4A
Turn-On Rise Time	t <sub>r</sub>	—	6.4	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	18.9	—		
Turn-Off Fall Time	t <sub>f</sub>	—	56.6	—		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	—	103	—	nS	I <sub>F</sub> = 1A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	—	314	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  - I<sub>AR</sub> and E<sub>AR</sub> rating are based on low frequency and duty cycles to keep T<sub>J</sub> = +25°C.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.

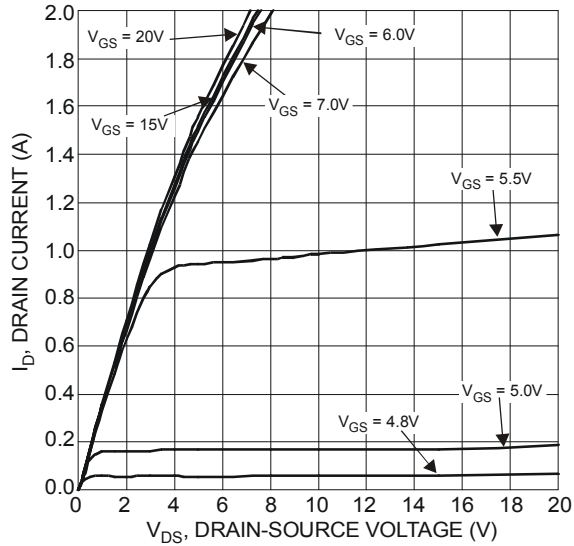


Figure 1 Typical Output Characteristics

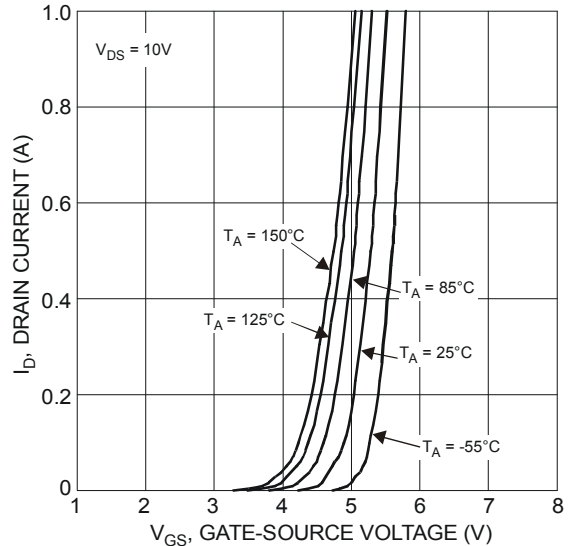


Figure 2 Typical Transfer Characteristics

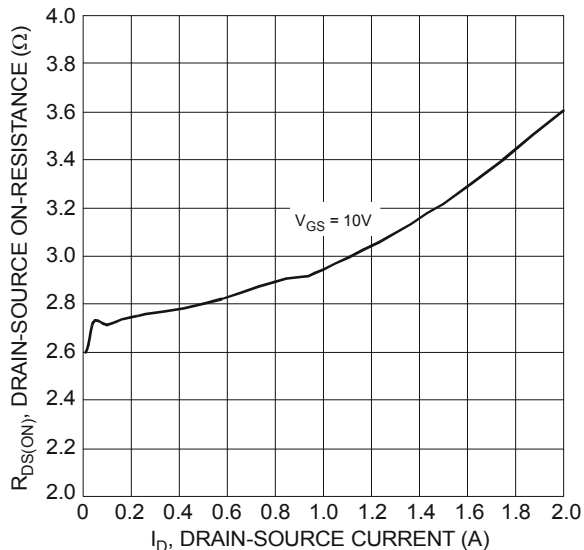


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

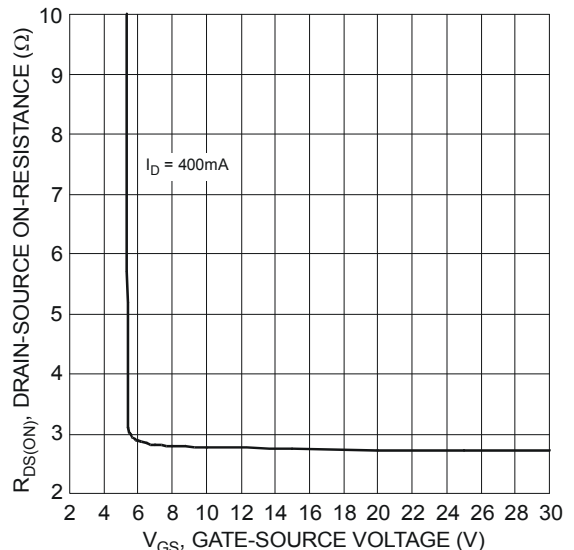


Figure 4 Typical Transfer Characteristic

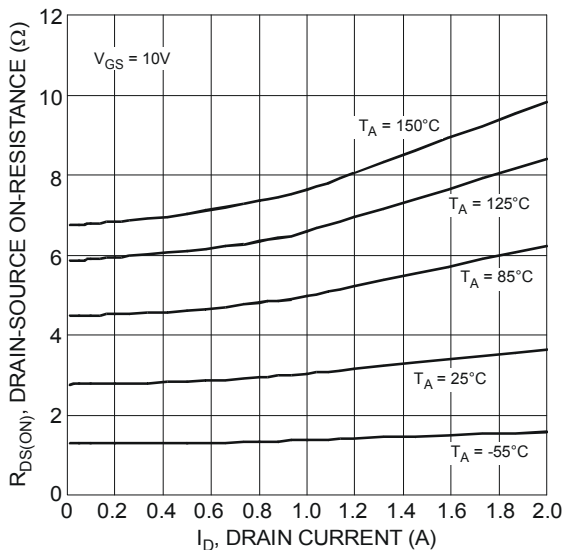


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

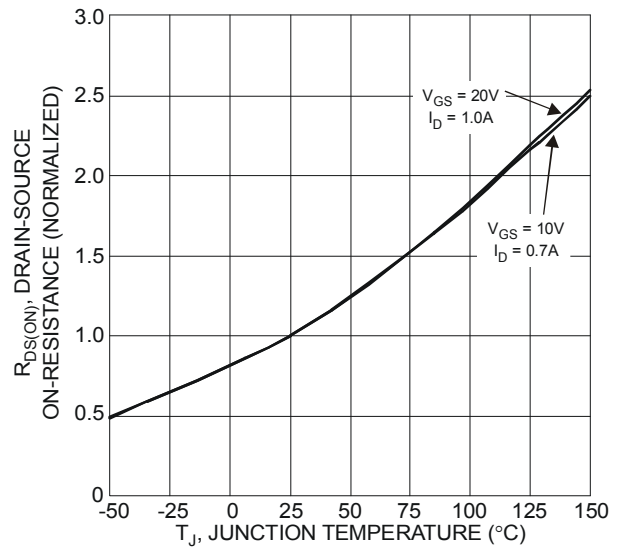


Figure 6 On-Resistance Variation with Temperature

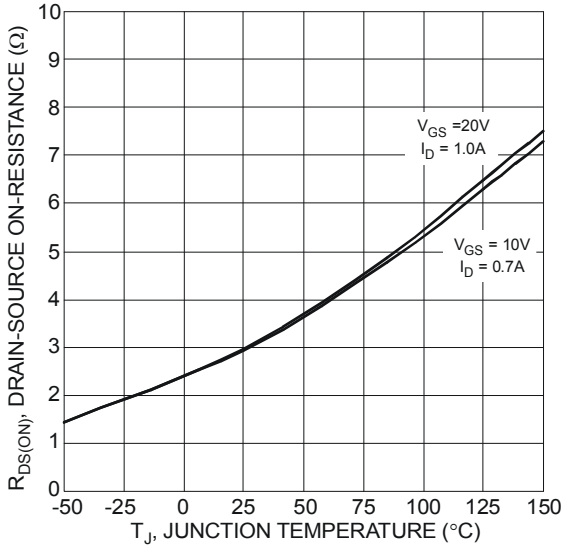


Figure 7 On-Resistance Variation with Temperature

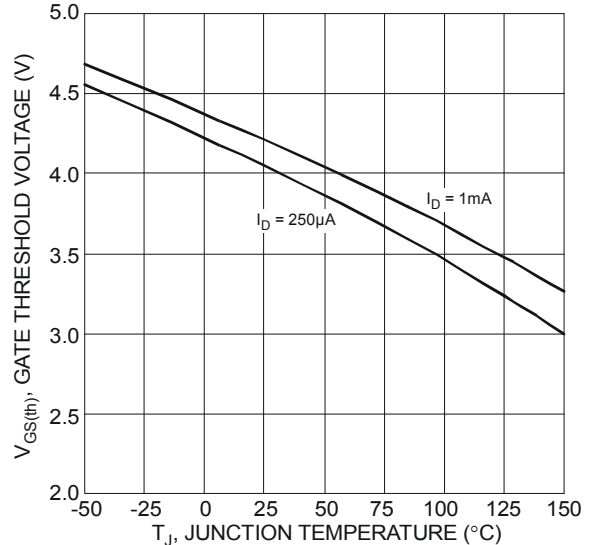


Figure 8 Gate Threshold Variation vs. Ambient Temperature

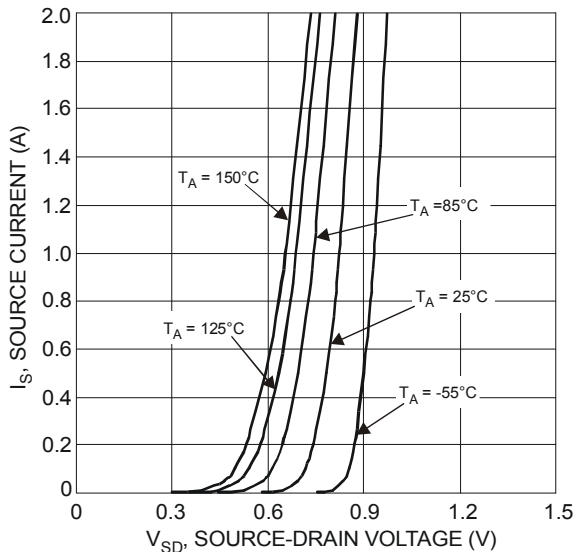


Figure 9 Diode Forward Voltage vs. Current

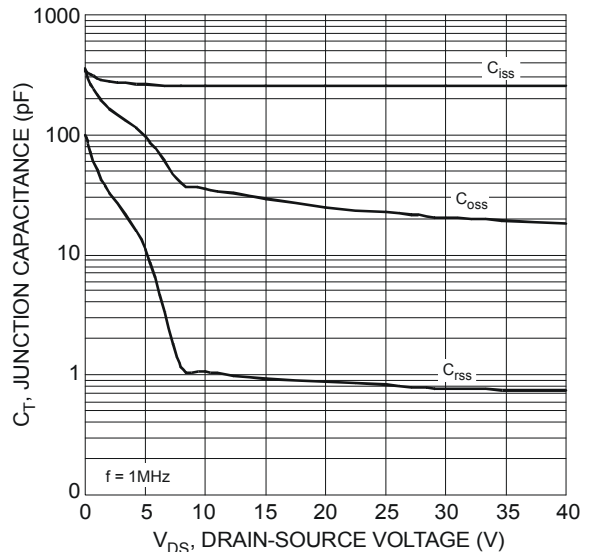


Figure 10 Typical Junction Capacitance

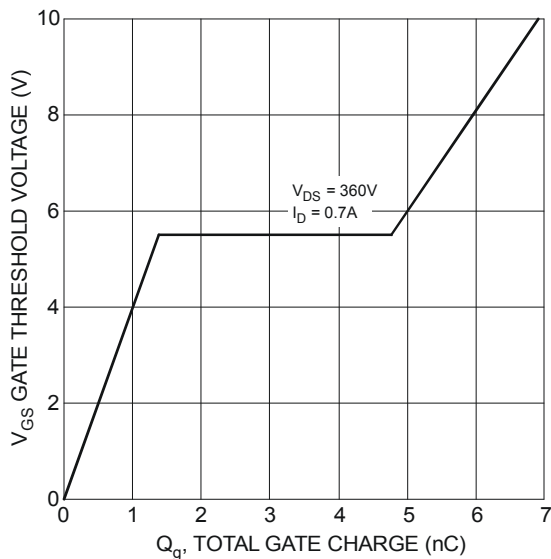


Figure 11 Gate Charge

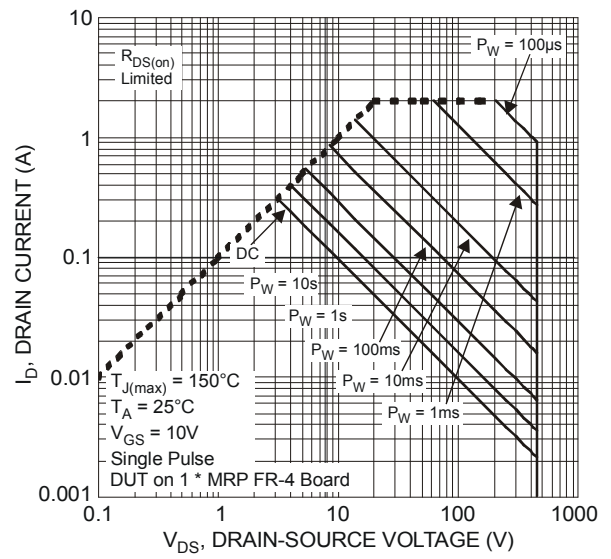
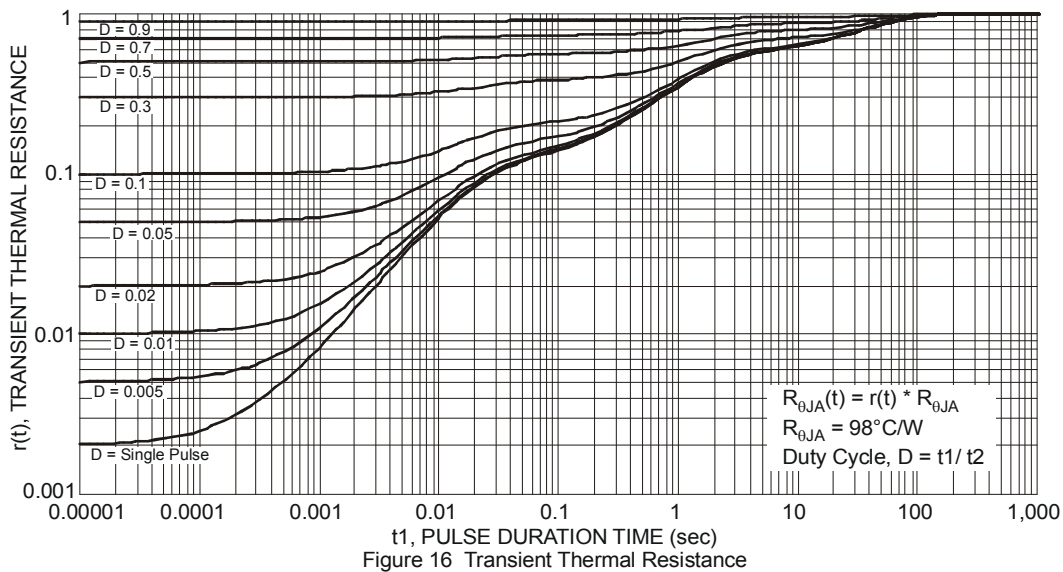
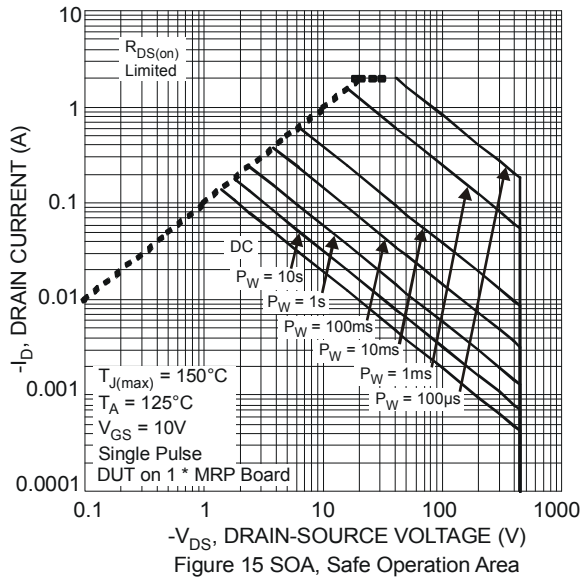
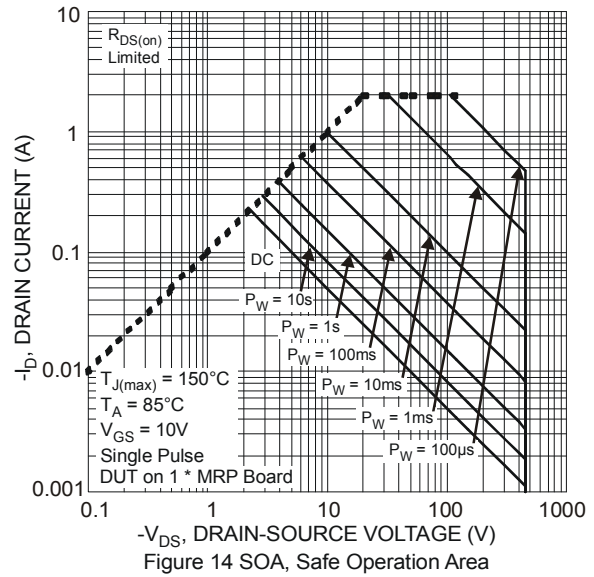
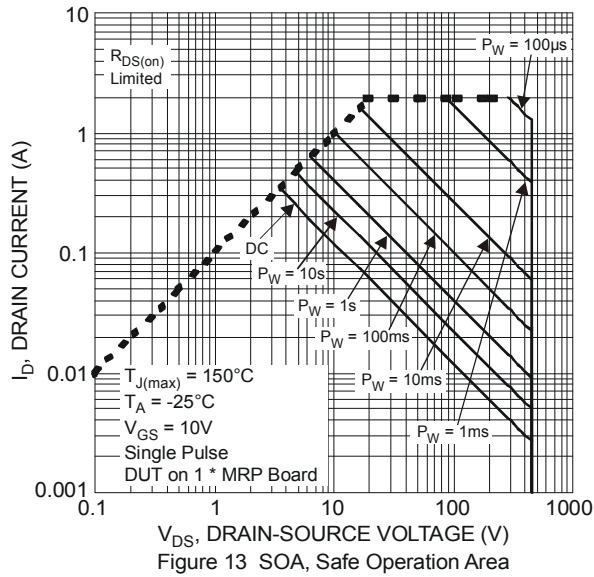
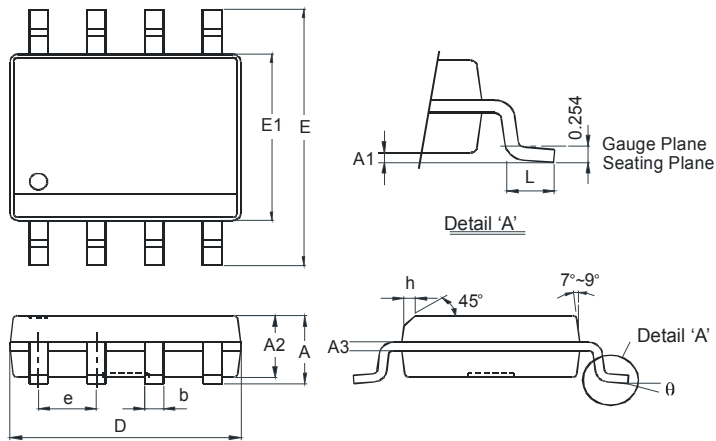


Figure 12 SOA, Safe Operation Area



### Package Outline Dimensions

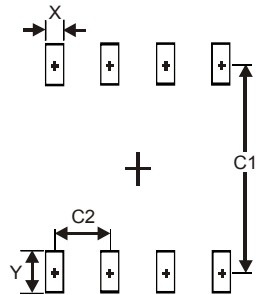
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	—	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	—	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

### Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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