PI6LC48P25104

Single Output LVPECL Clock Generator

Features

- Single differential LVPECL output
- Output frequency range: 145MHz to 187.5MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz - 20MHz): 0.3ps (typical)
- Full 3.3V or 2.5V supply modes
- Commercial and industrial operating temperature
- Available in lead-free package: 8-TSSOP

Description

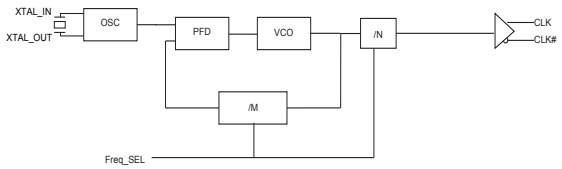
The PI6LC48P25104 is a single output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 25MHz, it can generate 156.25MHz, or 187.5MHz output. Using other crystal frequencies, it can generate other popular frequencies for networking and server storage systems.

The PI6LC48P25104 uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, so it is ideal for SATA/SAS or Ethernet interface in all kind of systems.

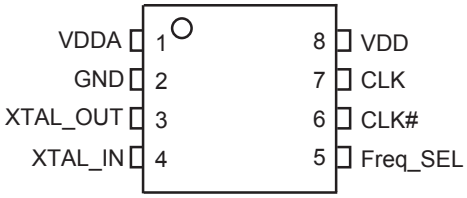
Applications

- Networking systems
- Servers and Storage systems

Block Diagram



Pin Configuration



Pinout Table

Pin No.	Pin Name	I/O Type		Description
1	VDDA	Power		Analog Power Supply
2	GND	Power		Ground
3, 4	XTAL_OUT, XTAL_IN	Crystal		Crystal Input and Output
5	Freq_SEL	Input	Pull Down	"LOW", output is multiplied by 6.25, "HIGH", output is multiplied by 7.5.
6, 7	CLK#, CLK	Output		Output Clock
8	VDD	Power		Core Power Supply

Output Frequency Table

Xtal Frequency (MHz)	Freq_SEL	Output Frequency (MHz)
20	1	150
21.25	1	159.375
24	0	150
25	0	156.25
	1	187.5
25.5	0	159.375
30	0	187.5

Typical Crystal Requirement

Parameter		Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency	Freq_SEL = 0	23.2		30	MHz
	Freq_SEL = 1	19.33		25	
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Recomended Crystal Specification

Pericom recommends:
a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm
http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm
http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature..... -65°C to+155°C
Ambient Temperature with Power Applied.....-40°C to+85°C
3.3V Analog Supply Voltage .....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, ($V_{DD} = V_{DDA}$, T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min.	Typ	Max	Units
V_{DD}, V_{DDA}	Core, Analog Supply Voltage		3.135	3.3	3.465	V
V_{DD}, V_{DDA}	Core, Analog Supply Voltage		2.375	2.5	2.625	V
I_{GND}	Power Supply Current				70	mA
I_{DDA}	Analog Supply Current				25	mA

LVPECL DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ	Max	Units
V_{OH}	Output High Voltage(1)	V_{DD} = 3.3V	1.9		2.4	V
		V_{DD} = 2.5V	1.1		1.6	
V_{OL}	Output Low Voltage(1)	V_{DD} = 3.3V	1.2		1.6	V
		V_{DD} = 2.5V	0.4		0.8	

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

LVPECL AC Electrical Characteristics

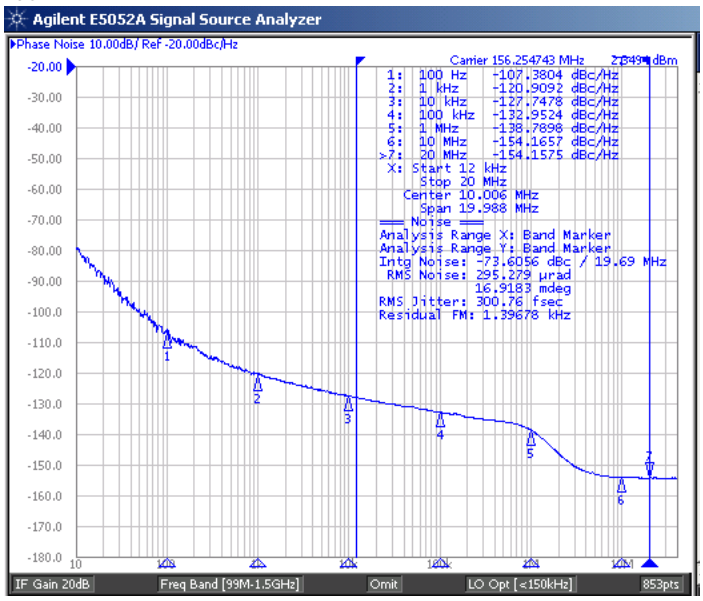
LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

Symbol	Parameter	Condition	Min..	Typ.	Max	Units
f_{OUT}	Output Frequency		145	125	187.5	MHz
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(1)	156.25MHz, (12kHz - 20MHz)		0.30		ps
		187.5MHz, (12kHz - 20MHz)		0.33		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%			400	ps
o_{DC}	Output Duty Cycle		48		52	%

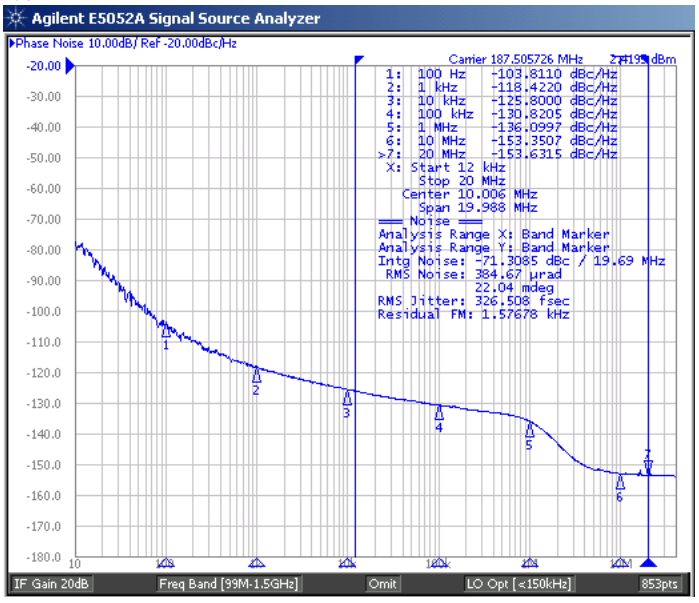
Note:
1. Please refer to the Phase Noise Plots.

Phase Noise Plots

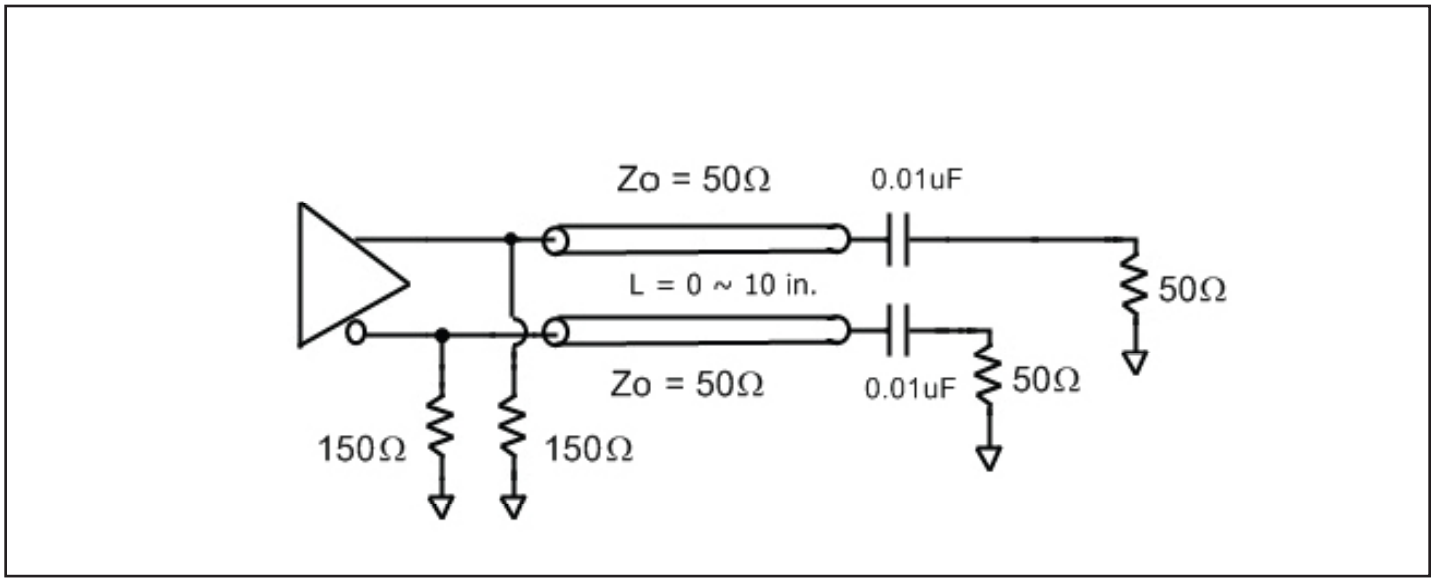
f_{OUT} = 156.25MHz



f_{OUT} = 187.5MHz

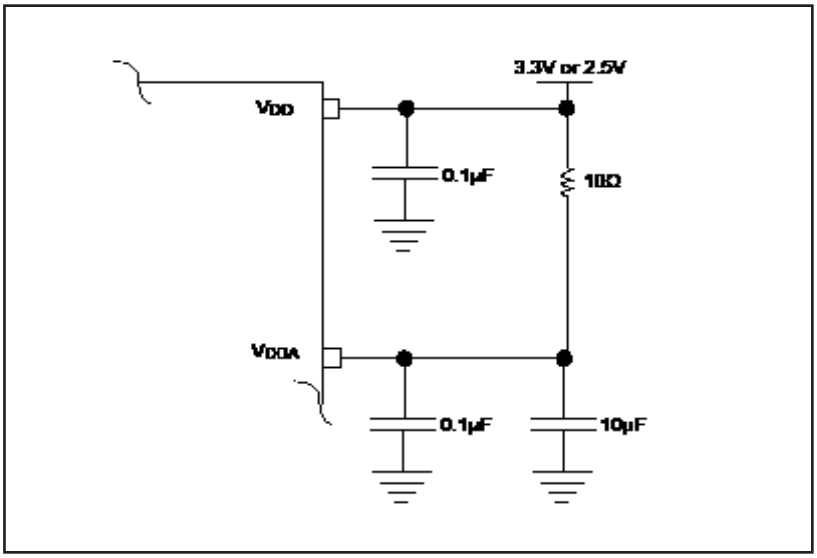


LVPECL Test Circuit



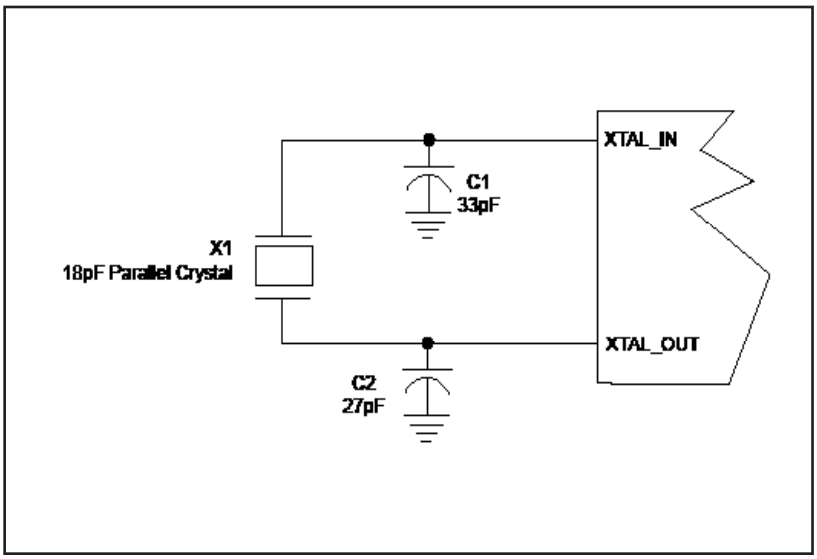
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P25104 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



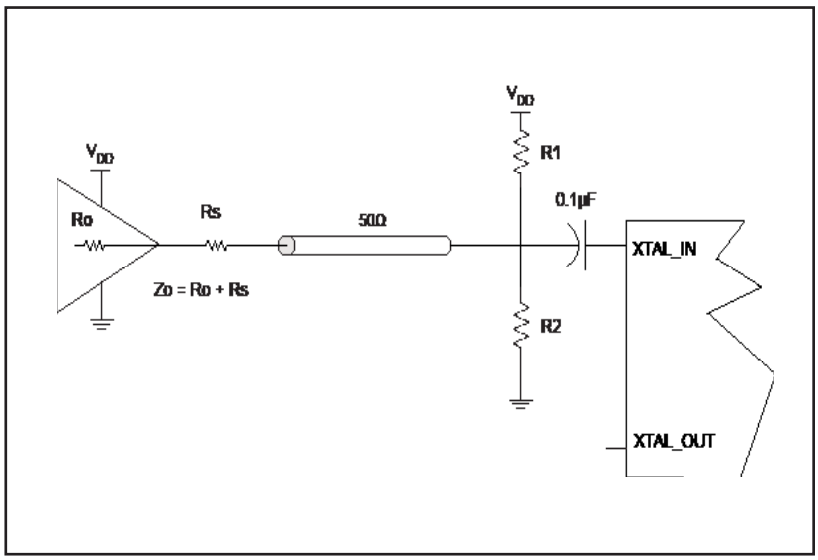
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



LVCMOS to XTAL Interface

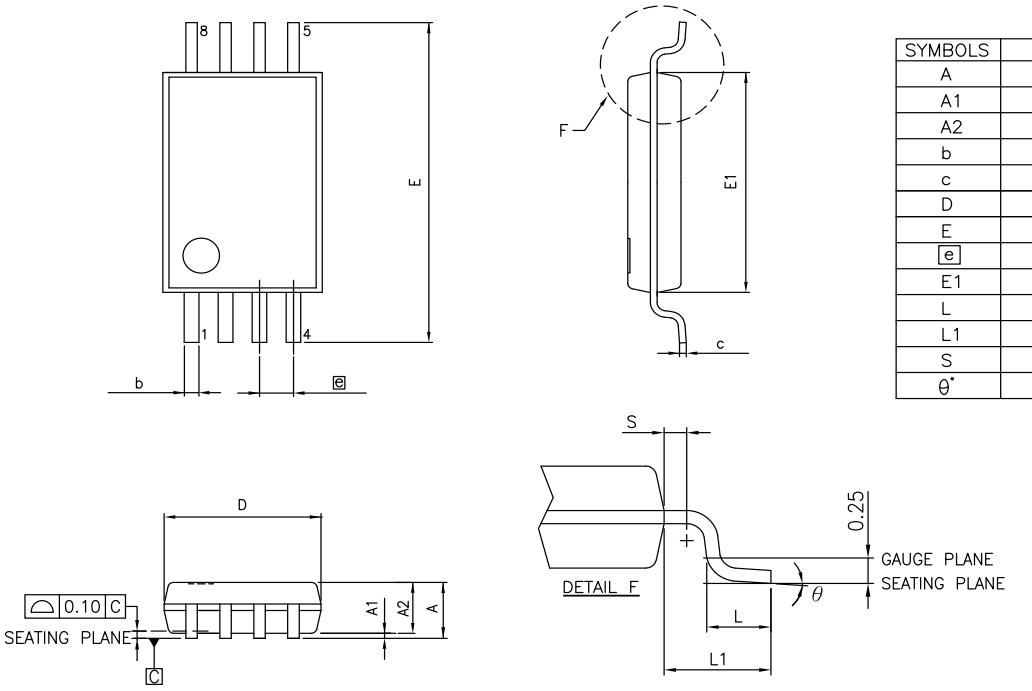
The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	124.0 °C/W
Θ_{JC}	Junction-to-case thermal resistance		37.0 °C/W

Packaging Mechanical: 8-Contact TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E		6.40 BSC	
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

UNIT : MM

Notes:
1. Refer JEDEC MO-153F/AA
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 8 pin, 173mil wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1308 **REVISION: F**

12-0370

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P25104LE	L	Pb-free & Green, 8-pin TSSOP	Commercial
PI6LC48P25104LIE	L	Pb-free & Green, 8-pin TSSOP	Industrial

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)