

DUAL N-CANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR
Product Summary

BV_{DSS}	$R_{DS(on)}$ Max	I_D Max $T_A = +25^\circ C$
60V	$3\Omega @ V_{GS} = 5V$	0.3A

Features and Benefits

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **ESD Protected Up To 2kV**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.** <https://www.diodes.com/quality/product-definitions/>
- **An Automotive-Compliant Part is Available Under Separate Datasheet ([DMN601DWKQ](#))**

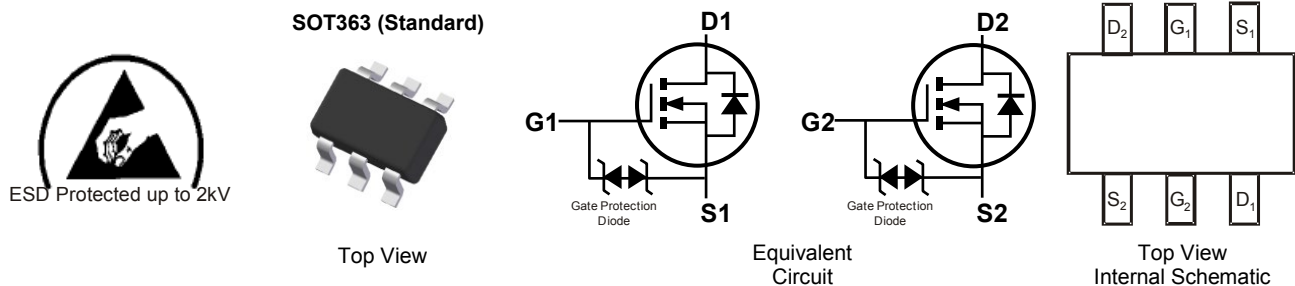
Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Motor Control
- Power Management Functions

Mechanical Data

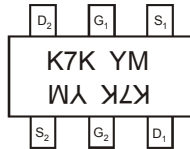
- Case: SOT363 (Standard)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead-Free Plating). Solderable per MIL-STD-202, Method 208 (E3)
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)


Ordering Information (Note 4)

Part Number	Case	Packaging
DMN601DWK-7	SOT363 (Standard)	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

SOT363


K7K = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: 1 = 2021)
 M or \bar{M} = Month (ex: 9 = September)

Date Code Key

Year	2005	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	S	I	J	K	L	M	N	O	P	R	S

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current (Note 5)	I_D	Continuous	305
		Pulsed (Note 6)	800

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	200	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	625	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 10\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.6	2.5	V	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	1.3	2.0	Ω	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
			1.5	3.0		$V_{GS} = 5\text{V}, I_D = 0.05\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	80	—	—	ms	$V_{DS} = 10\text{V}, I_D = 0.2\text{A}$
Diode Forward Voltage	V_{SD}	0.5	0.8	1.4	V	$V_{GS} = 0\text{V}, I_S = 115\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	30	50	pF	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	4.2	25	pF	
Reverse Transfer Capacitance	C_{riss}	—	2.9	5.0	pF	
Gate Resistance	R_g	—	133	—	Ω	$f = 1\text{MHz}, V_{GS} = 0\text{V}, V_{DS} = 0\text{V}$
Total Gate Charge	Q_g	—	304	—	pC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V},$ $I_D = 250\text{mA}$
Gate-Source Charge	Q_{gs}	—	203	—	pC	
Gate-Drain Charge	Q_{gd}	—	84	—	pC	
Turn-On Delay Time	$t_{D(on)}$	—	3.9	—	nS	$V_{DD} = 30\text{V}, V_{GS} = 10\text{V},$ $R_G = 25\Omega, I_D = 200\text{mA}$
Turn-On Rise Time	t_r	—	3.4	—	nS	
Turn-Off Delay Time	$t_{D(off)}$	—	15.7	—	nS	
Turn-Off Fall Time	t_f	—	9.9	—	nS	

- Notes:
- Device mounted on FR-4 PCB.
 - Pulse width $\leq 10\mu\text{s}$, duty cycle $\leq 1\%$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

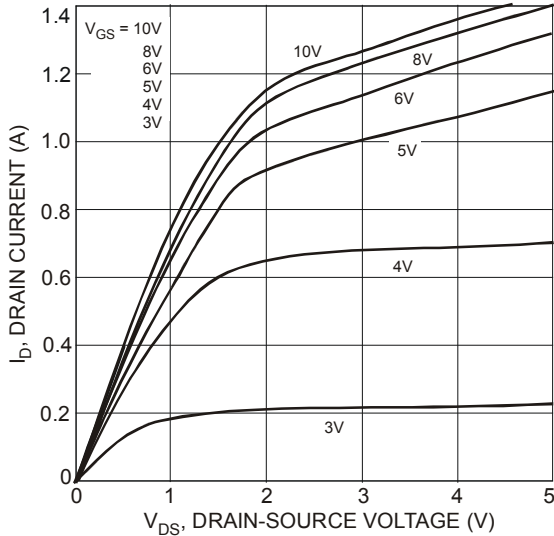


Figure 1 Typical Output Characteristics

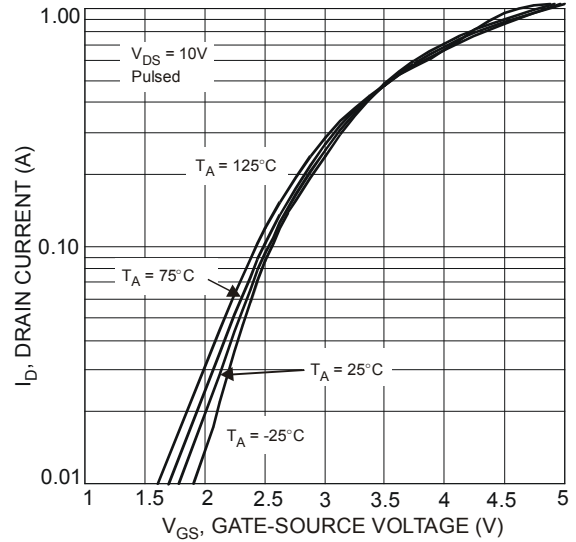


Figure 2 Typical Transfer Characteristics

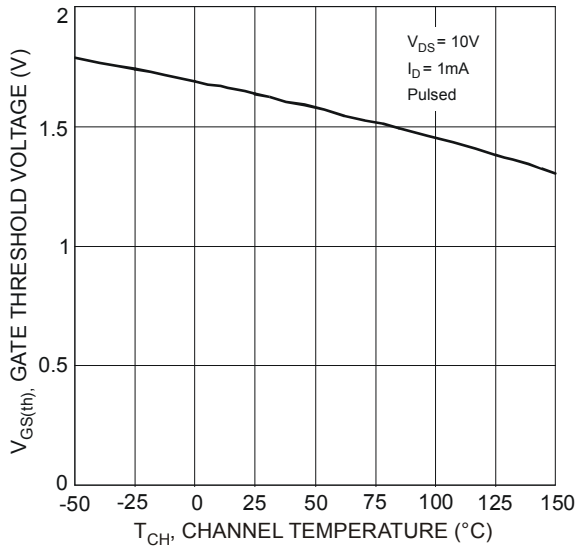


Figure 3 Gate Threshold Voltage vs. Channel Temperature

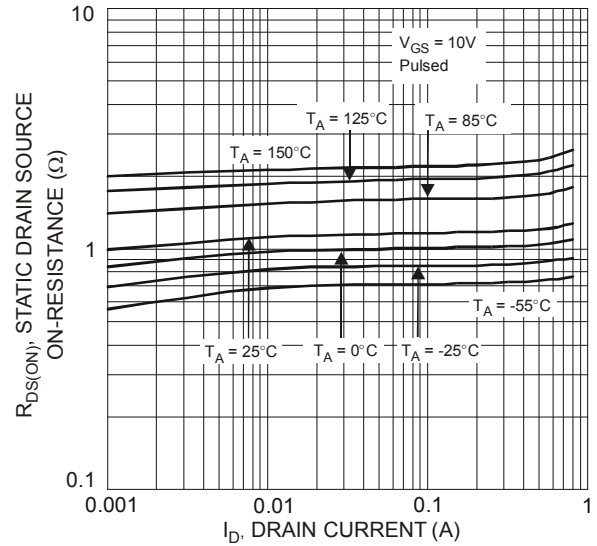


Figure 4 Static Drain-Source On-Resistance vs. Drain Current

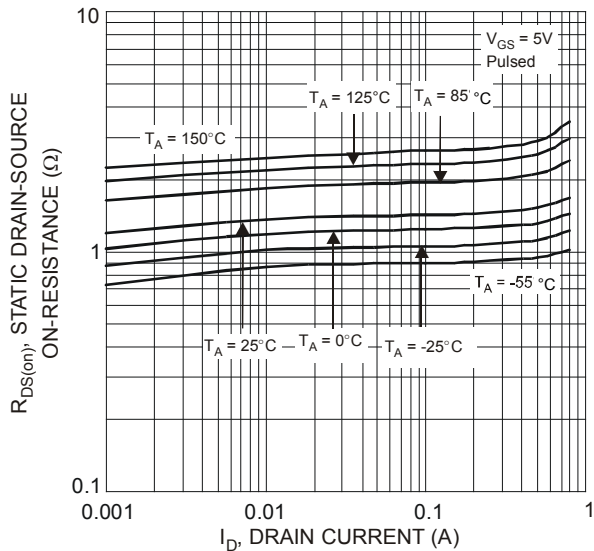


Figure 5 Static Drain-Source On-Resistance vs. Drain Current

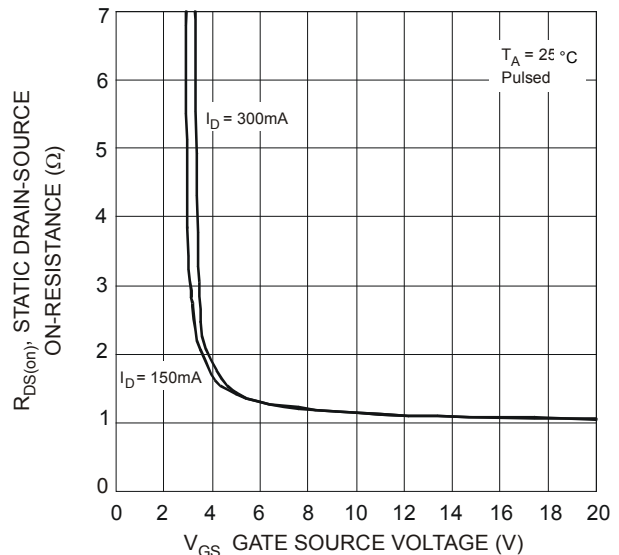


Figure 6 Static Drain-Source On-Resistance vs. Gate-Source Voltage

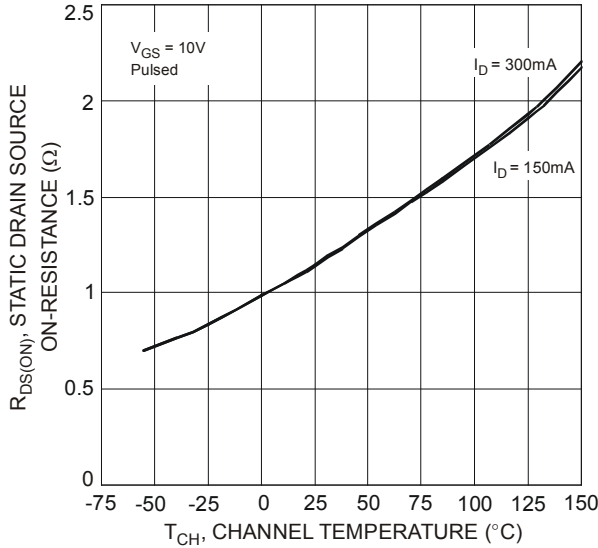


Figure 7 Static Drain-Source On-State Resistance vs. Channel Temperature

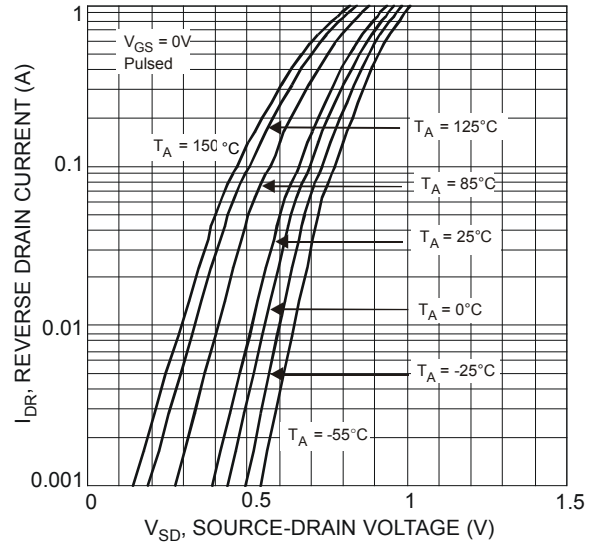


Figure 8 Reverse Drain Current vs. Source-Drain Voltage

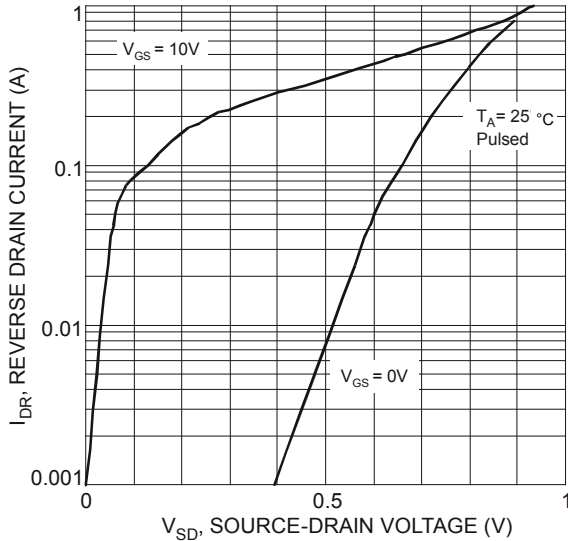


Figure 9 Reverse Drain Current vs. Source-Drain Voltage

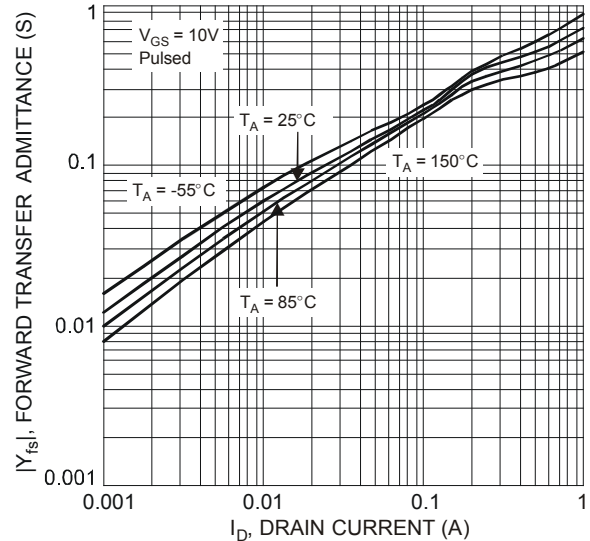


Figure 10 Forward Transfer Admittance vs. Drain Current

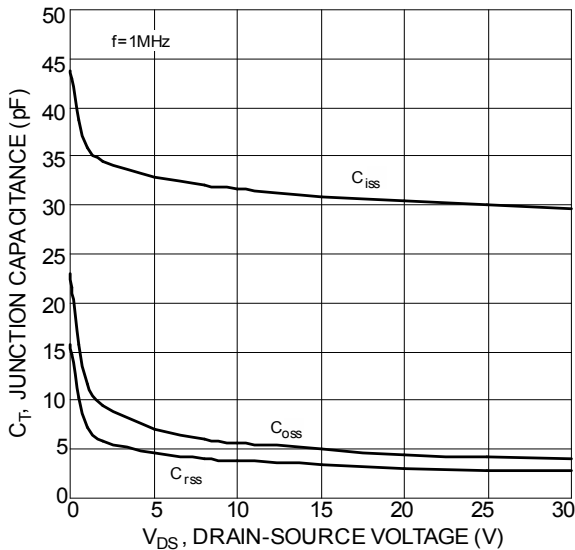


Figure 11 Typical Junction Capacitance

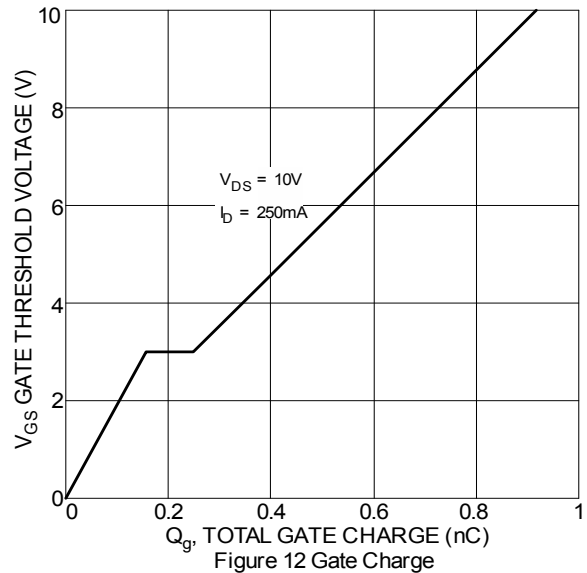
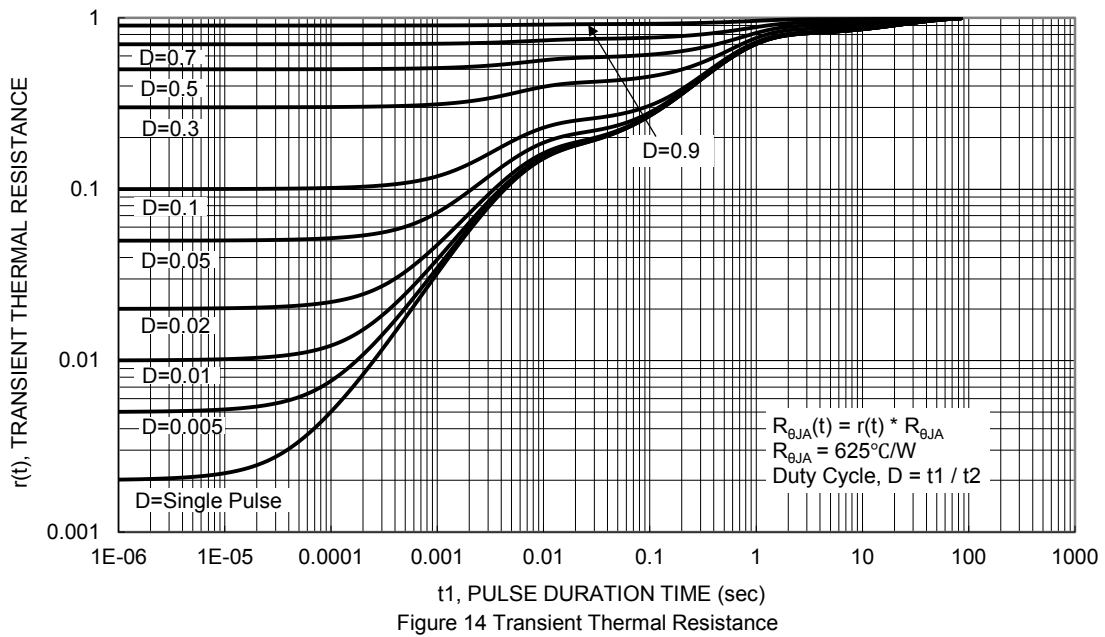
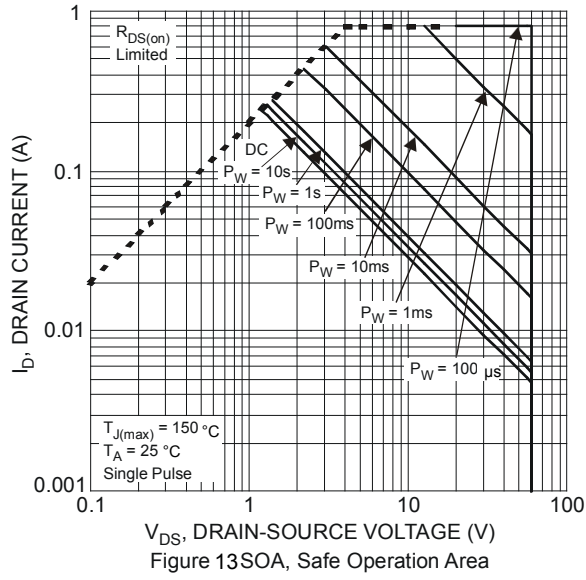


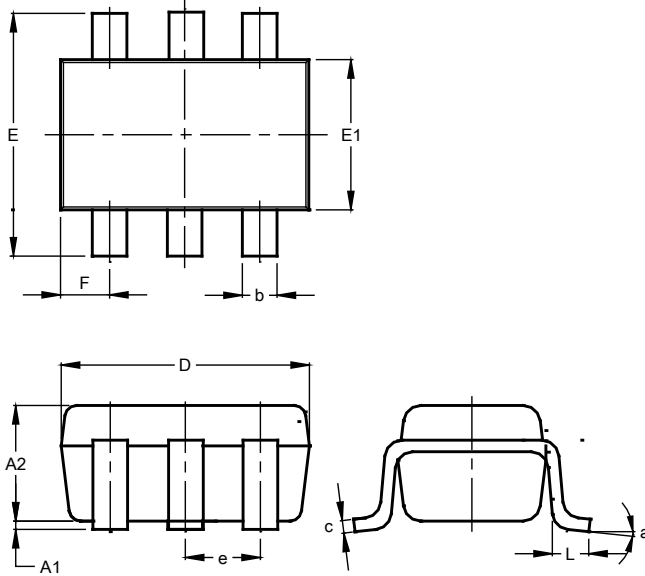
Figure 12 Gate Charge



Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT363 (Standard)

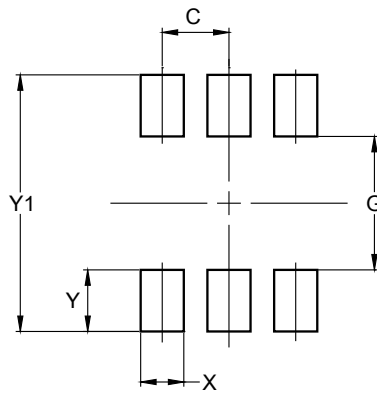


SOT363 (Standard)			
Dim	Min	Max	Typ
A1	0.00	0.10	0.05
A2	0.80	1.00	0.90
b	0.10	0.35	0.225
c	0.08	0.22	0.15
D	1.80	2.20	2.00
E	2.00	2.45	2.225
E1	1.15	1.35	1.25
e	--	--	0.65
F	0.25	0.45	0.35
L	0.25	0.46	0.355
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT363 (Standard)



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

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