PI3HDMI101

1:1 Active HDMI™ ReDriver™ with Optimized Equalization & I²C Buffer

Features

- Supply voltage, V_{DD} = 3.3V ±5%
- Support for both DVI and HDMI™ signals
- Supports both AC-coupled and DC-coupled inputs
- Supports Deep Color™
- High Performance, up to 2.5 Gbps per channel
- 5V Tolerance on I²C path
- Integrated 50-Ohm (±10%) termination resistors at each high speed signal input
- Rx Sense Support, CLK-off channel is switched to 250K-Ohm pull-up vs. 50-Ohm pull-up
- Configurable output swing control (400mV, 500mV, 600mV, 750mV, 1000mV)
- Configurable Pre-Emphasis levels (0dB, 1.5dB, 3.5dB, & 6.0dB, 9.0dB)
- Configurable De-Emphasis (0dB, -3.5dB, -6.0dB, -9.5dB)
- Optimized Equalization
  Single default setting will support all cable lengths
- 8kV Contact ESD protection on all input/output data channels per IEC 61000-4-2
- Hot insertion support on output high speed pins & SCL/SDA pins only
- Propagation delay ≤ 1ns
- High Impedance Outputs when disabled
- Packaging (Pb-free & Green): 42-contact TQFN (ZH42)

Description

Pericom Semiconductor's PI3HDMI101 1:1 active ReDriver™ circuit is targeted for high-resolution video networks that are based on DVI/HDMI™ standards and TMDS signal processing. The PI3HDMI101 is an active ReDriver with Hi-Z outputs. The device receives differential signals from selected video components and drives the video display unit. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times which are reduced during transmission across long distances.

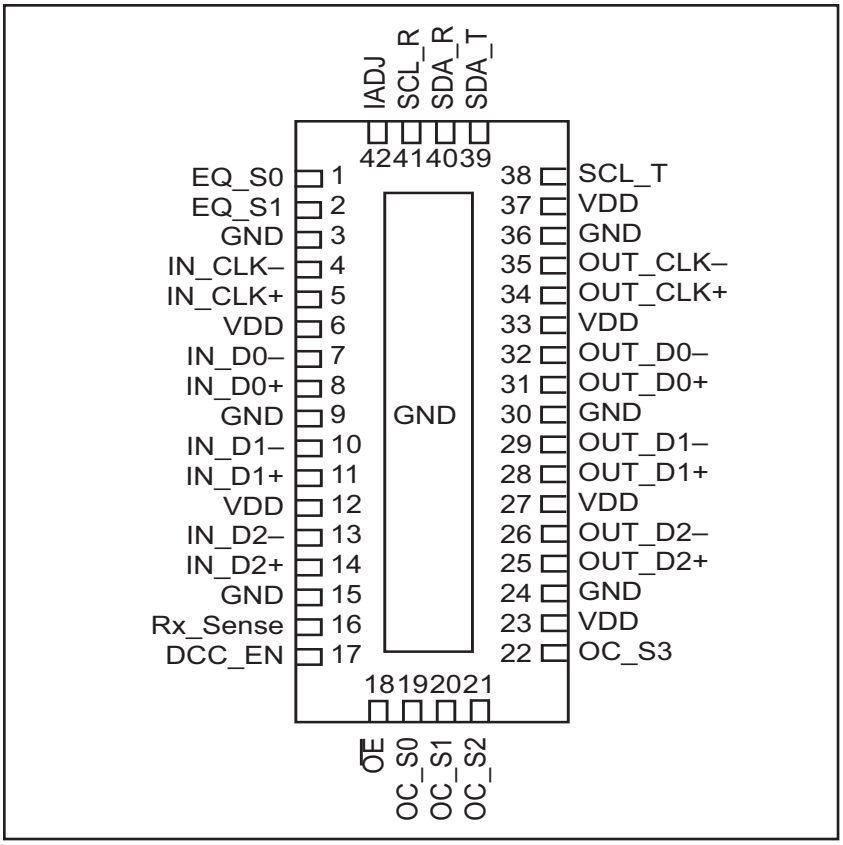
Each complete HDMI/DVI channel also has slower speed, side band signals, that are required to be switched. Pericom's solution provides a complete solution by integrating the side band buffer together with the high speed buffer in a single solution. Using Equalization at the input of each of the high speed channels, Pericom can successfully eliminate deterministic jitter caused by long cables from the source to the sink. The elimination of the deterministic jitter allows the user to use much longer cables (up to 25 meters).

The maximum DVI/HDMI Bandwidth of 2.5 Gbps provides 36-bit Deep Color™ support, which is offered by HDMI revision 1.3. The PI3HDMI101 also provides enhanced robust ESD/EOS protection of 8kV, which is required by many consumer video networks today.

The Optimized Equalization provides the user a single optimal setting that can provide HDMI compliance for all cable lengths: 1meter to 20meters and color depths of 8bit/ch, or 12bit/ch.

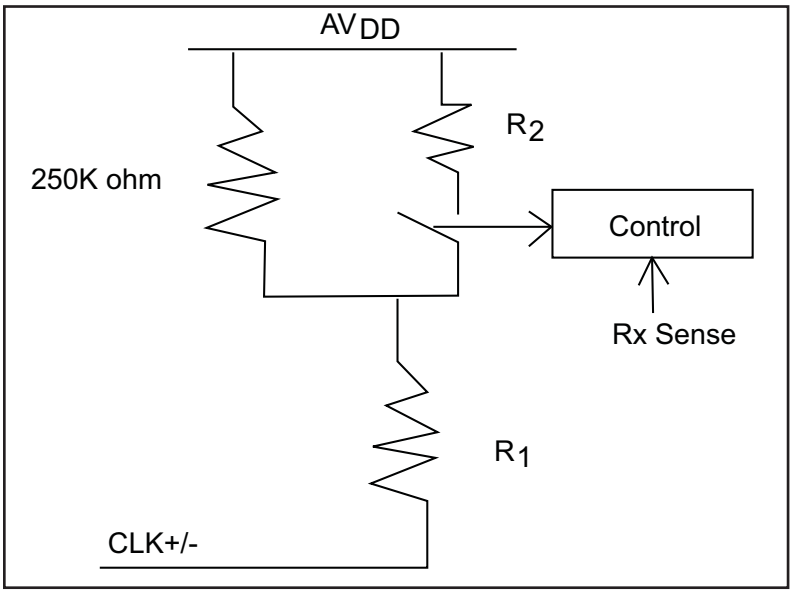
Pericom also offers the ability to fine tune the equalization settings in situations where cable length is known. For example, if 25meter cable length is required, Pericom's solution can be adjusted to 16dB EQ to accept 25meter cable length.

Pin Configuration



TMDS Receiver Block

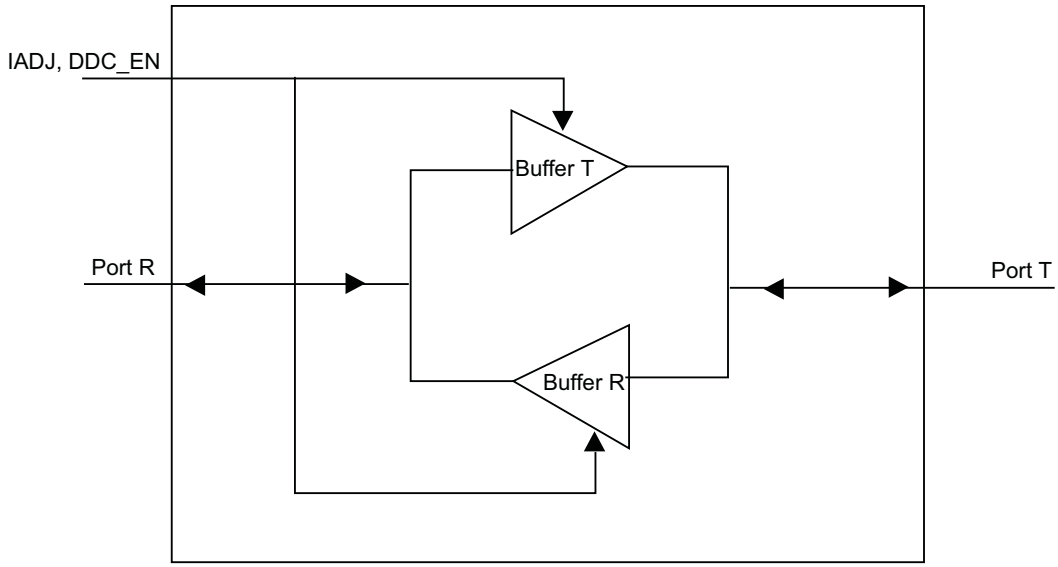
Each high speed data and clock input has the same integrated equalization that can eliminate deterministic jitter caused by input traces or cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, and DDC signals. Pixel clock channel has following termination scheme for Rx Sense support.



Rx Sense	
L	R_2 switch is open, CLK+/- termination is 250kΩ
H	R_2 switch is closed, CLK+/- termination is 50Ω

Although the TMDS clock input channel (pin 4 and 5) has different termination scheme when port is off, user can still connect TMDS data channels to these pins for better layout if required. Any of the 4 differential inputs and outputs can have data or clock signals passing through.

I²C Buffer



The VOL of the Buffer R is around 0.2V.
The VOL of the Buffer T is around 0.7V.

Functional Truth Tables

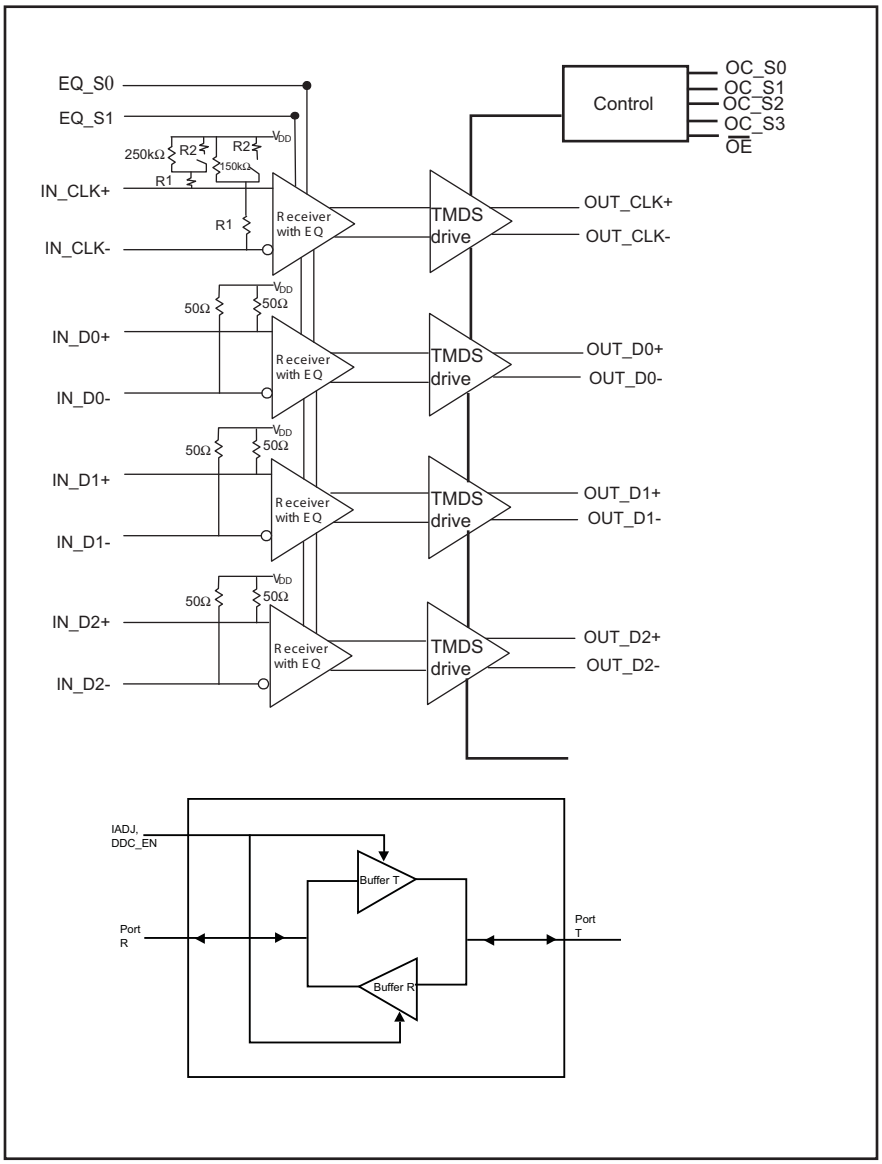
IADJ	External Pull-Up Range
H	1KΩ to 2KΩ (HDMI spec)
L	> 3KΩ (4.7KΩ typically)

DDC_EN	Port T / Port R (if no external pull-up resistor
L	Hi-Z (I²C buffer disable)
H	(I²C buffer enable)

Pin Description

Pin #	Pin Name	I/O	Description
5 8 11 14	IN_CLK+ IN_D0+ IN_D1+ IN_D2+	I	TMDS Positive inputs
4 7 10 13	IN_CLK- IN_D0- IN_D1- IN_D2-	I	TMDS Negative inputs
3, 9, 15, 24, 30, 36	GND	P	Ground
18	$\overline{OE}$	I	Output Enable, Active LOW
41	SCL_R	I/O	DDC Clock , Source Side
40	SDA_R	I/O	DDC Data, Source Side
6, 12, 23, 27, 33, 37	V_{DD}	P	3.3V Power Supply
34 31 28 25	OUT_CLK+ OUT_D0+ OUT_D1+ OUT_D2+	O	TMDS positive outputs
35 32 29 26	OUT_CLK- OUT_D0- OUT_D1- OUT_D2-	O	TMDS negative outputs
1 2	EQ_S0 EQ_S1	I	Equalizer controls, both pins with internal pull-ups
19 20 21 22	OC_S0 OC_S1 OC_S2 OC_S3	I	Output buffer controls Note: All 4 pins have internal pull-ups
17	DDC_EN	I	I²C path enable
38	SCL_T	I/O	DDC Clock, Sink side
39	SDA_T	I/O	DDC Data, Sink side
16	Rx_Sense	I	Rx_Sense control
42	IADJ	I	High/Low Voltage Selection, depends on I²C external pull-up range

Complete high speed input Rx block is as follows:



Truth Table

$\overline{OE}$	Function
0	Active
1	All TMDS outputs are Hi-Z

Truth Table 1

OC_S3(2)	OC_S2(2)	OC_S1(2)	OC_S0(2)	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	660	-3.5dB
1	1	1	0	500	-6dB
1	1	1	1	330	-9dB

EQ Setting Value Logic Table

EQ_S1(2)	**EQ_S0(2)**	**Setting Value @ 825MHz**
0	0	3dB on all high speed inputs
0	1	8dB on all high speed inputs
1	0	12dB on all high speed inputs
1	1	16dB on all high speed inputs

Notes:

1. External pull-ups are required along SCL/SDA path
2. Internal 100Kohm pull-ups

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential..... –0.5V to +4.0V
DC Input Voltage ..... –0.5V to V_{DD}
DC Output Current..... 120mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
T_A	Operating free-air temperature	0		70	°C
TMDS Differential Pins					
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
V_{IC}	Input common mode voltage	2		V_{DD} + 0.01	V
V_{DD}	TMDS output termination voltage	3.135	3.3	3.465	
R_T	Termination resistance when RxSense pin is HIGH	45	50	55	ohm
TMDS Data Rate	Signaling rate	0.25		2.5	Gbps
Control Pins (OC_Sx, EQ_Sx, $\overline{OE}$, DDC_EN)					
V_{IH}	LVTTL High-level input voltage	2		V_{DD}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	
DDC Pins (SCL_R, SCL_T, SDA_R, SDA_T)					
$V_{I(DDC)}$	Input voltage	GND		5.5	V
I²C Pins (SCL_T, SDA_T)					
V_{IH}	High-level input voltage	0.7 x V_{DD}		5.5	V
V_{IL}	Low-level input voltage	-0.5		0.3 x V_{DD}	
V_{ICL}	Low-level input voltage contention (1)	-0.5		0.4	
I²C Pins (SCL_R, SDA_R)					
V_{IH}	High-level input voltage	0.7 x V_{DD}		5.5	V
V_{IL}	Low-level input voltage	-0.5		0.3 x V_{DD}	

Note:
1. VIL specification is for the first low level seen by the SCL/SDA lines. V_{ICL} is for the second and subsequent low levels seen by the TSCL/TSDA lines.

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
I_{DD}	Supply Current	$V_{IH} = V_{DD}$, $V_{IL} = V_{DD}$ - 0.4V, R_T = 50-ohm, V_{DD} = 3.3V Data Inputs = 1.65 Gbps HDMI data pattern CLK Inputs = 165 MHz clock OC_Sx = Low, x = 0,1,2,3		120		mA
P_D	Power Dissipation			400		mW
I_{DDQ}	Standby Current	$\overline{OE}$ = HIGH, VDD = 3.3V, Source = off		2		mA
TMDS Differential Pins						
V_{OH}	Single-ended high-level output voltage	V_{DD} = 3.3V, R_T = 50-ohm Pre-emphasis/De-emphasis = 0dB	V_{DD}-10		V_{DD} + 10	mV
V_{OL}	Single-ended low-level output voltage		V_{DD} - 600		V_{DD} - 400	
V_{swing}	Single-ended output swing voltage		400		600	
$V_{OD(O)}$	Overshoot of output differential voltage			6%	15%	2x V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage			12%	25%	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			0.5	5	mV
$I_{(OS)}$	Short circuit output current				12	mA
$V_{ODE(SS)}$	Steady state output differential voltage	OC_Sx = GND, Data Inputs = 250 Mbps HDMI data pattern, 25 MHz pixel clock, x = 0,1,2,3	560		840	mVp-p
$V_{ODE(PP)}$	Peak-to-peak output differential voltage		800		1200	
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	I_I = 10µA	V_{DD} - 10		V_{DD} + 10	mV
R_{INT}	Input termination resistance	V_{IN} = 2.9V, RxSense pin = HIGH	45	50	55	ohm
Control Pins ($\overline{OE}$, DDC_EN, IADJ)						
I_{IH}	High-level digital input current	V_{IH} = 2V or V_{DD}	-10		10	µA
I_{IL}	Low-level digital input current	V_I = GND or 0.8 V	-10		10	
I²C Pins (SCL_T, SDA_T) (T Port)						
I_{ikg}	Input leakage current	V_I = 5.5 V	-50		50	µA
		$V_I = V_{DD}$	-20		20	
I_{OH}	High-level output current	V_O = 3.6 V	-10		10	
I_{IL}	Low-level input current	V_{IL} = GND	-40		40	
V_{OL}	Low-level output voltage	I_{OL} = 2.5 mA IADJ = H	0.65		0.9	V
C_{IO}[1]	Input/output capacitance	V_{DD} = 0V or 3.0V, Frequency = 100kHz		4	7	pF
$V_{OH(TTL)}$[2]	TTL High-level output voltage	I_{OH} = -8 mA	2.4			V
$V_{OL(TTL)}$[2]	TTL Low-level output voltage	I_{OL} = 8 mA			0.4	

Note:

1. Measured at Vbias = 0V or 5V, Vrms = 0.2V;
   Vbias = 1.65V, Vrms = 0.84V;
   Vbias = 2.5V, Vrms = 1.2V.
2. Voh/Vol of external driver at the R and T ports.

(Table Continued)

I²C Pins (SCL_R, SDA_R Port)						
I_{ikg}	Input leakage current	V_I = 5.5 V	-50		50	µA
		$V_I = V_{DD}$	-10		10	
I_{OH}	High-level output current	V_O = 3.6 V	-10		10	
I_{IL}	Low-level input current	V_{IL} = GND	-10		10	
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, IADJ = H			0.2	V
C_I	Input capacitance	V_I = 5.0 V or 0 V, Freq = 100kHz			25	pF
		V_I = 3.0 V or 0 V, Freq = 100kHz			10	

Switching Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
TMDS Differential Pins						
tpd	Propagation delay	V_{DD} = 3.3V, R_T = 50-ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t_r	Differential output signal rise time (20% - 80%)		75		240	
t_f	Differential output signal fall time (20% - 80%)		75		240	
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew(2)				100	
$t_{CLKjit(pp)}$	Peak-to-peak output jitter for TMDS clock channel	pre-emphasis/de-emphasis = 0dB, Data Inputs = 1.65 Gbps HDMI data pattern CLK input = 165 MHz clock		15	30	
$t_{Datajit(pp)}$	Peak-to-peak output jitter for TMDS data channels			18	50	
t_{DE}	De-emphasis duration	de-emphasis = -3.5dB, Data Inputs = 250 Mbps HDMI data pattern, CLK output = 25 MHz clock		240		
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				200	
t_{dis}	Disable time				10	
I²C PINS (SCL_R, SDA_R, SCL_T, SDA_T)						
t_{PLH}	Propagation delay time, low-to-high-level output SCL_T/SDA_T to SCL_R/SDA_R	IADJ = V_{DD} C_{LOAD} = 300 pF Tbuffer : Rpu = 2K, Vpu = 3.0V			500	ns
t_{PHL}	Propagation delay time, high-to-low-level output SCL_T/SDA_T to SCL_R/SDA_R				136	
t_{PLH}	Propagation delay time, low-to-high-level output SCL_T/SDA_T to SCL_R/SDA_R	Rbuffer : Rpu = 1.2K, Vpu = 3.3V or Rpu = 1.8K, Vpu = 5V IADJ = GND C_{LOAD} = 100 pF			450	
t_{PHL}	Propagation delay time, high-to-low-level output SCL_T/SDA_T to SCL_R/SDA_R				136	
t_r	SCL_T/SDA_T Output signal rise time	See Fig. A			999	
t_f	SCL_T/SDA_T Output signal fall time				90	
t_r	SCL_R/SDA_R Output signal rise time				999	
t_f	SCL_R/SDA_R Output signal fall time				90	
t_{set}	Enable to start condition			6	10	
t_{hold}	Enable after stop condition			6	10	

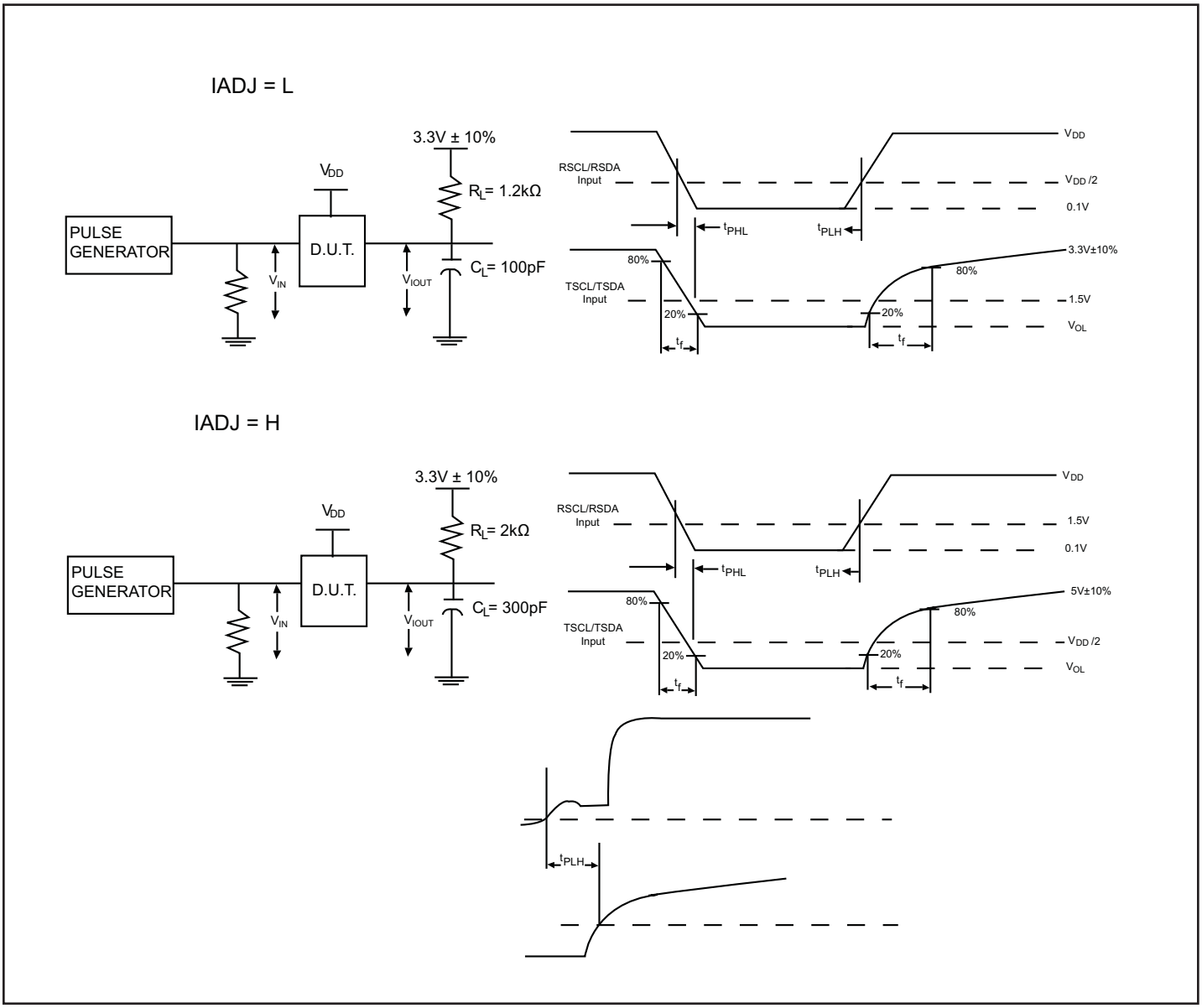
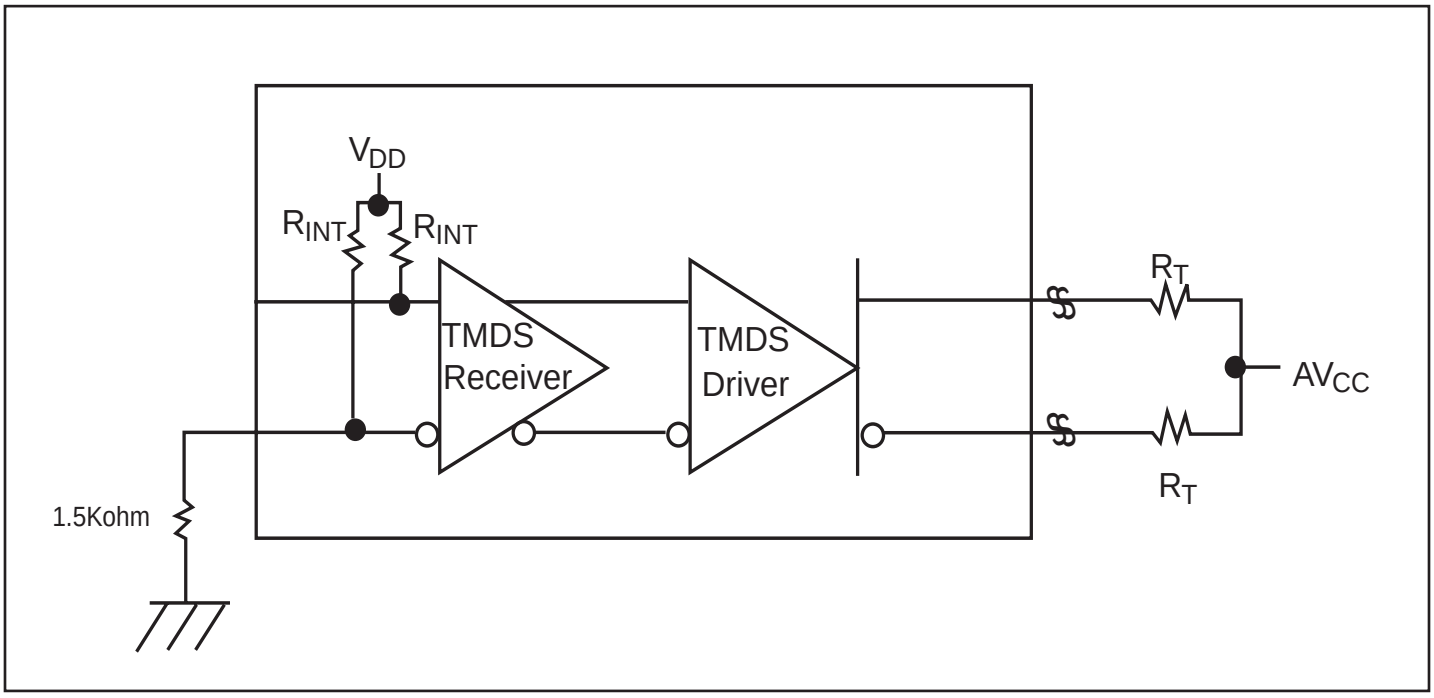


Figure A. I²C Timing Test Circuit and Definition

TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. One pin will be pulled high to V_{DD} with the other grounded through a 1.5K-ohm resistor as shown.



TMDS Input Fail-Safe Recommendation

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V_{DD} pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitors on each V_{DD} pins, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

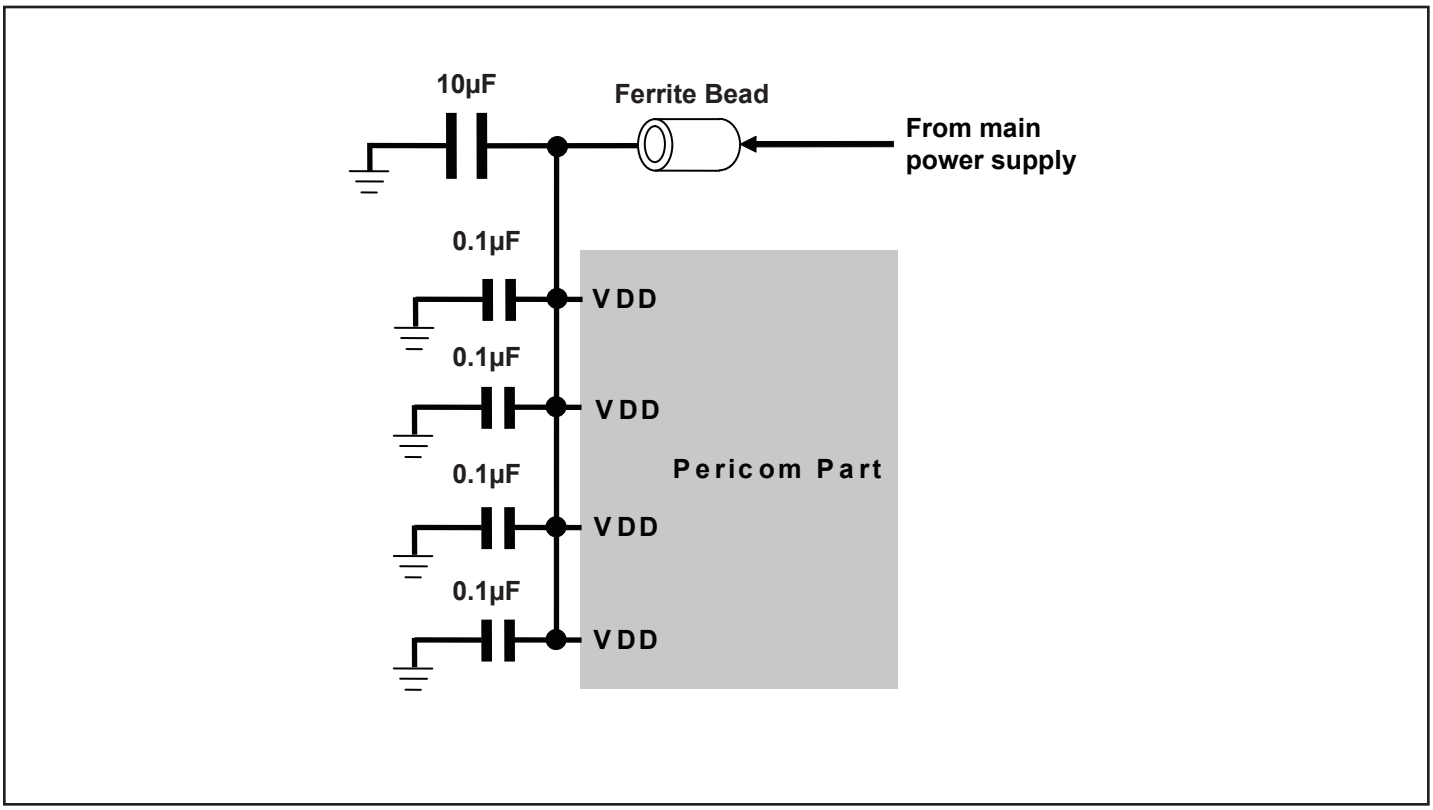


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling CapacitorPlacement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

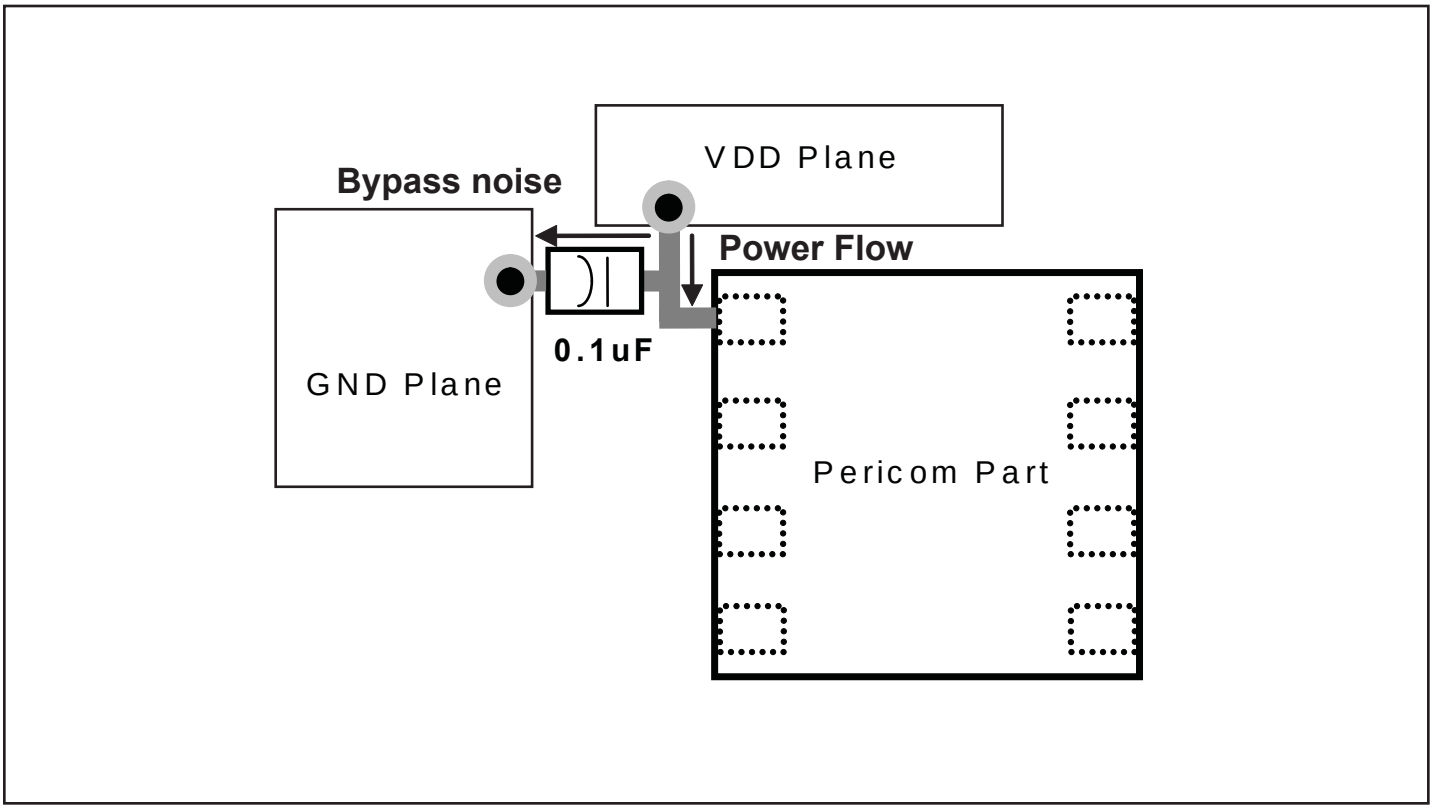


Figure 2 Layout and Decoupling Capacitor Placement Diagram

Application Information

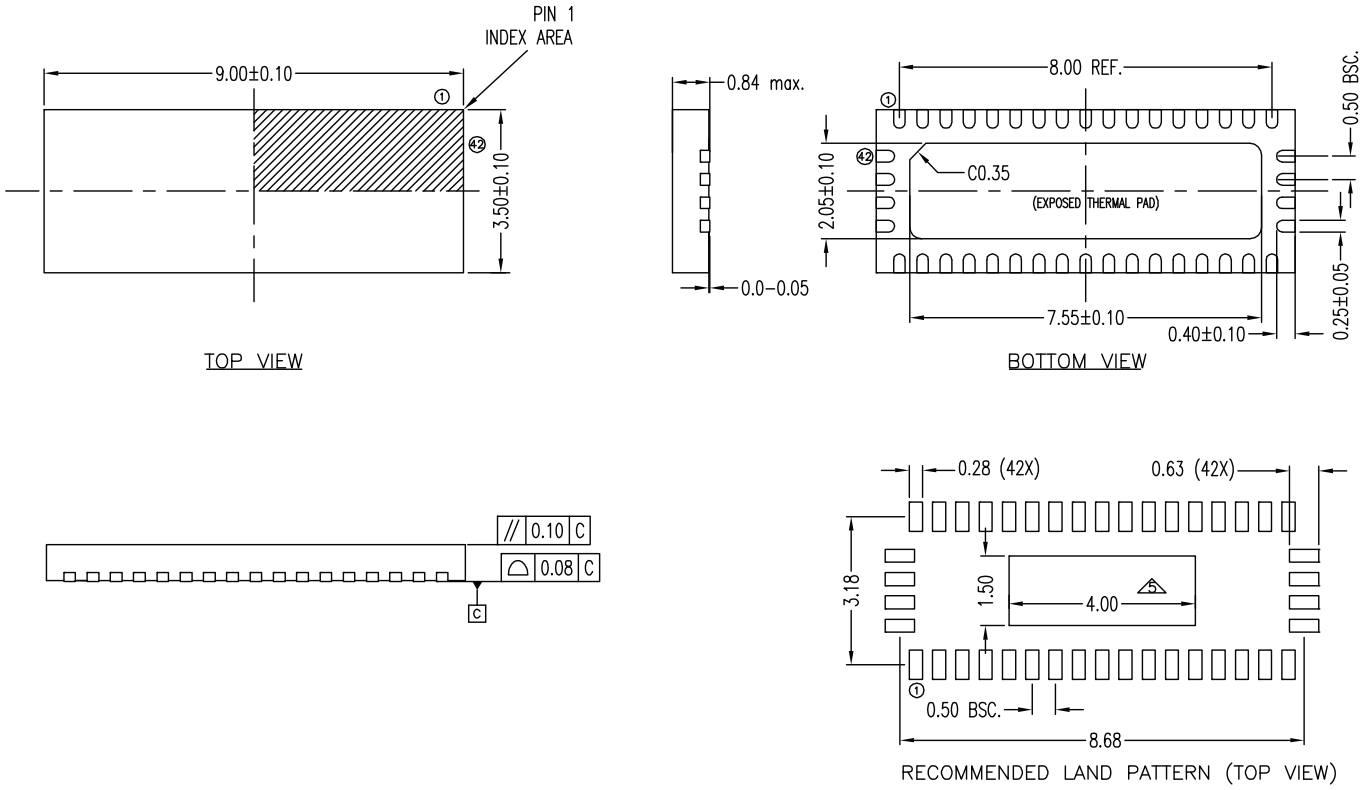
Supply Voltage

All V_{DD} pins are recommended to have a 0.01µF capacitor tied from V_{DD} to GND to filter supply noise

TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDM101 device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

Package Mechanical: 42-pin, Low Profile Quad Flat Package (ZH42)



Notes:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended Land Pattern is for reference only.
5. Thermal Pad Soldering Area

PERICOM Semiconductor Corporation — DATE: 02/17/09

DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 — REVISION: C

Note: 09-0116

• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI101ZHE	ZH	42-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel

单击下面可查看定价，库存，交付和生命周期等信息

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