A Product Line of
Diodes Incorporated

PI6C4911504-03

High Performance LVPECL Fanout Buffer

Features

- 4 LVPECL Outputs
- Up to 1.5GHz Output Frequency
- Ultra Low Additive Phase Jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two selectable inputs
- Low delay from input to output (Tpd typ. 1.5ns)
- 2.5V / 3.3V power supply
- Industrial temperature support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 20-pin, TSSOP (L)

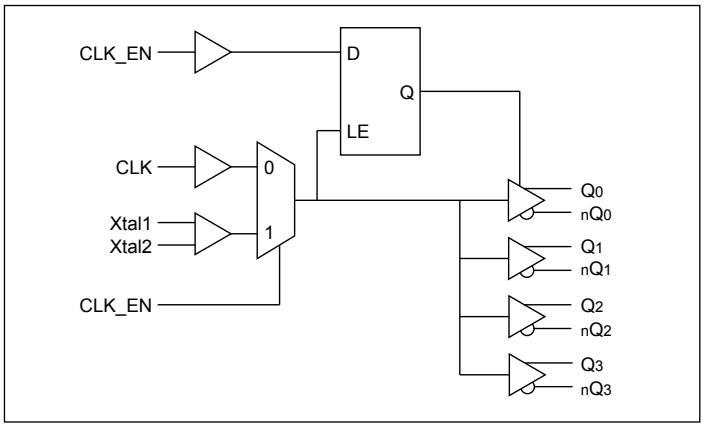
Description

The PI6C4911504-03 is a high performance fanout buffer device which supports up to 1.5GHz frequency. PI6C4911504-03 features selectable single-ended clock or crystal inputs and translates to four LVPECL outputs. The outputs are synchronized with input clock during asynchronous assertion /deassertion of CLK_EN pin. PI6C4911504-03 is ideal for crystal or LVCMOS/LVTTL to LVPECL translation. Typical clock translation and distribution applications are data-communications and telecommunications. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

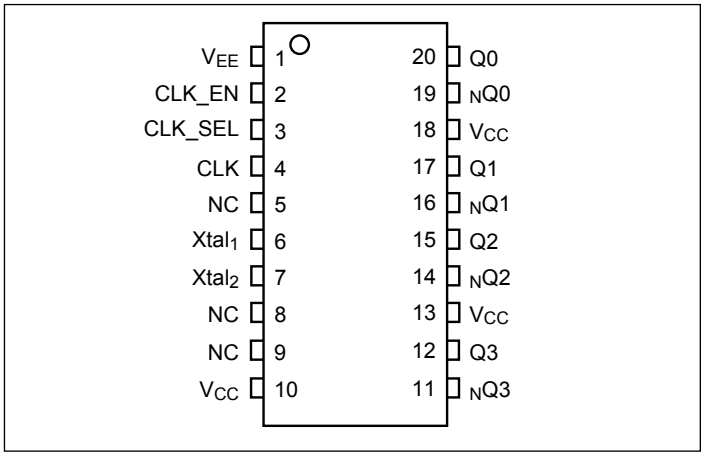
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	V_{EE}	Power		Negative power supply
2	CLK_EN	Input	Pullup	Clock output enable/ disable
3	CLK_SEL	Input	Pulldown	Clock input source selection pin
4	CLK	Input	Pulldown	Clock input
5	NC	-		No Connect
6	XTAL1	Input		Xtal input
7	XTAL2	Output		Xtal output
8, 9	NC	-		No connect
10, 13, 18	V_{CC}	Power		Power supply
11, 12	nQ3 Q3	Output		LVPECL output clock
14, 15	nQ2 Q2	Output		LVPECL output clock
16, 17	nQ1 Q1	Output		LVPECL output clock
19, 20	nQ0 Q0	Output		LVPECL output clock

Note: Pullup and Pulldown are for internal input resistors

Function Table

Table 1: Clock source input select function

CLK_SEL	Function
0	CLK is the selected reference input
1	XTAL is the selected input

Table 2: Clock output select function

CLK_EN	Function
0	All outputs disabled. Qx disabled low, nQx disabled High
1	All outputs enabled.

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential (VCC)..... -0.5 to +4.65V
Inputs (Referenced to GND) ..... -0.5 to Vcc+0.5V
Clock Output (Referenced to GND)..... -0.5 to Vcc+0.5V
Soldering Temperature (Max of 10 seconds) .....+260°C
Latch up 200mA
Junction Temperature .....Max. 125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		3.135		3.465	V
			2.375		2.625	V
I_{DD}	Power Supply Current	All outputs unloaded			130	mA
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		V_{CC}=3.3V	2.0		V_{CC}+0.3	V
V_{IL}	Input low voltage		V_{CC}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage		V_{CC}=2.5V	1.7		V_{CC}+0.3	V
V_{IL}	Input low voltage		V_{CC}=2.5V	-0.3		0.7	V
I_{IH}	Input High current	CLK, CLK_SEL				150	uA
		CLK_EN				10	uA
I_{IL}	Input Low current	CLK, CLK_SEL		-10			uA
		CLK_EN		-150			uA
C_{IN}	Input capacitance				4		pF
$R_{PULLUP/PULLDOWN}$	Input pullup and pulldown resistor				50		kΩ

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{CC}=3.3V	2.1		2.6	V
		V_{CC}=2.5V	1.3		1.75	
V_{OL}	Output Low voltage	V_{CC}=3.3V	1.0		1.8	V
		V_{CC}=2.5V	0.4		0.8	

AC Electrical Specifications – Differential Outputs

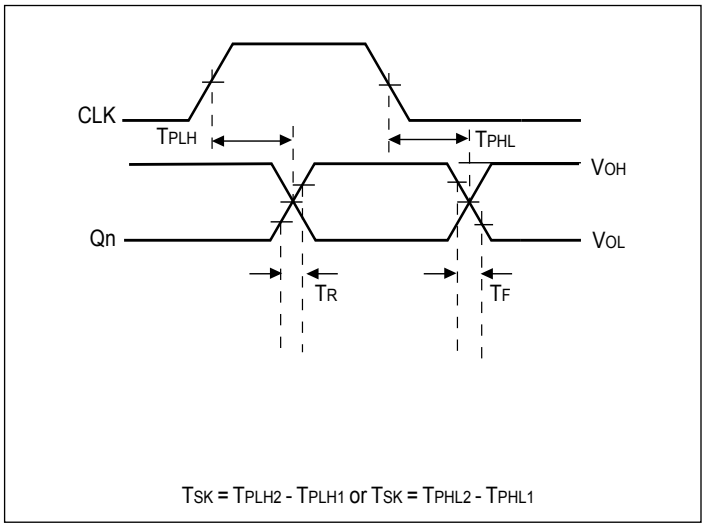
Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL			1500	MHz
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle		48		52	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
T_j	Buffer additive jitter RMS			0.03		ps
T_{SK}	Output Skew	4 outputs devices, outputs in same bank, with same load, at DUT.		25		ps
T_{PD}	Propagation Delay			1500		ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns

Notes:
All parameters are measured with CMOS input of 266MHz unless stated otherwise

Crystal Characteristics

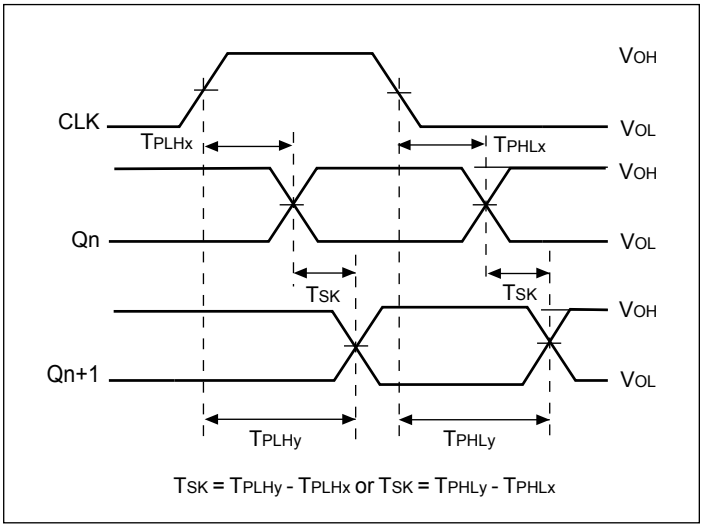
Parameters	Test Conditions	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency		12		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Propagation Delay



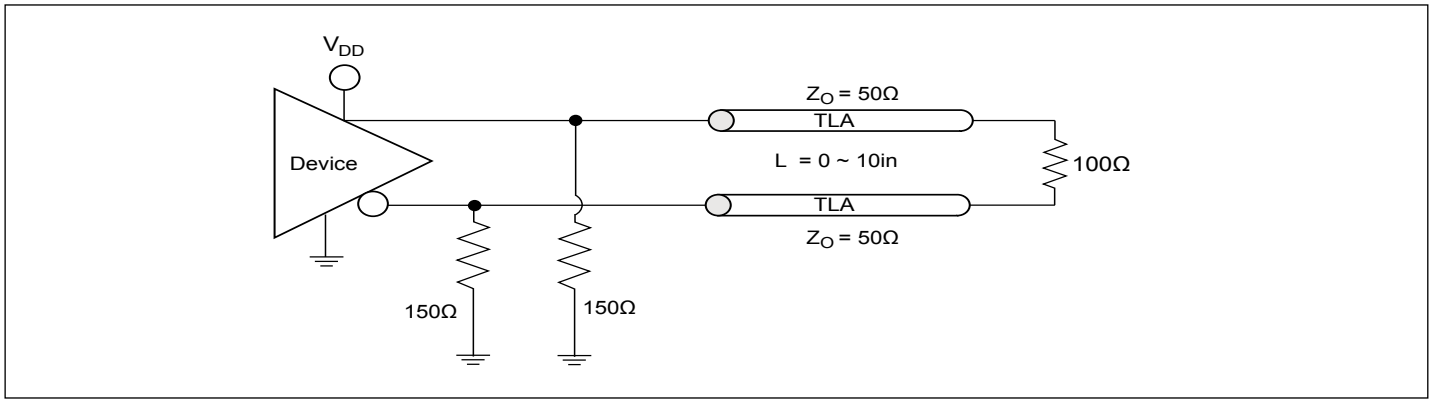
TSK = TPLH2 - TPLH1 or TSK = TPHL2 - TPHL1

Output Skew



TSK = TPLHy - TPLHx or TSK = TPHLy - TPHLx

Configuration Test Load Board Termination for LVPECL

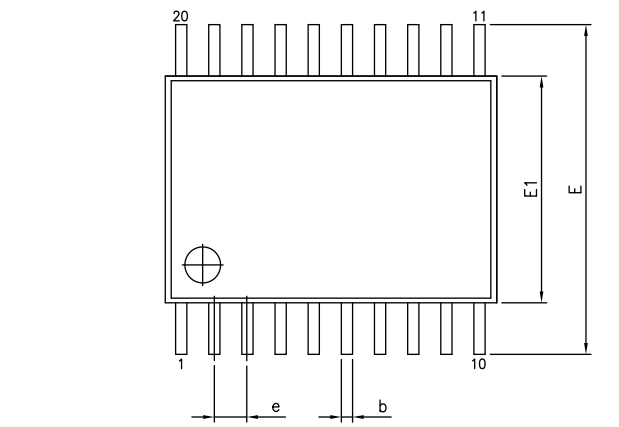


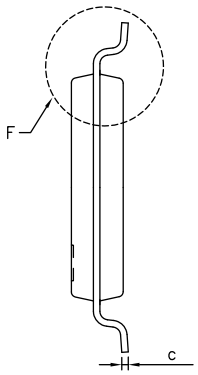
Part Marking

PI6C4911
504-03LIE
ZYYWWXX
○

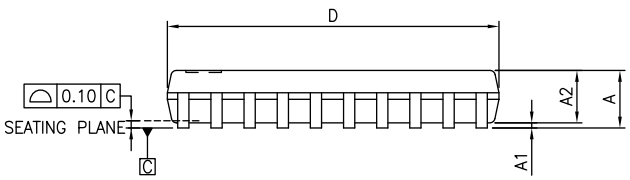
Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

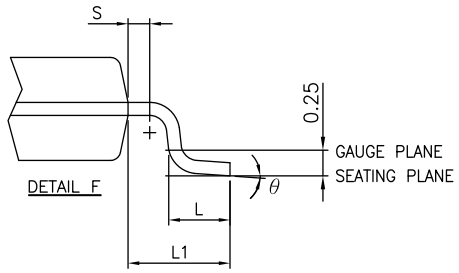
Packaging Mechanical: 20-TSSOP (L)





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/31/16

DESCRIPTION: 20-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L20)

DOCUMENT CONTROL #: PD-1311 REVISION: G

16-0074

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI6C4911504-03LIEX	L	20-Pin, 173mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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