

### Features

- Three differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 125MHz, 156.25MHz, 312.5MHz, 625MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.26ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.4ps (max)
- Full 3.3V or 2.5V supply modes
- Commercial and industrial ambient operating temperature
- Available in lead-free package: 28-TQFN

### Description

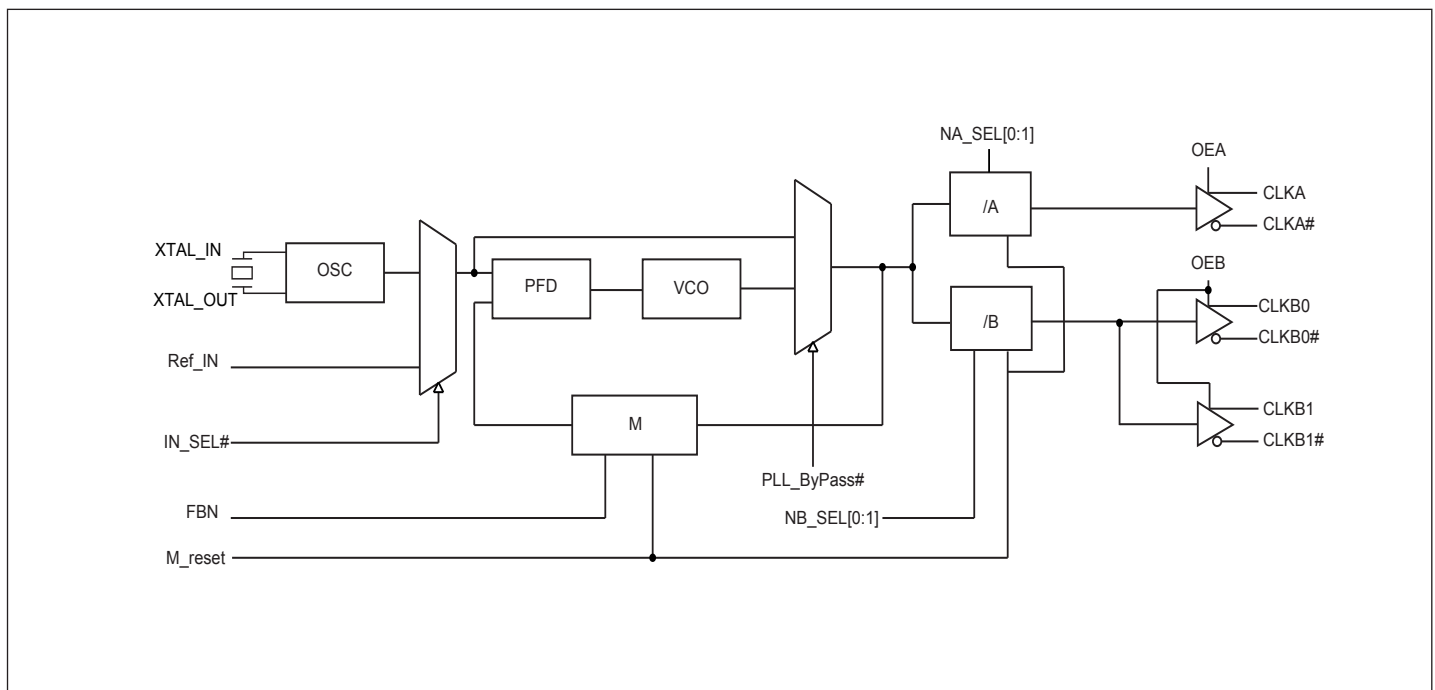
The PI6LC48P0301A is a 3-output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex™ family of high performance clock solutions. Using a 25MHz or other fundamental frequency crystal, the most popular Ethernet frequencies can be generated based on the settings of 4 frequency select pins.

The PI6LC48P0301A uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, so it is ideal for Ethernet interface in all kind of systems.

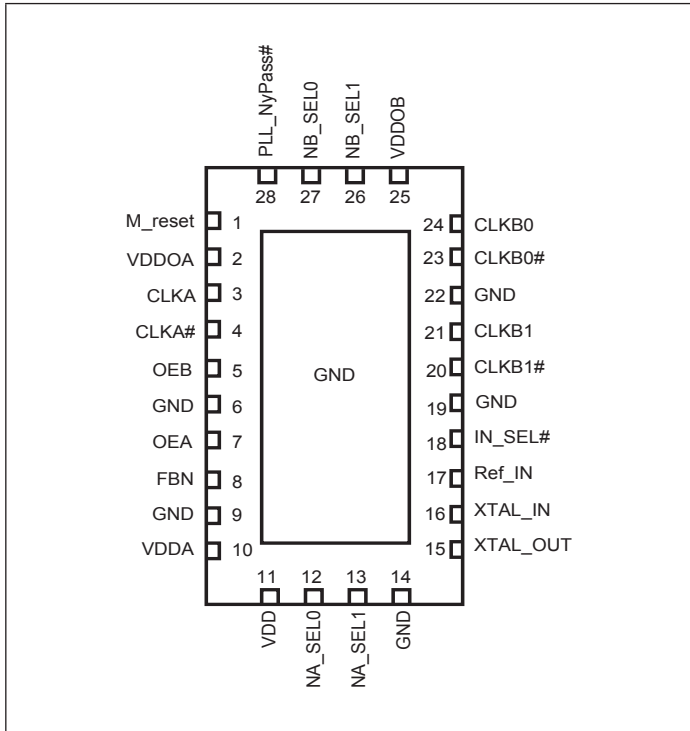
### Applications

- Networking systems

### Block Diagram



### Pin Configuration



### Pinout Table

Pin No.	Pin Name	I/O Type		Description
1	M_reset	Input	Pull-down	Master Reset. When HIGH, CLKx goes to “low” and CLKx# goes to “high”; When LOW outputs are enabled.
2	VDDOA	Power		Bank A Output Power Supply
3, 4	CLKA, CLKA#	Output		Bank A LVPECL Output Clock
5	OEB	Input	Pull-up	Bank B Output Enable. When LOW, output is differential low.
6, 9, 14, 19, 22	GND	Ground		Ground
7	OEA	Input	Pull-up	Bank A Output Enable. When LOW, output is differential low.
8	FBN	Input	Pull-down	Feedback Divider Select
10	VDDA	Power		Analog Power Supply
11	VDD	Power		Core Power Supply
12, 13	NA_SEL0, NA_SEL1	Input	Pull-up	Bank A Output Divider Select
15, 16	XTAL_OUT, XTAL_IN	Crystal		Crystal Input and Output
17	Ref_IN	Input	Pull-down	CMOS Reference Clock Input
18	IN_SEL#	Input	Pull-up	When HIGH, Crystal is selected; When LOW, reference input is selected.

Pin No.	Pin Name	I/O Type		Description
20, 21	CLKB1#, CLKB1	Output		Bank B LVPECL Output Clock 1
23, 24	CLKB0#, CLKB0	Output		Bank B LVPECL Output Clock 0
25	VDDOB	Power		Bank B Output Power Supply
26, 27	NB_SEL1, NB_SEL0	Input	Pull-up	Bank B Output Divider Select
28	PLL_ByPass#	Input	Pull-up	Active Low PLL Bypass

### Bank A Frequency Table

Input				Feedback Divider	Bank A Output Divider	CLKA/CLKA# Output Frequency (MHz)
Crystal Frequency (MHz)	FBN	NA_SEL1	NA_SEL0			
25	0	0	0	25	1	625
25	0	0	1	25	2	312.5
20	0	0	1	25	2	250
22.5	0	1	0	25	3	187.5
25	0	1	1	25	4	156.25
24	0	1	1	25	4	150
20	0	1	1	25	4	125
19.44	1	0	0	32	1	622.08
19.44	1	0	1	32	2	311.04
15.625	1	0	1	32	2	250
18.75	1	1	0	32	3	200
19.44	1	1	1	32	4	155.52
18.75	1	1	1	32	4	150
15.625	1	1	1	32	4	125

### Bank B Frequency Table

Input				Feedback Divider	Bank B Output Divider	CLKB0/CLKB0#, CLKB1/CLKB1# Output Frequency (MHz)
Crystal Frequency (MHz)	FBN	NB_SEL1	NB_SEL0			
25	0	0	0	25	2	312.5
20	0	0	0	25	2	250
25	0	0	1	25	4	156.25
24	0	0	1	25	4	150
20	0	0	1	25	4	125
25	0	1	0	25	5	125
25	0	1	1	25	8	78.125
24	0	1	1	25	8	75
20	0	1	1	25	8	62.5
19.44	1	0	0	32	2	311.04
15.625	1	0	0	32	2	250
19.44	1	0	1	32	4	155.52
18.75	1	0	1	32	4	150
15.625	1	0	1	32	4	125
15.625	1	1	0	32	5	100
19.44	1	1	1	32	8	77.76
18.75	1	1	1	32	8	75
15.625	1	1	1	32	8	62.5

### Typical Crystal Requirement

Parameter		Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency	FBN = 0	19.6		27.2	MHz
	FBN = 1	15.313		21.25	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

### Recommended Crystal Specification

Pericom recommends:

a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)

**Maximum Ratings** (Over operating free-air temperature range)

Storage Temperature.....	-65°C to +155°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
3.3V Analog Supply Voltage.....	-0.5 to +3.6V
ESD Protection (HBM) .....	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics**
**Power Supply DC Characteristics, ( $T_A = -40$  to  $85^\circ\text{C}$ )**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO\_A}$ $V_{DDO\_B}$	Output Supply Voltage		3.135	3.3	3.465	V
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{DDO\_A}$ $V_{DDO\_B}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{GND}$	Power Supply Current				150	mA
$I_{DDA}$	Analog Supply Current				37	mA

**LVC MOS/LVTTL DC Characteristics, ( $T_A = -40$  to  $85^\circ\text{C}$ )**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3\text{ V} \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5\text{ V} \pm 5\%$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3\text{ V} \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5\text{ V} \pm 5\%$	-0.3		0.7	V
$I_{IH}$	Input High Current	Ref_IN, FBN, M_reset $V_{DD} = V_{IN} = 3.465\text{V}$			150	$\mu\text{A}$
		OEA, OEB, PLL_By-pass#, IN_SEL#, NA_SEL[1:0], NB_SEL[1:0] $V_{DD} = V_{IN} = 3.465\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	Ref_IN, FBN, M_reset $V_{DD} = 3.465\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		OEA, OEB, PLL_By-pass#, IN_SEL#, NA_SEL[1:0], NB_SEL[1:0] $V_{DD} = 3.465\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$

LVPECL DC Characteristics, ( $T_A = -40$  to  $85^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Typ	Max	Units
V <sub>OH</sub>	Output High Voltage <sup>(1)</sup>	V <sub>DD</sub> = 3.3V	1.9		2.4	V
		V <sub>DD</sub> = 2.5V	1.1		1.6	
V <sub>OL</sub>	Output Low Voltage <sup>(1)</sup>	V <sub>DD</sub> = 3.3V	1.2		1.6	V
		V <sub>DD</sub> = 2.5V	0.4		0.8	

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

## AC Electrical Characteristics

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

AC Characteristics, ( $T_A = -40$  to  $85^\circ\text{C}$ )

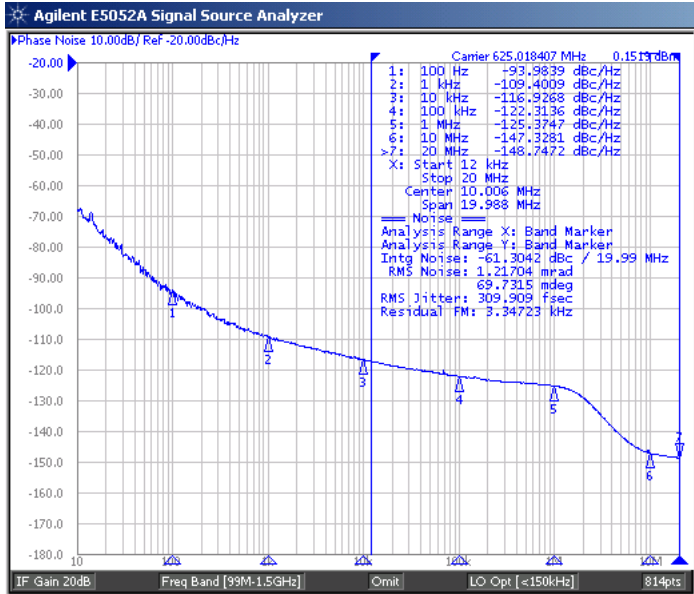
Symbol	Parameter	Condition	Min.	Typ.	Max	Units	
$f_{\text{OUT}}$	Output Frequency Range	Otuput Divider = $\div 1$	490		680	MHz	
		Otuput Divider = $\div 2$	245		340	MHz	
		Otuput Divider = $\div 3$	163.33		226.67	MHz	
		Otuput Divider = $\div 4$	122.5		170	MHz	
		Otuput Divider = $\div 5$	98		136	MHz	
		Otuput Divider = $\div 8$	61.25		85	MHz	
$t_{\text{sk}(b)}$	Bank Skew <sup>(1)</sup>				25	ps	
$t_{\text{sk}(o)}$	Output Skew <sup>(2,4)</sup>	Output @ Same Frequencies			70	ps	
		Output @ Different Frequencies			200	ps	
$t_{\text{jit}(\emptyset)}$	RMS Phase Jitter, (Random) <sup>(3)</sup>	625MHz, (1.875MHz - 20MHz)		0.14		ps	
		625MHz, (12kHz - 20MHz)		0.32	0.4	ps	
		312.5MHz, (1.875MHz - 20MHz)		0.15		ps	
		312.5MHz, (12kHz - 20MHz)		0.29	0.4	ps	
		156.25MHz, (1.875MHz - 20MHz)		0.14		ps	
		156.25MHz, (12kHz - 20MHz)		0.26	0.4	ps	
		125MHz, (1.875MHz - 20MHz)		0.17		ps	
		125MHz, (12kHz - 20MHz)		0.29	0.4	ps	
$t_R / t_F$	Output Rise/Fall Time	20% to 80%			400	ps	
$\theta_{\text{DC}}$	Output Duty Cycle	Measured at the differential cross point	Otuput Divider = $\div 1$	47		53	%
			Other divider values	47		53	%

**Note:**

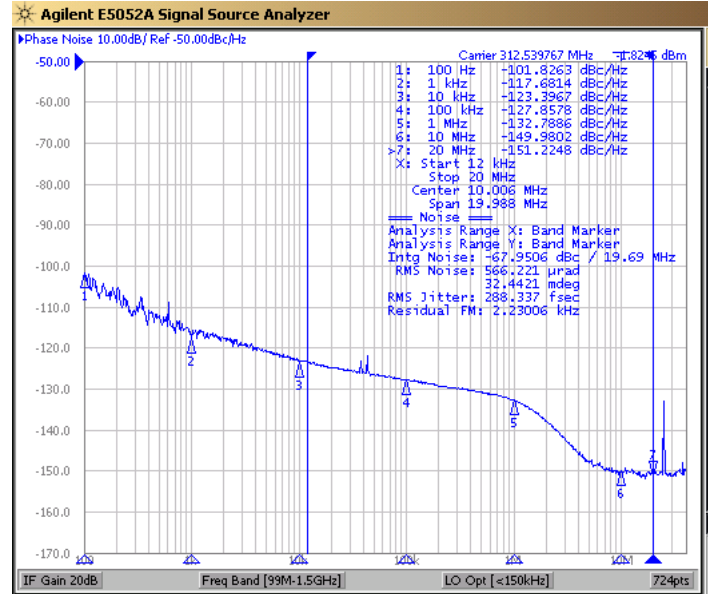
1. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
3. Please refer to the Phase Noise Plots.
4. This parameter is defined in accordance with JEDEC Standard 65.

**Phase Noise Plots**

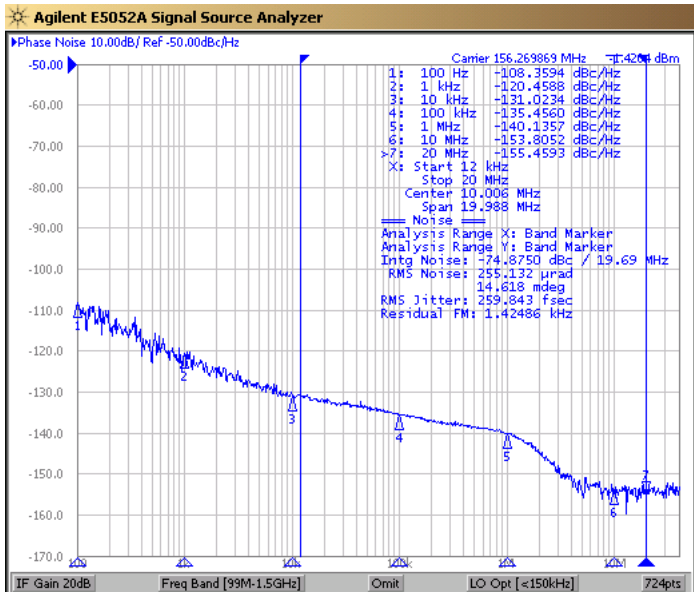
$f_{OUT} = 625\text{MHz}$



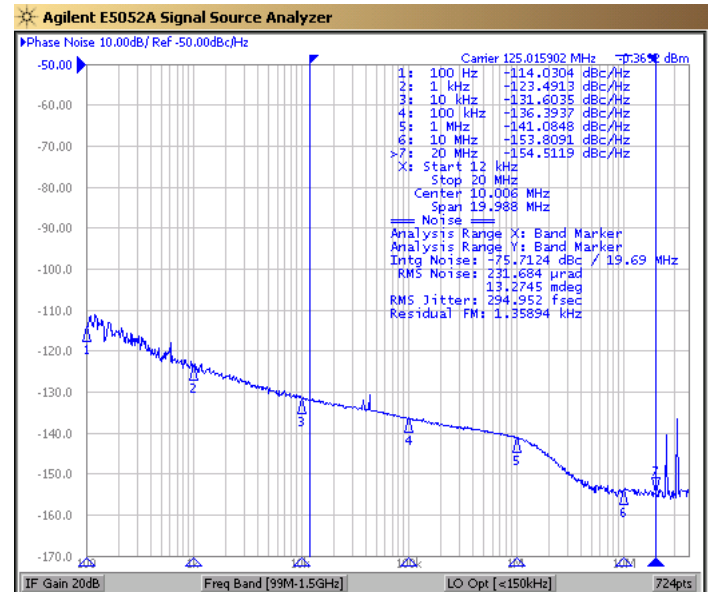
$f_{OUT} = 312.5\text{MHz}$



$f_{OUT} = 156.25\text{MHz}$

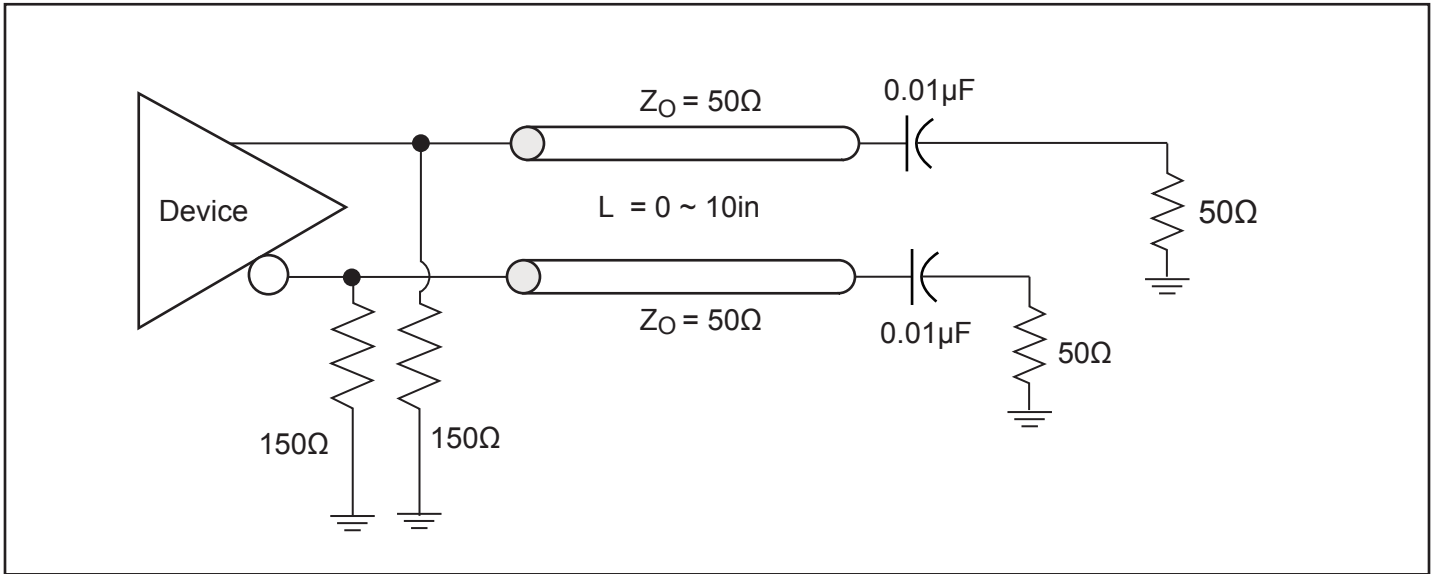


$f_{OUT} = 125\text{MHz}$



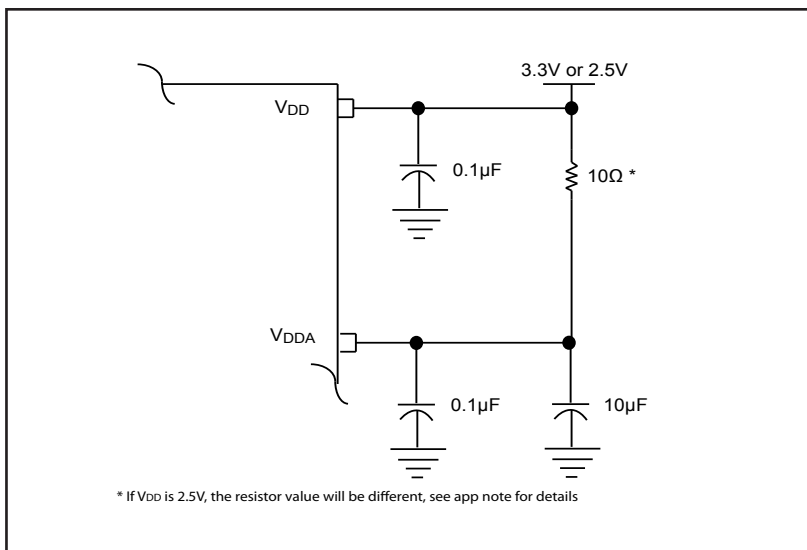


**LVPECL Test Circuit**



**Power Supply Filtering Techniques**

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P0301A provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and 0.1μF bypass capacitors should be used for each pin. Figure below illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional 10Ω resistor along with a 10μF bypass capacitor be connected to the  $V_{DDA}$  pin.



## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. A 1kΩ resistor can be tied from XTAL\_IN to ground for additional protection.

#### Ref\_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref\_IN to ground can provide additional protection.

#### LVC MOS Control Pins:

All control pins have internal pulldowns/pullups; A 1kΩ resistor tied from internal pulldown control pins to ground, and a 4.7kΩ tied from internal pullup control pins to power supply can provide additional protection.

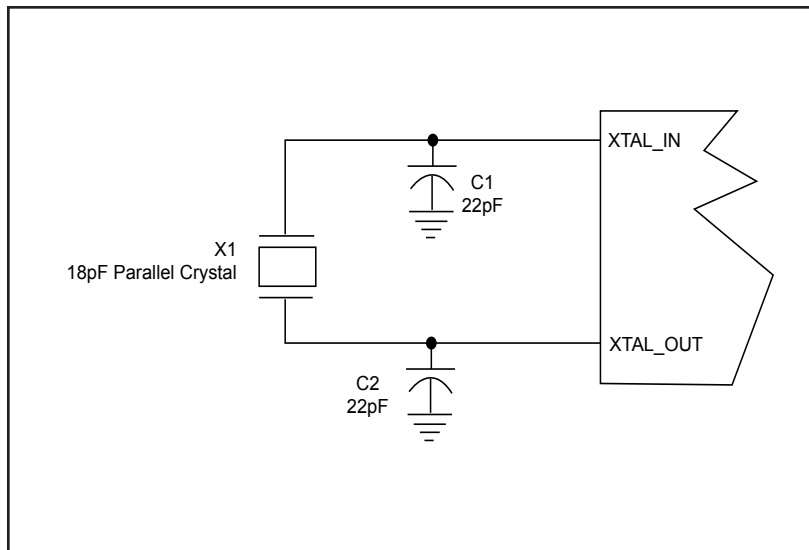
### Outputs:

#### LVPECL Outputs:

All unused LVPECL outputs can be left floating.

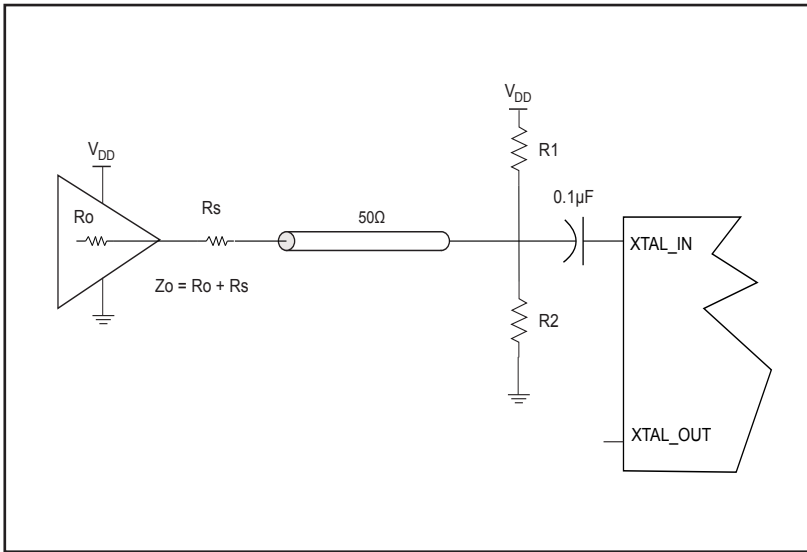
## Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



**LVCMOS to XTAL Interface**

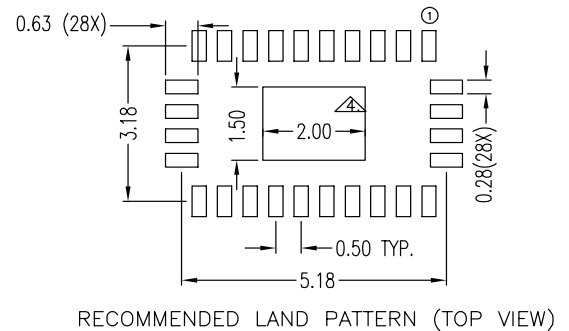
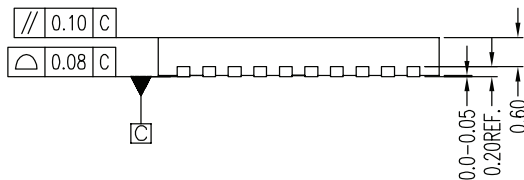
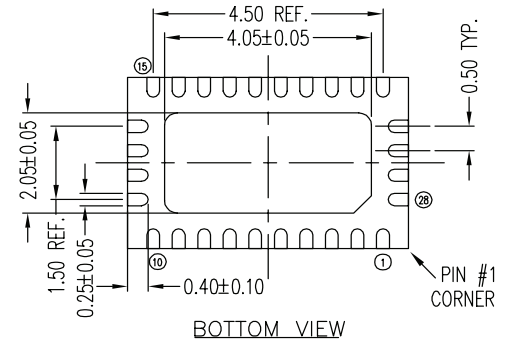
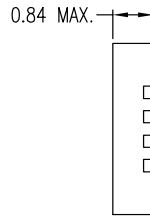
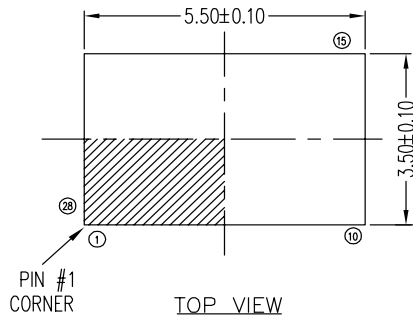
The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Thermal Information**

Symbol	Description	Condition	
$\Theta_{JA}$	Junction-to-ambient thermal resistance	Still air	41.68 °C/W
$\Theta_{JC}$	Junction-to-case thermal resistance		23.78 °C/W

### Packaging Mechanical: 28-Contact TQFN (ZH)



**NOTE :**

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
4. THERMAL PAD SOLDERING AREA

### Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P0301AZHE	ZH	Pb-free & Green, 28-pin TQFN	Commercial
PI6LC48P0301AZHIE	ZH	Pb-free & Green, 28-pin TQFN	Industrial

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

单击下面可查看定价，库存，交付和生命周期等信息

[>>Diodes Incorporated\(达达科技\(美台\)\)](#)