

Low Power High Integration Clock Generator

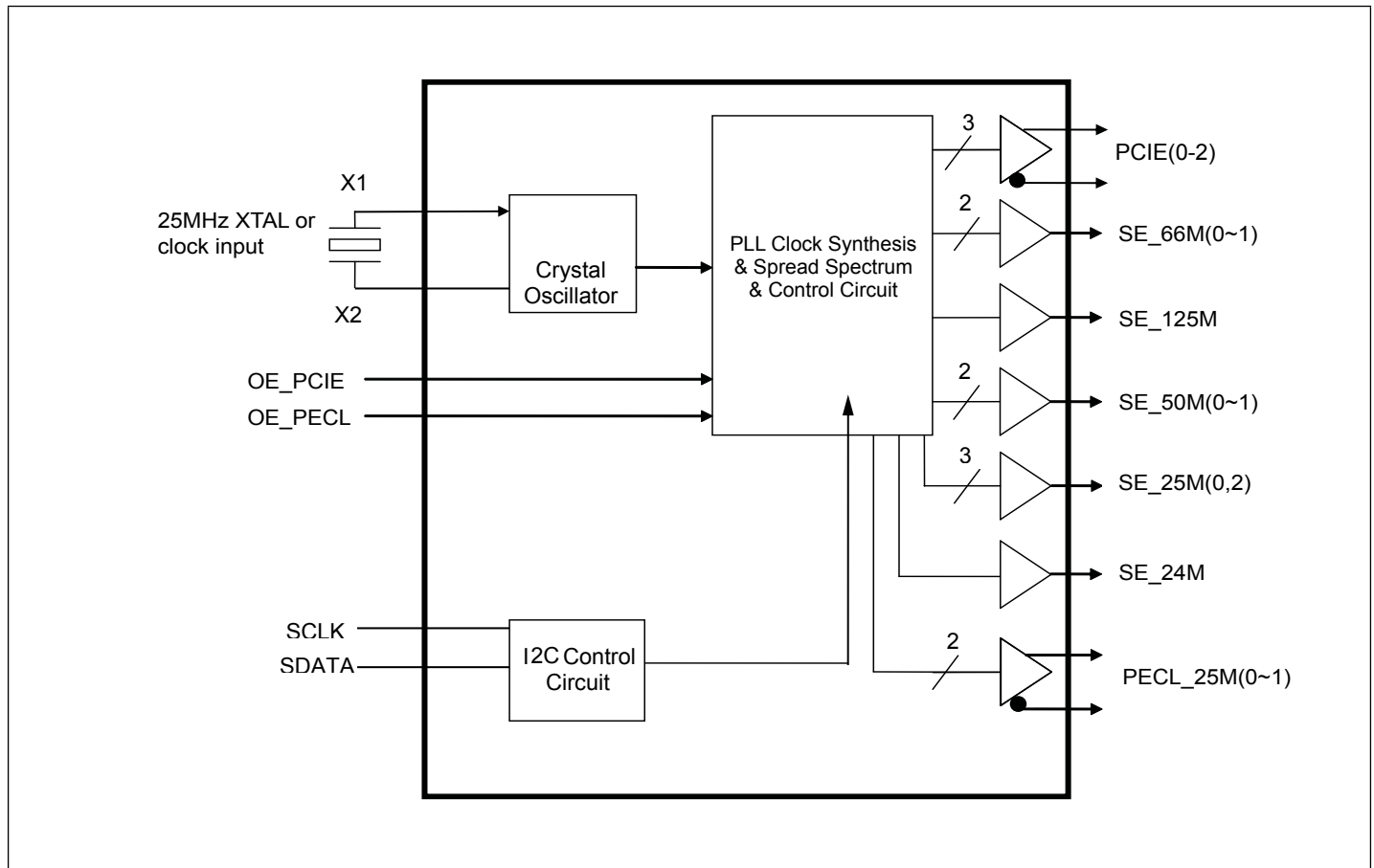
Features

- 3.3V supply voltage
- 25MHz XTAL or reference clock input
- Output
 - 3 x low power PCIe 2.0 100MHz clock with spread spectrum support and integrate series termination resistor
 - 2 x 66.667MHz LVCMOS clock for CPU
 - 1 x 125MHz LVCMOS clock for Gigabit Ethernet
 - 2 x 50MHz LVCMOS clock for CPLD
 - 3 x 25MHz LVCMOS clock for Ethernet PHY
 - 2 x 25MHz low jitter LVPECL Ethernet clock
 - 1 x 24MHz LVCMOS for USB PHY
- Packaging (Pb free and Green)
 - 48-pin TQFN

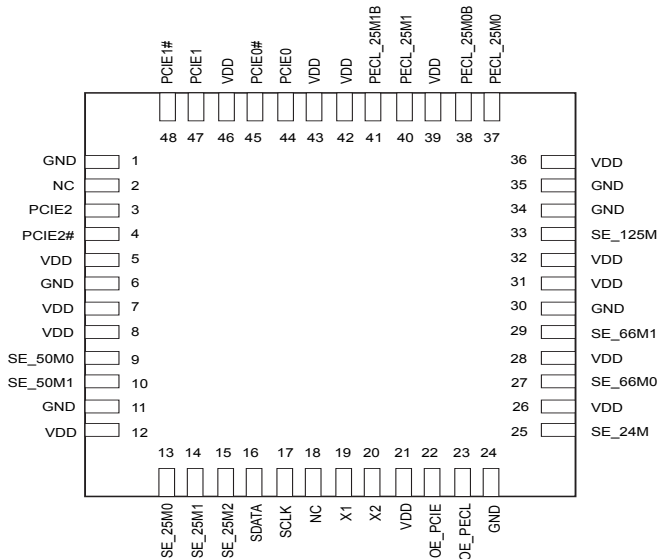
Description

The new PI6C49021 is a high integration clock generator intended for all kinds of embedded applications and networking application with PCIe interface. The device is the most cost effective way to generate multi-frequencies and multi-outputs clocks from a 25MHz crystal and reference clock. The device can generate 100MHz HCSL clock, single-ended clocks includes 24MHz, 25MHz, 50MHz, 125MHz, and low jitter 25MHz LVPECL clock.

Block Diagram



Pin Configuration



| Pins | Group Description |
|--------|--------------------------------------|
| 5 | Power for 66.667MHz PLL |
| 7 | Power for 24MHz PLL |
| 31 | Power for 125M/50MHz PLL |
| 36 | Power for 100MHz PCIe PLL |
| 8 | Power for 50MHz outputs |
| 12 | Power for 25MHz LVCMOS outputs |
| 21 | Power for crystal oscillator |
| 26 | Power for 24MHz output |
| 28 | Power for 66.667MHz outputs |
| 32 | Power for 125MHz output |
| 39, 42 | Power for 25MHz differential outputs |
| 43, 46 | Power for PCIe clock outputs |

Pin Description

| Pin# | Pin Name | Pin Type | Pin Description |
|---|----------|----------|---|
| 1, 6, 11, 24, 30, 34, 35 | GND | Power | Ground |
| 2 | NC | | Do not Connect |
| 3 | PCIE2 | Output | 100MHz HCSL output |
| 4 | PCIE2# | Output | 100MHz HCSL output |
| 5, 7, 8, 12, 21, 26, 28, 31, 32, 36, 39, 42, 43, 46 | VDD | Power | Power supply |
| 9 | SE_50M0 | Output | 50MHz LVCMOS output |
| 10 | SE_50M1 | Output | 50MHz LVCMOS output |
| 13 | SE_25M0 | Output | 25MHz LVCMOS output |
| 14 | SE_25M1 | Output | 25MHz LVCMOS output |
| 15 | SE_25M2 | Output | 25MHz LVCMOS output |
| 16 | SDATA | I/O | I2C compatible data |
| 17 | SCLK | Input | I2C compatible clock |
| 18 | NC | | Do not Connect (can be used as RESET# pin, global reset input powers down PLLs plus tri-states outputs and sets the I2C tables to their default state when pulled low.) |
| 19 | X1 | Input | Crystal input. Connect to 25MHz Fundamental mode crystal or clock. |
| 20 | X2 | Output | Crystal output. Connect to 25MHz Fundamental mode crystal. Float for clock input. |

Pin List

| Pin# | Pin Name | Pin Type | Pin Description |
|------|------------|----------|--|
| 22 | OE_PCIE | Input | 100MHz HCSL PCIE2 enable pin. Set High to enable. |
| 23 | OE_PECL | Input | 25MHz LVPECL PECL 25M1 enable pin. Set High to enable. |
| 25 | SE_24M | Output | 24MHz LVCMOS output |
| 27 | SE_66M0 | Output | 66.667MHz LVCMOS output |
| 29 | SE_66M1 | Output | 66.667MHz LVCMOS output |
| 33 | SE_125M | Output | 125MHz LVCMOS output |
| 37 | PECL_25M0 | Output | 25MHz differential output |
| 38 | PECL_25M0# | Output | 25MHz differential output |
| 40 | PECL_25M1 | Output | 25MHz differential output |
| 41 | PECL_25M1# | Output | 25MHz differential output |
| 44 | PCIE0 | Output | 100MHz HCSL output |
| 45 | PCIE0# | Output | 100MHz HCSL output |
| 47 | PCIE1 | Output | 100MHz HCSL output |
| 48 | PCIE1# | Output | 100MHz HCSL output |

Notes: VDD and GND Pins Layout Guide

1. Small value decoupling caps. (0.1uF, 1uF, and 2.2uF) should be placed close each VDD pin or its via
2. Connect all GND pins to package thermal pad which must be connected to the GND plane for better thermal distribution and signal conducting with reasonable via count (>8)

Selection Table – Spread Spectrum

| SS1 | SS0 | SSC |
|-----|-----|-------------|
| 0 | 0 | No spread |
| 0 | 1 | Down -0.75% |
| 1 | 0 | Down -0.5% |
| 1 | 1 | No spread |

Selection Table – PCIE2 / PECL_25M1 Output Control

| OE_PCIE | PCIE2 Status |
|---------|------------------------------------|
| 1 | Enable PCIE2 output (Default) |
| 0 | Disable PCIE2 output, Tristate |
| OE_PECL | PECL_25M1 Status |
| 1 | Enable PECL_25M1 output (Default) |
| 0 | Disable PECL_25M1 output, Tristate |

Serial Data Interface (SMBus)

PI6C49021 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|----|----|-----|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0/1 |

How to Write

| 1 bit | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | | 8 bits | 1 | 1 bit |
|-----------|--------|-----|-----------------|-----|----------------|-----|-------------|-----|-----|-----------------|-----|----------|
| Start bit | D2H | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack | ... | Data Byte N - 1 | Ack | Stop bit |

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

| 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | ... | 8 bits | 1 bit | 1 bit |
|--------------|---------------|--------------|---------------------------------------|--------------|--------------|---------------|--------------|---|--------------|-------------------------------|--------------|-----|--------------------------|--------------------|-------------|
| M: Start bit | M: Send "D2h" | S: sends Ack | M: send starting databyte location: N | S: sends Ack | M: Start bit | M: Send "D3h" | S: sends Ack | S: sends # of data bytes that will be sent: X | M: sends Ack | S: sends starting data byte N | M: sends Ack | ... | S: sends data byte N+X-1 | M: Not Acknowledge | M: Stop bit |

Byte 0: Spread Spectrum Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|-----|---|------|--------------------|--------------------|--|
| 7 | OE for SE_66M0 | RW | 1 | SE_66M0 output | 0 = disabled 1 = enabled |
| 6 | Enable hardware or software control of OE bits (see Byte 0-Bit 6 and Bit 5 Functionality table) | RW | 0 | All outputs | 0 = hardware cntl 1 = software ctrl |
| 5 | Software RESET# bit. Enable or disables all outputs. (see Byte 0-Bit 6 and Bit 5 Functionality table) | RW | 1 | All outputs | 0 = disabled 1 = enabled |
| 4 | Reserved | R | Undefined | Not applicable | |
| 3 | Reserved | R | Undefined | | |
| 2 | Reserved | R | Undefined | | |
| 1 | Reserved | R | Undefined | | |
| 0 | OE for SE_66M1 | RW | 1 | SE_66M1 output | 0 = disabled 1 = enabled |

Byte 0: Bit 6 and Bit 5 Functionality

| Bit | Bit 5 | Description |
|-----|-------|--|
| 0 | X | RESET# = "H" will enable all outputs; SMBus can not control each output. |
| 1 | 0 | Disable all outputs and tri-states the outputs. When pin 18 (RESET#) is set low, force device to power-on reset and set all registers to default values. |
| 1 | 1 | Enable outputs according to the SMBus default values; SMBus can control each output. When pin 18 (RESET#) is set low, force to power-on reset and set all registers to default values. |

Byte 1: Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|-----|---|------|--------------------|-------------------------------------|---|
| 7 | OE for SE_125M | RW | 1 | SE_125M | 0 = disabled 1 = enabled |
| 6 | OE for SE_50M0 | RW | 1 | SE_50M0 | 0 = disabled 1 = enabled |
| 5 | OE for SE_50M1 | RW | 1 | SE_50M1 | 0 = disabled 1 = enabled |
| 4 | OE for SE_25M0 | RW | 1 | SE_25M0 | 0 = disabled 1 = enabled |
| 3 | OE for SE_25M1 | RW | 1 | SE_25M1 | 0 = disabled 1 = enabled |
| 2 | OE for SE_24M | RW | 1 | SE_24M | 0 = disabled 1 = enabled |
| 1 | Spread Spectrum Selection for 100MHz HCSL PCI Express clocks Bit 1: SS1, Bit 0:SS0 | RW | 0 | All 100MHz HCSL PCI Express outputs | See Selection Table 2 - Spread Spectrum |
| 0 | | RW | 0 | | |

Byte 2: Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|--------|-------------|------|--------------------|--------------------|-------|
| 7 to 0 | Reserved | R | Undefined | Not Applicable | |

Byte 3: Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|-----|------------------|------|--------------------|--------------------|-----------------------------|
| 7 | Reserved | RW | Undefined | Not Applicable | |
| 6 | OE for PECL_25M0 | RW | 1 | PECL_25M0 | 0 = disabled 1 = enabled |
| 5 | OE for PECL_25M1 | RW | 1 | PECL_25M1 | 0 = disabled 1 = enabled |
| 4 | OE for SE_25M2 | RW | 1 | SE_25M2 | 0 = disabled 1 = enabled |
| 3 | OE for PCIE2 | RW | 1 | PCIE2 | 0 = disabled 1 = enabled |
| 2 | OE for PCIE1 | RW | 1 | PCIE1 | 0 = disabled 1 = enabled |
| 1 | OE for PCIE0 | RW | 1 | PCIE0 | 0 = disabled 1 = enabled |
| 0 | Reserved | R | Undefined | Not Applicable | |

Byte 4 & 5: Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|--------|-------------|------|--------------------|--------------------|-------|
| 7 to 0 | Reserved | R | Undefined | Not Applicable | |

Byte 6: Control Register

| Bit | Description | Type | Power Up Condition | Output(s) Affected | Notes |
|-----|-------------------|------|--------------------|--------------------|-------|
| 7 | Revision ID bit 3 | R | 0 | Not Applicable | |
| 6 | Revision ID bit 2 | R | 0 | Not Applicable | |
| 5 | Revision ID bit 1 | R | 0 | Not Applicable | |
| 4 | Revision ID bit 0 | R | 0 | Not Applicable | |
| 3 | Vendor ID bit 3 | R | 0 | Not Applicable | |
| 2 | Vendor ID bit 2 | R | 0 | Not Applicable | |
| 1 | Vendor ID bit 1 | R | 1 | Not Applicable | |
| 0 | Vendor ID bit 0 | R | 1 | Not Applicable | |

Recommended Operation Conditions¹ (Over operating free-air temperature range)

| Symbol | Parameters | Min. | Max. | Units |
|------------------|---------------------|-------|-------|-------|
| V _{DD} | Supply Voltage | 3.135 | 3.465 | V |
| T _s | Storage Temperature | -65 | 150 | °C |
| V _{ESD} | ESD Protection | 2000 | | V |

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|---|--------------------------------|
| Maximum Supply Voltage, V _{DD} | 7V |
| All Inputs and Outputs | -0.5V to V _{DD} +0.5V |
| Ambient Operating Temperature..... | -40°C to +85°C |
| Storage Temperature..... | -65°C to +150°C |
| Junction Temperature | 125°C |
| Peak Soldering Temperature..... | 260°C |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Unless otherwise specified, V_{DD} = 3.3V ± 5%, Ambient Temperature -40°C to +85°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--------------------------|-----------------|----------------|--------------------|-----|-----------------------|-------|
| Operating Supply Voltage | V _{DD} | | 3.135 | | 3.465 | V |
| Input High Voltage | V _{IH} | | 2 | | V _{DD} + 0.3 | |
| Input Low Voltage | V _{IL} | | -0.3 | | 0.8 | |
| Input High Voltage | V _{IH} | SCLK,SDATA | 0.7V _{DD} | | V _{DD} | |
| Input Low Voltage | V _{IL} | SCLK,SDATA | | | 0.3V _{DD} | |
| Operating Supply Current | I _{DD} | | | 197 | 230 | mA |
| Input Capacitance | C _{IN} | All input pins | | 6 | | pF |

Electrical Characteristics - Single-Ended

Unless otherwise specified, $V_{DD}=3.3V\pm 5\%$, Ambient Temperature $-40^{\circ}C$ to $+85^{\circ}C$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|------------|--|---------|-----|-----------|-------|
| Input Clock Frequency | F_{IN} | | | 25 | | MHz |
| Frequency Stability | F_T | 25MHz XTAL | | | ± 50 | ppm |
| Frequency Synthesis Error | Ferror | 24MHz, 25MHz, 50MHz, 66.667MHz, 125MHz output | | | 0 | ppm |
| SCLK Frequency | | | | 100 | 400 | kHz |
| Output Rise/Fall Time | t_r, t_f | 20% to 80% 24MHz, 25MHz, 50MHz, 66.667MHz output | | 1 | 1.5 | ns |
| | | 0.6V to 2.7V 125MHz output | | | 1.2 | ns |
| Output Clock Duty Cycle | | Measured at $V_{DD}/2$ 24MHz, 25MHz, 50MHz, 66.667MHz output | 45 | 50 | 55 | % |
| | | Measured at $V_{DD}/2$, 125MHz | 47 | 50 | 53 | |
| High-Level Output Voltage | V_{OH} | $I_{OH} = -4mA$ | VDD-0.4 | | | V |
| High-Level Output Voltage | V_{OH} | $I_{OH} = -8mA$ | 2.4 | | | |
| Low-Level Output Voltage | V_{OL} | $I_{OL} = 8mA$ | | | 0.4 | |
| RMS phase jitter | | 25MHz clock output, Fj=1kHz to 5MHz offset frequency | | | 3 | ps |
| Peak-to-Peak Jitter | | 125MHz clock output | | | ± 150 | ps |
| | | 66.667MHz clock output | | | ± 150 | |
| | | 50MHz clock output | | | 250 | |
| Clock Stabilization Time from Power Up | | | 3 | | 6 | ms |

Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified, $V_{DD}=3.3V\pm 5\%$, Ambient Temperature $-40^{\circ}C$ to $+85^{\circ}C$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|--------------------|--------------------------------------|-------|------|--------|-------|
| Output Frequency | | | | | 100 | MHz |
| Cycle-to-Cycle Jitter | $T_{CC/Jitter}$ | | | | 150 | ps |
| Peak-to-Peak Phase Jitter | | Using PCIe jitter measurement method | | | 86 | |
| PCIe 2.0 RMS Phase Jitter | $J_{RMS2.0}$ | PCIe 2.0 Test Method @ 100MHz Output | | | 3.1 | ps |
| Spread Modulation Percentage | | | | -0.5 | 0 | % |
| Spread Modulation Frequency | | | | 32 | | kHz |
| Duty Cycle | T_{DC} | | 45 | 50 | 55 | % |
| Rising Edge Rate | | Note 3, 4 | 0.6 | | 4.0 | V/ns |
| Falling Edge Rate | | Note 3, 4 | 0.6 | | 4.0 | V/ns |
| Output Skew | T_{OSKEW} | $V_T = 50\%$ (measurement threshold) | | | 75 | ps |
| High-Level Output Voltage | V_{OH} | Note 2, ($R_s=33\text{-Ohm}$) | 0.65 | 0.71 | 0.85 | V |
| Low-Level Output Voltage | V_{OL} | | -0.20 | 0 | 0.05 | |
| Absolute Crossing Point Voltage | V_{CROSS} | Note 2, 5, 6 | 0.25 | | 0.55 | V |
| Variation of VCROSS over all rising clock edges | $V_{CROSS\ Delta}$ | Note 2, 5, 8 | | | 140 | mV |
| Average Clock Period Accuracy | $T_{PERIOD\ AVG}$ | Note 3, 9, 10 | -300 | | 2800 | ppm |
| Absolute Period (including jitter and spread spectrum) | $T_{PERIOD\ ABS}$ | Note 3, 7 | 9.847 | | 10.203 | ns |

Notes:

1. Measured at the end of an 8-inch trace with a 5pF load.
2. Measurement taken from a single-ended waveform.
3. Measurement taken from a differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M-.

Notes (Continued)

- 6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
 Refers to all crossing points for this measurement.
- 7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
- 8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M-.
- 9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
- 10. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100Hz/PPM * 300 PPM = 30 kHz. The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than ±300 ppm. With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

Electrical Characteristics - 25MHz LVPECL outputs

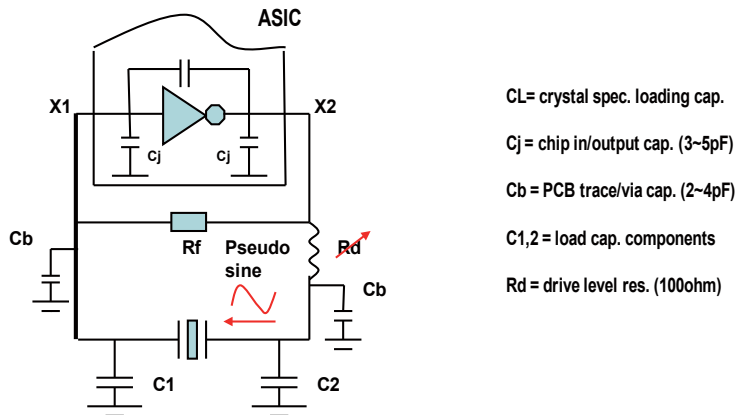
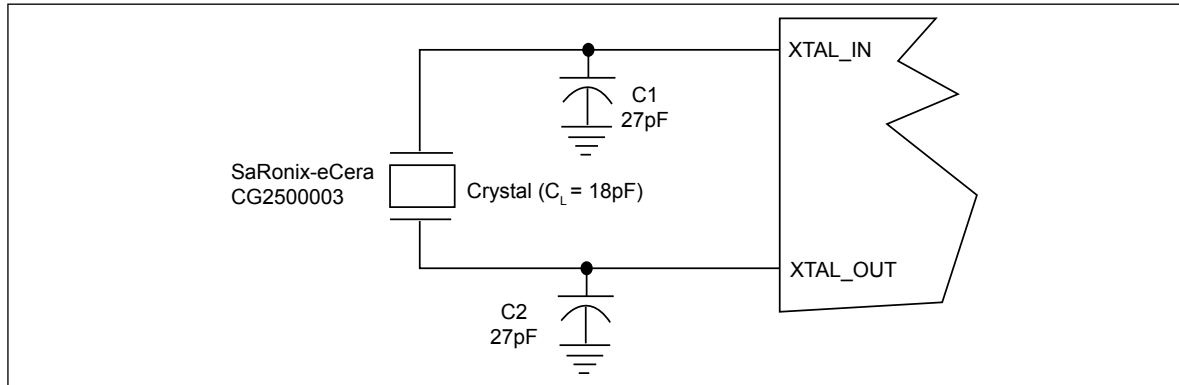
| Parameter | Min | Typ | Max | Unit |
|-----------------------------------|--------------|-----|--------------|--------|
| Cycle Time | - | 40 | - | ns |
| Duty Cycle | 45 | - | 55 | % |
| Rise/Fall Time (20%-80%) | 0.3 | - | 0.6 | ns |
| RMS Jitter (12kHz-5 MHz) | - | - | 2 (spur off) | ps-RMS |
| Clock Tolerance (25MHz) | -50 | - | +50 | ppm |
| Output High Voltage | $V_{DD}-1.4$ | | $V_{DD}-0.9$ | V |
| Output Low Voltage | $V_{DD}-2.0$ | | $V_{DD}-1.7$ | |
| Peak to Peak Output Voltage Swing | 0.6 | | 1.0 | |

Application Notes

Crystal circuit connection

The following diagram shows PI6C49021 crystal circuit connection with a parallel crystal. For the $CL=18\text{pF}$ crystal, it is suggested to use $C1=27\text{pF}$, $C2=27\text{pF}$. $C1$ and $C2$ can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



- CL = crystal spec. loading cap.
- Cj = chip in/output cap. (3~5pF)
- Cb = PCB trace/via cap. (2~4pF)
- C1,2 = load cap. components
- Rd = drive level res. (100ohm)

Final choose/trim $C1=C2=2 * CL - (Cb + Cj)$ for the target +/-ppm
 Example: $C1=C2=2*(18\text{pF}) - (4\text{pF}+5\text{pF})=27\text{pF}$

Recommended Crystal Specification

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, $CL=18\text{pF}$, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf
- b) FY2500081, SMD 5x3.2(4P), 25M, $CL=18\text{pF}$, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf
- c) FL2500047, SMD 3.2x2.5(4P), 25M, $CL=18\text{pF}$, +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>

Configuration test load board termination for HCSL Outputs

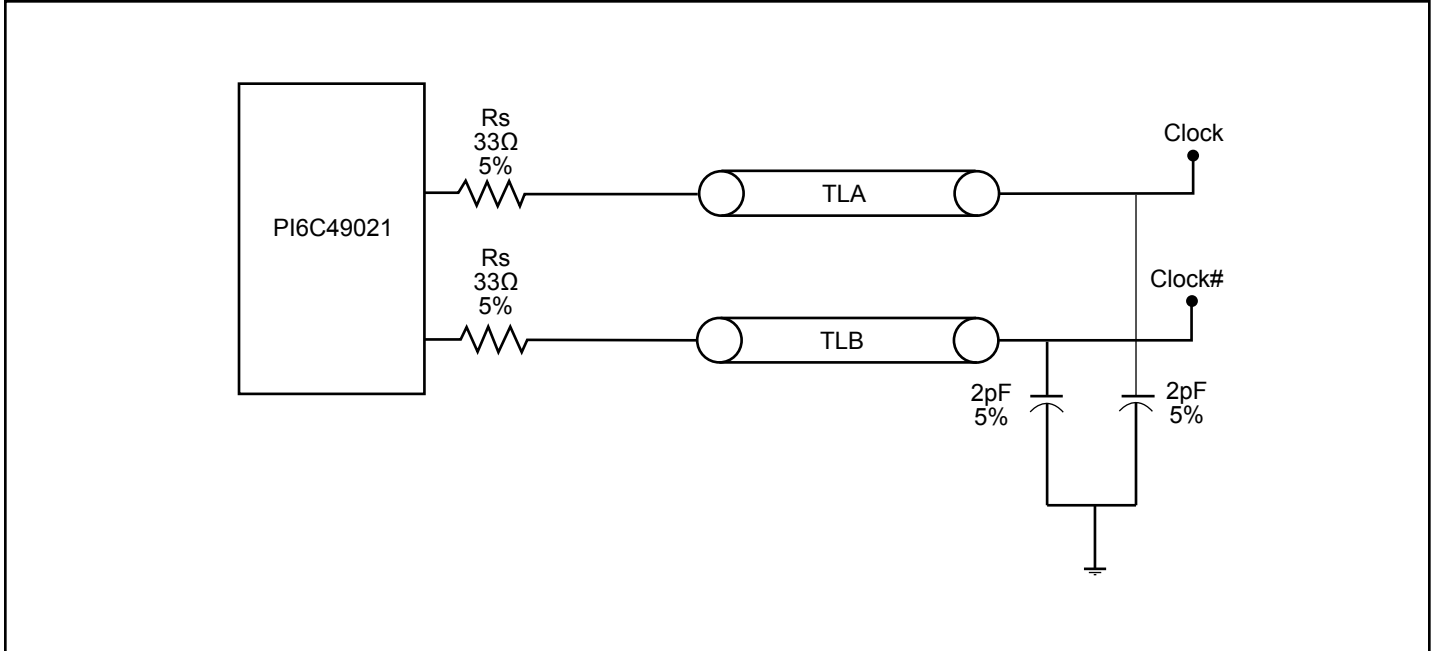


Figure 4. Configuration Test Load Board Termination

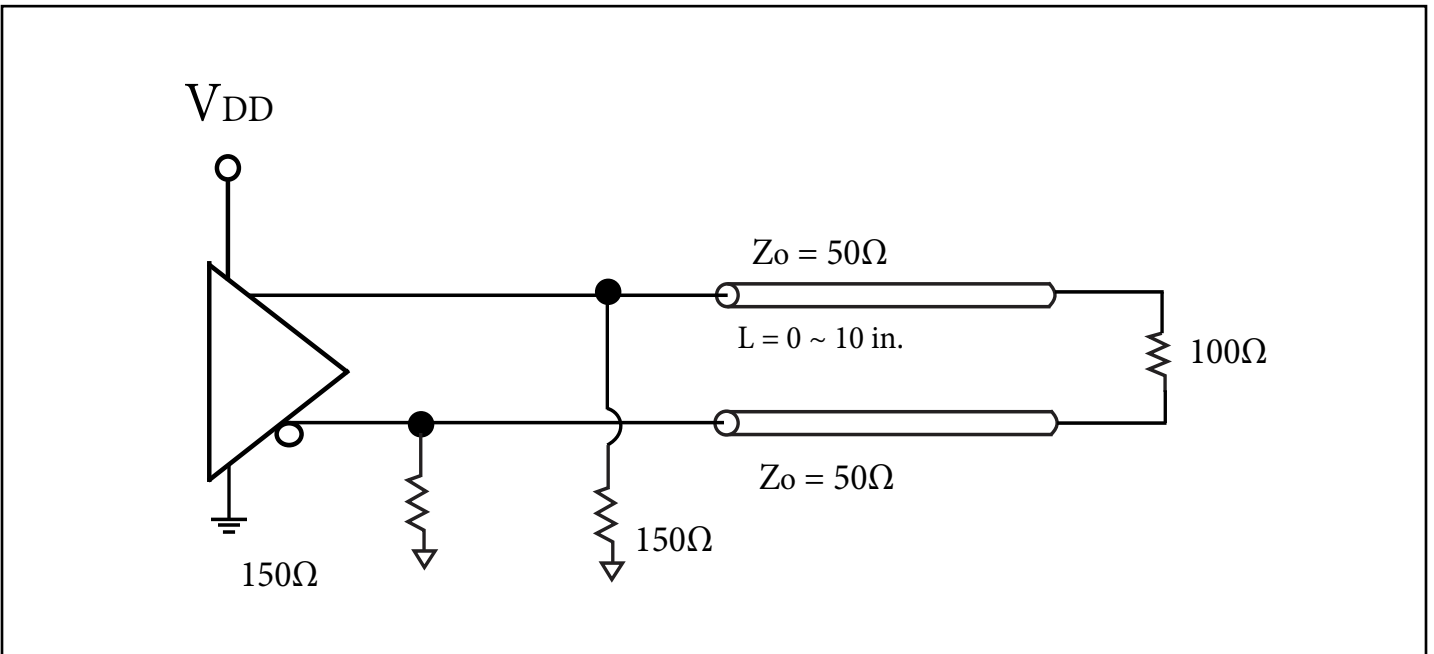
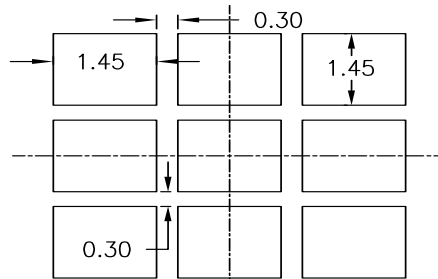
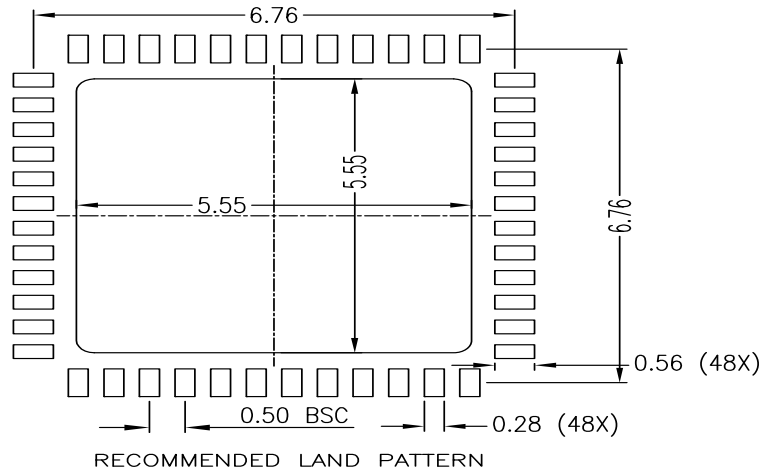


Figure 5. LVPECL output termination



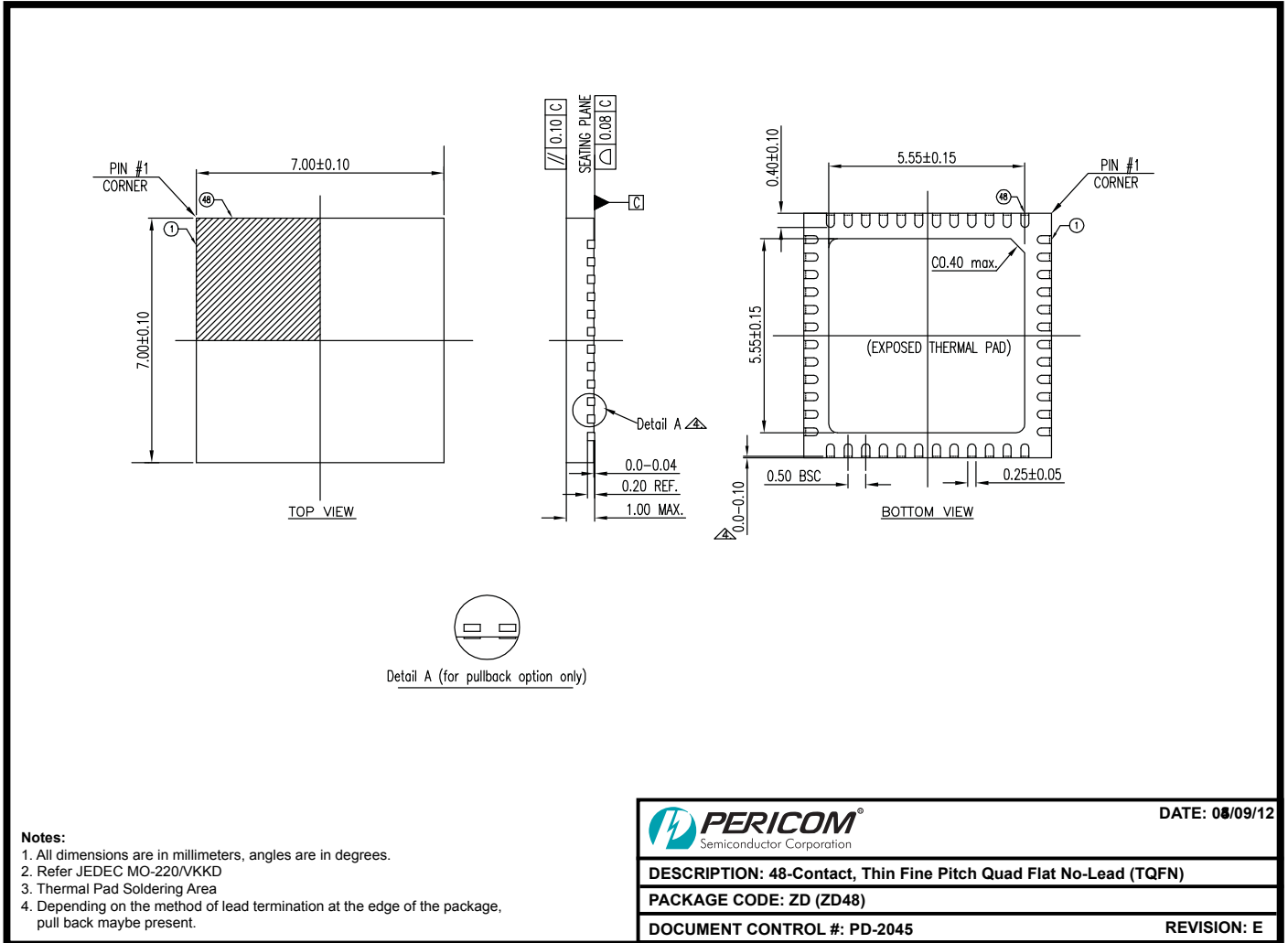
- NOTE :
1. ALL DIMENSIONS ARE IN MILLIMETER.
 2. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.



Pericom Semiconductor Corporation
<http://www.pericom.com>

| | |
|-------------------------------------|--------------|
| DESCRIPTION: Recommend Land Pattern | SHEET 1 of 1 |
| PACKAGE CODE: ZD48 (TQFN 7 X 7mm) | 20120927 |

Packaging Mechanical: 48-Contact TQFN (ZD)



Note: 12-0458

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information⁽¹⁻³⁾

| Ordering Code | Package Code | Package Description |
|---------------|--------------|-------------------------------|
| PI6C49021ZDIE | ZD | 48-pin, Pb-free & Green, TQFN |

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

单击下面可查看定价，库存，交付和生命周期等信息

[>>Diodes Incorporated\(达达科技\(美台\)\)](#)