A Product Line of
Diodes Incorporated

PI6CBF18501

Very Low Power 5-Output PCIe Fanout Buffer With On-chip Termination

Features

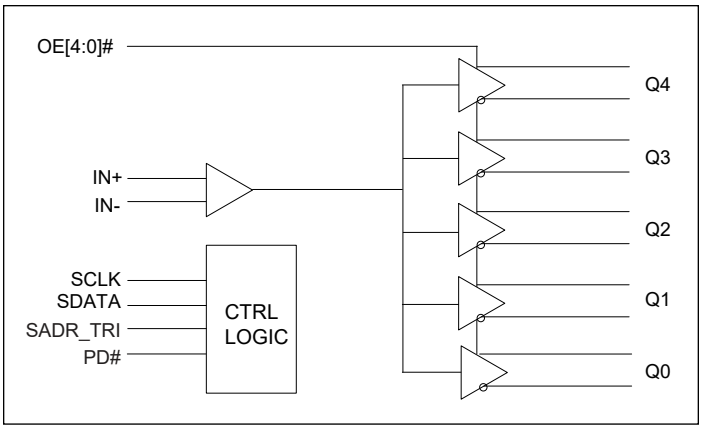
- 1.8V supply voltage
- HCSL input
- 5-differential low power HCSL outputs with on-chip termination
- Individual output enable
- Programmable slew rate and output amplitude for each output through SMBus
- 3.3V tolerant SMBus interface support
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - Differential output-to-output skew <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4 compliant
- Support industrial temperature range: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 40-lead 5×5mm TQFN

Description

The PI6CBF18501 is a 5-output, very low power PCIe Gen1/Gen2/Gen3/Gen4 clock buffer. The device takes a reference input to fanout 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination saves 24 external resistors and makes layout easier. Individual OE pins for each output provides easier power management.

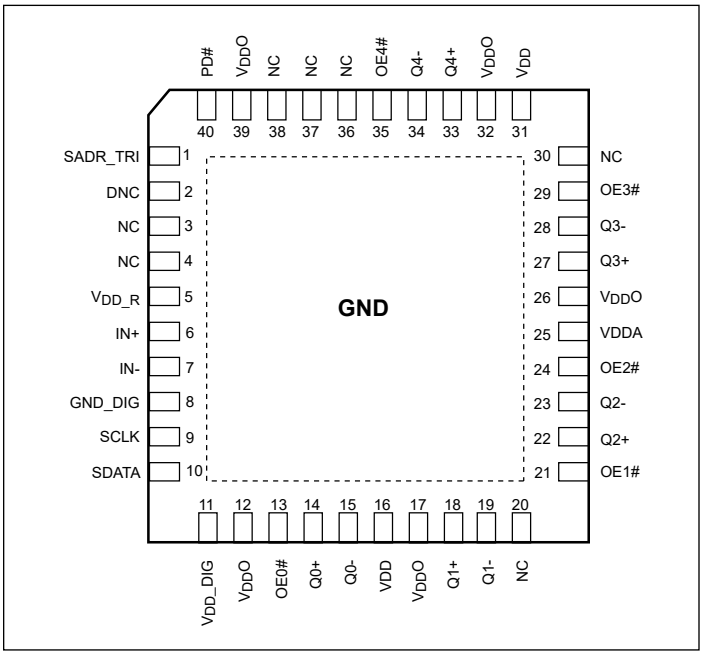
The device uses Diodes' proprietary design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4 requirements. It provides various advanced options, such as different slew rates and amplitudes through SMBus so users can easily configure the device to achieve the optimized performance for their individual boards.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin#	Pin Name	Type		Description
1	SADR_TRI	Input	Tri-level	Latch to select SMBus Address. This pin has an internal pull-down
2	DNC			Do not connect
3, 4, 20, 30, 36, 37, 38	NC			No connect
5	V_{DD}_R	Power		Power supply for input differential buffers
6	IN+	Input		Differential true clock input
7	IN-	Input		Differential complementary clock input
8	GND_DIG	Power		Ground for digital circuitry
9	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
10	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
11	V_{DD}_DIG	Power		Power supply for digital circuitry, nominal 1.8V
12, 17, 26, 32, 39	V_{DDO}	Power		Power supply for differential outputs
13	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
14	Q0+	Output	HCSL	Differential true clock output
15	Q0-	Output	HCSL	Differential complementary clock output
16, 31	V_{DD}	Power		Power supply, nominal 1.8V
18	Q1+	Output	HCSL	Differential true clock output
19	Q1-	Output	HCSL	Differential complementary clock output

Pin Description Cont.

Pin#	Pin Name	Type		Description
21	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
22	Q2+	Output	HCSL	Differential true clock output
23	Q2-	Output	HCSL	Differential complementary clock output
24	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
25	V_{DDA}	Power		Power supply for analog circuitry
27	Q3+	Output	HCSL	Differential true clock output
28	Q3-	Output	HCSL	Differential complementary clock output
29	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
33	Q4+	Output	HCSL	Differential true clock output
34	Q4-	Output	HCSL	Differential complementary clock output
35	OE4#	Input	CMOS	Active low input for enabling Q4 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
40	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
41	EPAD	Power		Connect to Ground

SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101011	X
	M	1101100	X
	1	1101101	X

Power Management Table

PD#	IN	SMBus OE bit	OEn#	Qn+	Qn-
0	X	X	X	Low	Low
1	Running	0	X	Low	Low
1	Running	1	0	Running	Running
1	Running	1	1	Low	Low

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Junction Temperature ..... 125°C
Supply Voltage to Ground Potential, V_{DDxx} .....–0.5V to +2.5V
Input Voltage ..... –0.5V to V_{DD}+0.5V, not exceed 2.5V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min..	Typ.	Max.	Units
V_{DD}, V_{DDA}, V_{DD}_R, V_{DD}_DIG	Power Supply Voltage		1.7	1.8	1.9	V
V_{DDO}	Output Power Supply Voltage		0.9975	1.05-1.8	1.9	V
I_{DDA}	Analog Power Supply Current	V_{DDA} + V_{DD}_R, All outputs active @100MHz		11	15	mA
I_{DD}	Power Supply Current	V_{DD} + V_{DD_DIG}, All outputs active @100MHz		6	10	mA
I_{DDO}	Power Supply Current for Outputs	All outputs active @100MHz		20	25	mA
I_{DDA_PD}	Analog Power Supply Power Down(1) Current	V_{DDA} + V_{DD}_R, All outputs active @100MHz		0.4	0.6	mA
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DD} + V_{DD_DIG}, All outputs LOW/LOW		0.5	0.8	mA
I_{DDO_PD}	Power Supply Current Power Down(1) for Outputs	V_{DDO}, All outputs LOW/LOW			0.1	mA
T_A	Ambient Temperature	Commercial grade	-40		85	°C

Note:

1. Input clock is not running.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal pull up resistance			120		KΩ
R_{dn}	Internal pull down resistance			120		KΩ
L_{PIN}	Pin inductance				7	nH

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal bus voltage		1.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.6	V
		SMBus, V_{DDSMB} < 3.3V			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SADR_TRI	0.4V_{DD}	0.5V_{DD}	0.6V_{DD}	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V
I_{IH}	Input High Current	Single-ended inputs, V_{IN} = V_{DD}			5	µA
I_{IL}	Input Low Current	Single-ended inputs, V_{IN} = 0V	-5			µA
I_{IH}	Input High Current	Single-ended inputs with pull up / pull down resistor, V_{IN} = V_{DD}			200	µA
I_{IL}	Input Low Current	Single-ended inputs with pull up / pull down resistor, V_{IN} = 0V	-200			µA
C_{IN}	Input Capacitance		1.5		5	pF

LVCMOS AC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{OELAT}	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion		20	300	us

HCSL Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IHDIF}	Diff. Input High Voltage(3)	IN+, IN-, single-end measurement	600	800	1150	mV
V_{ILDIF}	Diff. Input Low Voltage(3)	IN+, IN-, single-end measurement	-300	0	300	mV
V_{COM}	Diff. Input Common Mode Voltage		150		1000	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	300		1450	mV
f_{IN}	Input Frequency		1		200	MHz
t_{STAB}	Clock stabilization	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1.0	ms
t_{RF}	Diff. Input Slew Rate(2)	Measured differentially	0.4		8	V/ns
I_{IN}	Diff. Input Leakage Current	V_{IN} = V_{DD}, V_{IN} = GND	-5	0.01	5	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High(1)	Statistical measurement on single-ended signal using oscilloscope math function	660	770	850	mV
V_{OL}	Output Voltage Low(1)		-150		150	mV
V_{OMAX}	Output Voltage Maximum(1)	Measurement on single ended signal using absolute value		800	1150	mV
V_{OMIN}	Output Voltage Minimum(1)		-300	-15		mV
V_{OSWING}	Output Swing Voltage(1,2,3)	Scope averaging off	300	1536		mV
V_{OC}	Output Cross Voltage(1,2,4)		250	430	550	mV
DV_{OC}	V_{OC} Magnitude Change(1,2,5)			10	140	mV

Note:

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency			100		MHz
t_{RF}	Slew rate(1,2,3)	Scope averaging on fast setting	1.7	2.9	4.0	V/ns
		Scope averaging on slow setting	1.1	2.0	3.4	V/ns
Dt_{RF}	Slew rate matching(1,2,4)	Scope averaging on		7	20	%
t_{SKEW}	Output Skew(1,2)	Averaging on, V_T = 50%		43	50	ps
t_{PDELAY}	Propagation delay	V_T = 50%	3000	3600	4500	ps
tj_{c-c}	Cycle to cycle jitter(1,2)	Additive jitter		0.1	5	ps
t_{DCD}	Duty Cycle Distortion(1,7)	Measured differentially, at 100MHz	-1	0	1	%
tj_{PHASEA}	Additive Integrated phase jitter (RMS)(1,5,8)	PCIe Gen 1		0.6	5	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz		0.1	0.3	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)		0.05	0.1	ps
		PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.05	0.1	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.03	0.05	ps
$t_{STARTUP}$	Start up time				2	ms

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching applies to rising edge rate for Q+ and falling edge rate for Q-. It is measured using a +/-75mV window centered on the average cross point
5. See http://www.pcisig.com for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}
7. Duty cycle distortion is the difference in duty cycle between the out and input clock
8. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)*2 - (input jitter)*2]

SMBus Serial Data Interface

PI6CBF18501 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	See SBMus Address Selection table			1/0

Note: SMBus address is latched on SADR pin

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: Output Enable Register(1)

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Q4_OE	Q4 output enable	RW	1	Low/Low	Enabled
5	Reserved			1		
4	Q3_OE	Q3 output enable	RW	1	Low/Low	Enabled
3	Q2_OE	Q2 output enable	RW	1	Low/Low	Enabled
2	Q1_OE	Q1 output enable	RW	1	Low/Low	Enabled
1	Reserved			1		
0	Q0_OE	Q0 output enable	RW	1	Low/Low	Enabled

Note:
1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states

Byte 1: Output Amplitude Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			1		
5	Reserved			0		
4	Reserved			0		
3	Reserved			1		
2	Reserved			1		
1	Amplitude1	Control output amplitude	RW	1	'00' = 0.6V, '01' = 0.7V, '10' = 0.8V, '11' = 0.9V	
0	Amplitude0		RW	0		

Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	SLEWRATECTR_Q4	Control slew rate of Q4	RW	1	Slow setting	Fast setting
5	Reserved			1		
4	SLEWRATECTR_Q3	Control slew rate of Q3	RW	1	Slow setting	Fast setting
3	SLEWRATECTR_Q2	Control slew rate of Q2	RW	1	Slow setting	Fast setting
2	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
1	Reserved			1		
0	SLEWRATECTR_Q0	Control slew rate of Q0	RW	1	Slow setting	Fast setting

Byte 3: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	Reserved			0		
4	Reserved			0		
3	Reserved			0		
2	Reserved			1		
1	Reserved			1		
0	Reserved			1		

Byte 4: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved			1		

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	Rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Pericom = 0011	
2	PVID3		R	0		
1	PVID3		R	1		
0	PVID3		R	1		

Byte 6: Device Type/Device ID Register

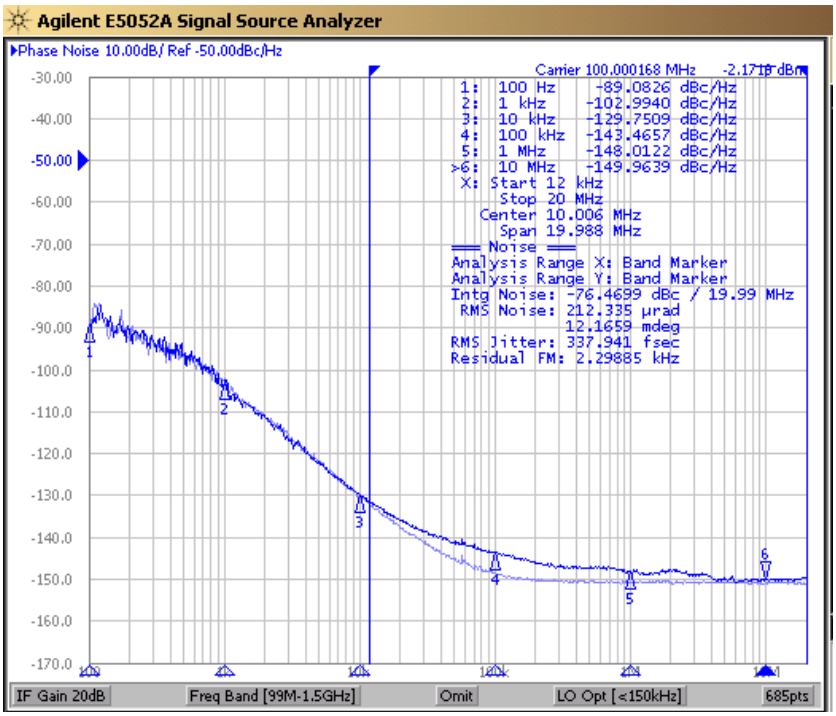
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DTYPE1	Device type	R	0		
6	DTYPE0		R	1		
5	DID5	Device ID	R	0	000110 binary, 06Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	1		
1	DID1		R	1		
0	DID0		R	0		

Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Phase Noise Plots

100MHz HCSL Clock



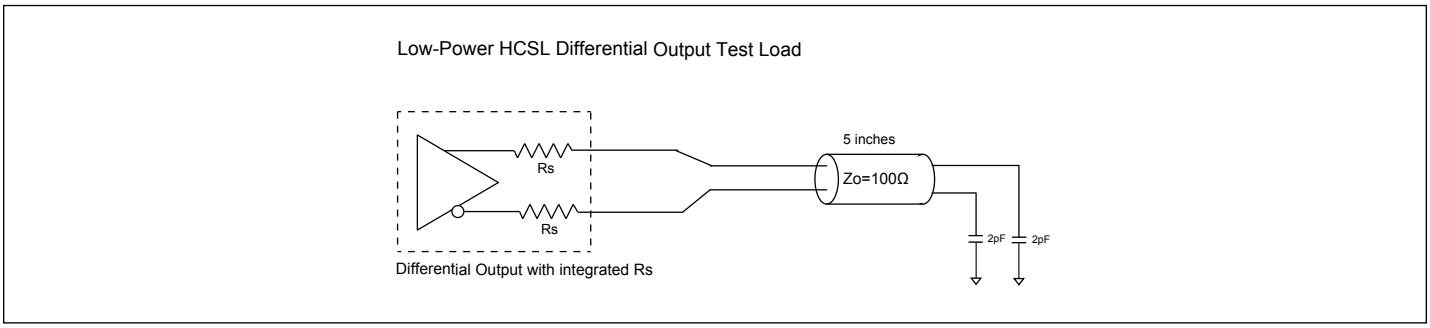


Figure 1. Low Power HCSL Test Circuit

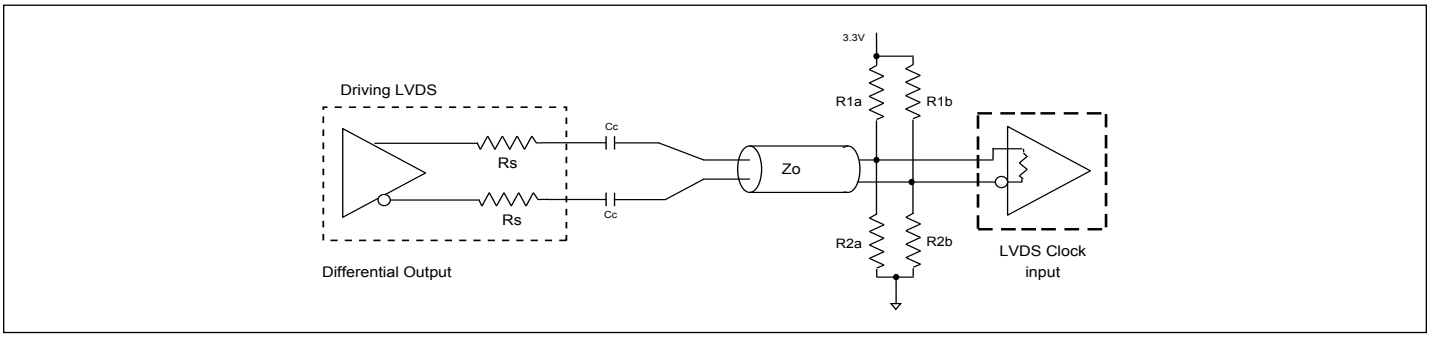


Figure 2. Differential Output Driving LVDS

Alternate Differential Output Terminations

Component	Receiver with termination	Receiver without termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5,600	75	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

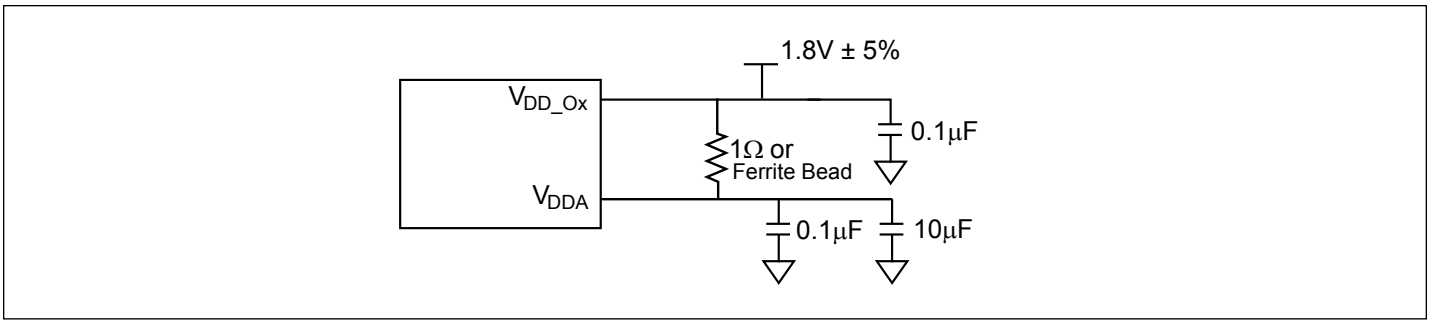


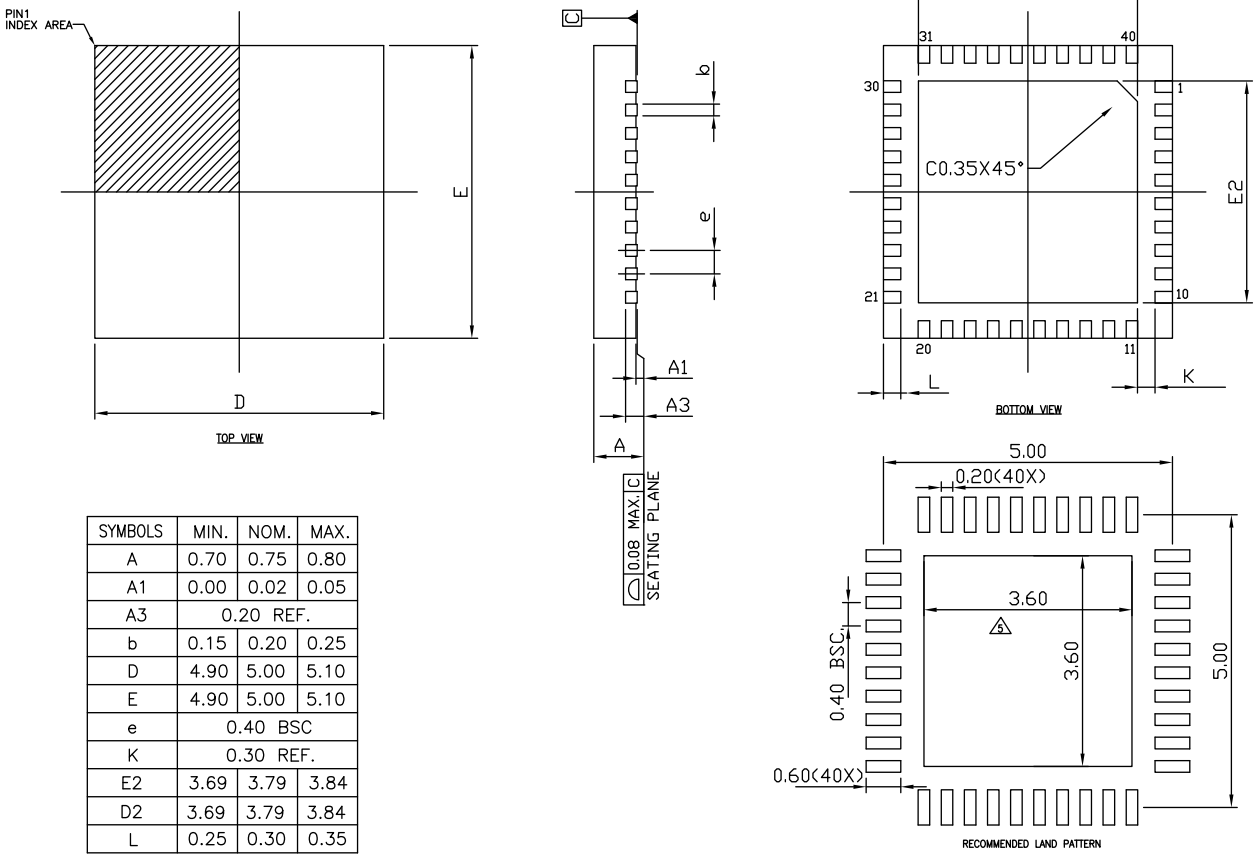
Figure 3. Power Supply Filter

Part Marking

PI6CBF18
501ZLAIE
YYWWXX̄
○

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 40-TQFN (ZLA)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.40 BSC	
K		0.30 REF.	
E2	3.69	3.79	3.84
D2	3.69	3.79	3.84
L	0.25	0.30	0.35

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 03/14/15

DESCRIPTION: 40-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLA (ZLA40)

DOCUMENT CONTROL #: PD-2195 REVISION: --

15-0019

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Pin 1 Location
PI6CBF18501ZLAIEX	ZLA	40-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Right Corner
PI6CBF18501ZLAIEX-13R	ZLA	40-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Left Corner

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)