AUTOMOTIVE-COMPLIANT, 40V, 3.5A SYNCHRONOUS BUCK WITH PROGRAMMABLE SOFT-START TIME

Description

The AP64351Q is an automotive-compliant, 3.5A, synchronous buck converter with a wide input voltage range of 3.8V to 40V. The device fully integrates a 75mΩ high-side power MOSFET and a 45mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

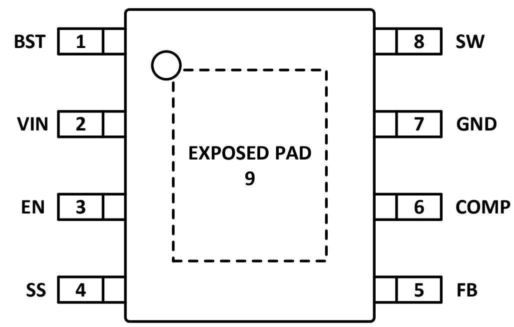
The AP64351Q device is easily used by minimizing the external component count due to its adoption of peak current mode control.

The AP64351Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. AP64351Q also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in an SO-8EP package.

Pin Assignments

(Top View)



SO-8EP

Features

- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- VIN: 3.8V to 40V
- 3.5A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22µA Low Quiescent Current (Pulse Frequency Modulation)
- 570kHz Switching Frequency
- Programmable Soft-Start Time
- Up to 85% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP64351Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- 12V Automotive Power Systems
- Automotive Infotainment
- Automotive Instrument Clusters
- Automotive Telematics
- Advanced Driver Assistance Systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

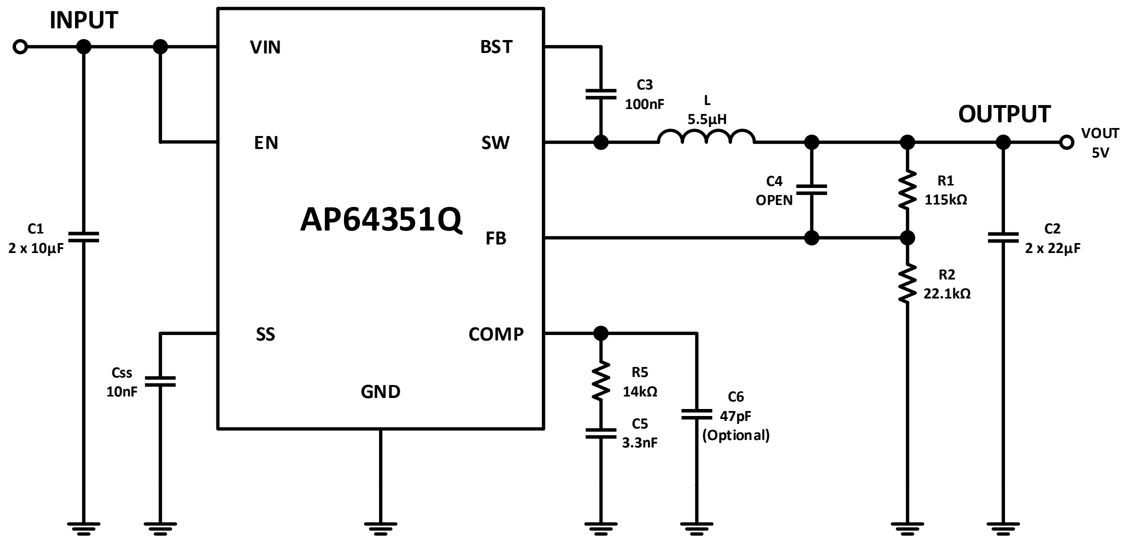


Figure 1. Typical Application Circuit

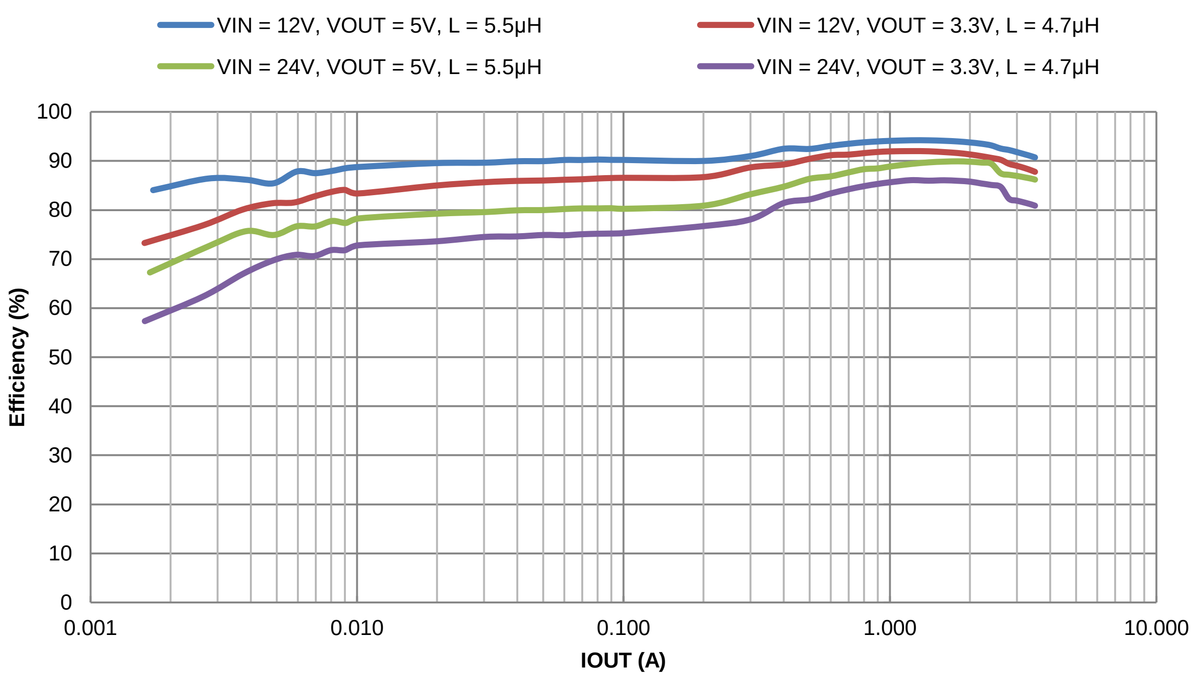


Figure 2. Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
BST	1	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
VIN	2	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 3.8V to 40V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup. The EN has a precision threshold of 1.18V for programing the UVLO. See **Enable** section for more details.
SS	4	Soft-start. Place a ceramic capacitor from this pin to ground to program soft-start time. An internal 4µA current source pulls the SS pin to VCC. See **Programming Soft-Start Time** section for more details.
FB	5	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
COMP	6	Compensation. Connect an external RC network to the COMP pin to adjust the loop response. See **External Loop Compensation Design** section for more details.
GND	7	Power Ground.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
EXPOSED PAD	9	Heat dissipation path of the die. The exposed thermal pad must be electrically connected to GND and must be connected to the ground plane of the PCB for proper operation and optimized thermal performance.

Functional Block Diagram

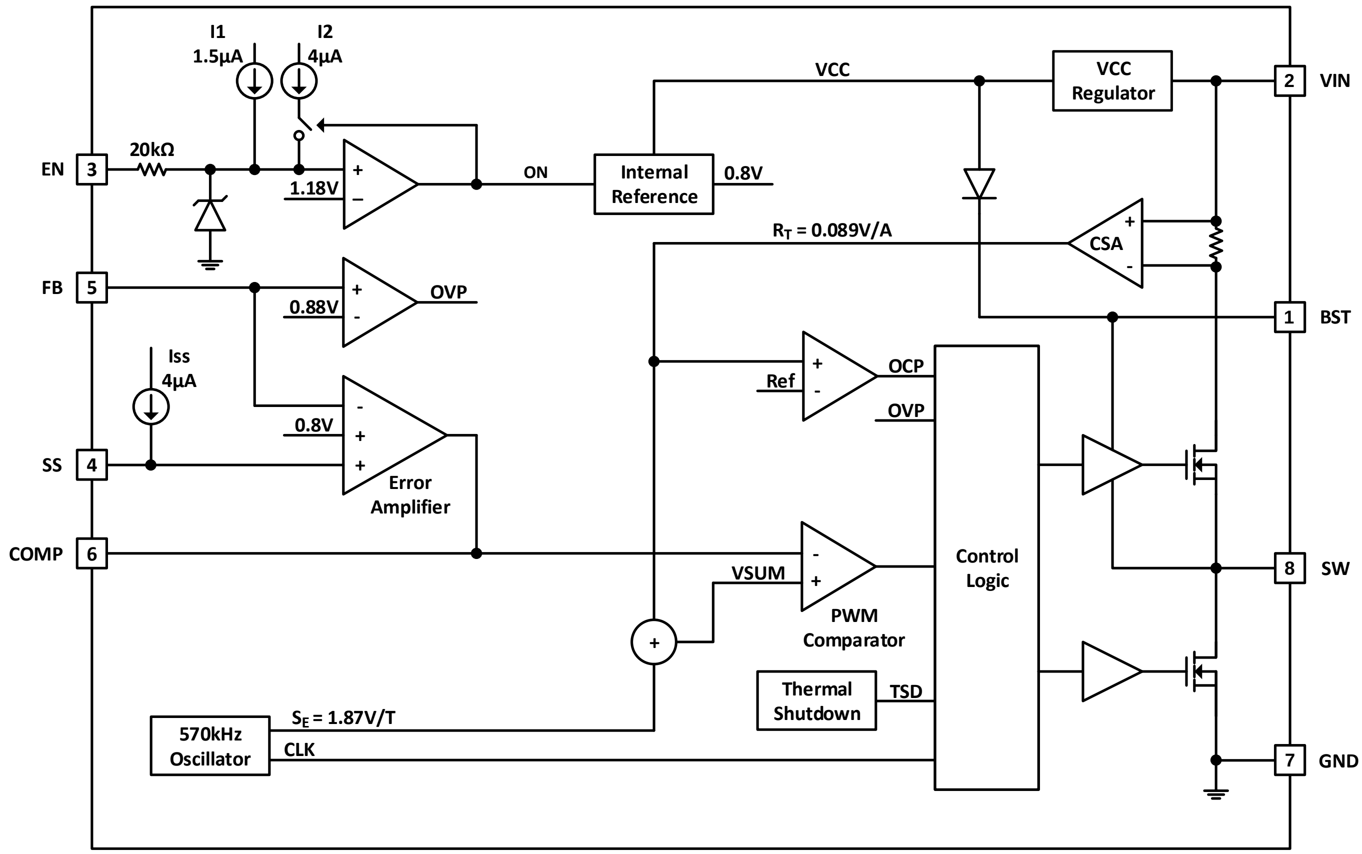


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +42.0 (DC)	V
		-0.3 to +45.0 (400ms)	
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +42.0	V
V_{SS}	Soft-Start Pin Voltage	-0.3 to +6.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
V_{COMP}	Compensation Pin Voltage	-0.3 to +6.0	V
V_{SW}	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±500	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SO-8EP	45	°C/W
θ_{JC}	Junction to Case	SO-8EP	5	°C/W

Note: 6. Test condition for SO-8EP: Device mounted on FR-4 substrate, four-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	40	V
VOUT	Output Voltage	0.8	VIN	V
T_A	Operating Ambient Temperature	-40	+125	°C
T_J	Operating Junction Temperature	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +150°C, and input voltage range, 3.8V to 40V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	—	µA
I_Q	Quiescent Supply Current	V_{EN} = Floating, V_{FB} = 1.0V	—	22	—	µA
POR	VIN Undervoltage Rising Threshold	—	—	3.5	3.7	V
UVLO	VIN Undervoltage Falling Threshold	—	—	3.1	—	V
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	75	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	45	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	—	4.2	5.0	6.5	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	—	—	5.5	—	A
I_{PFMPK}	PFM Peak Current Limit	—	—	750	—	mA
I_{ZC}	Zero Cross Current Threshold	—	—	0	—	mA
f_{SW}	Oscillator Frequency	—	500	570	640	kHz
t_{ON_MIN}	Minimum On-Time	—	—	100	—	ns
V_{FB}	Feedback Voltage	CCM	0.792	0.800	0.808	V
V_{EN_H}	EN Logic High Threshold	—	—	1.18	1.25	V
V_{EN_L}	EN Logic Low Threshold	—	1.03	1.09	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.5	—	µA
		V_{EN} = 1V	1	1.5	2	µA
t_{SS}	Soft-Start Time	C_{SS} = 10nF	—	2	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	+25	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP64351Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, C_{SS} = 10nF, unless otherwise specified.)

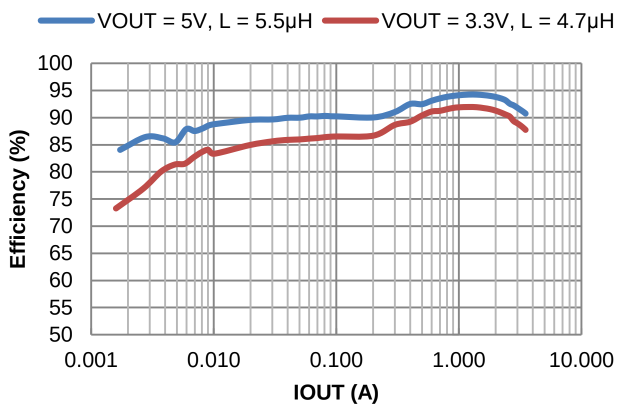


Figure 4. Efficiency vs. Output Current, VIN = 12V

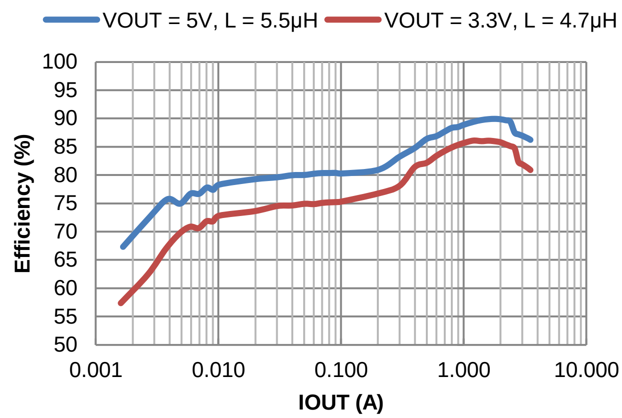


Figure 5. Efficiency vs. Output Current, VIN = 24V

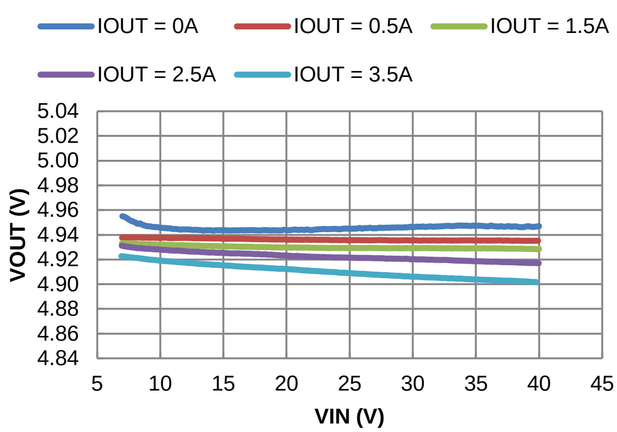


Figure 6. Line Regulation

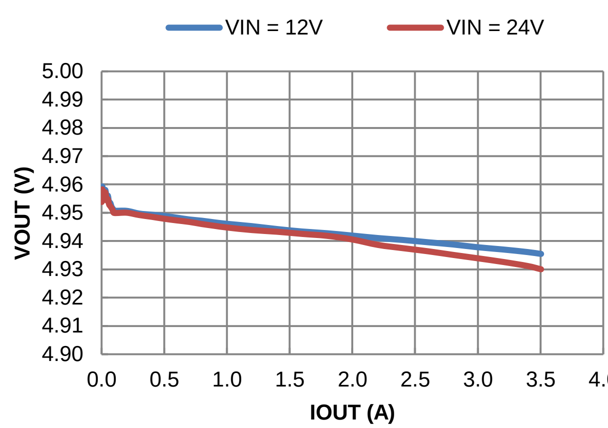


Figure 7. Load Regulation

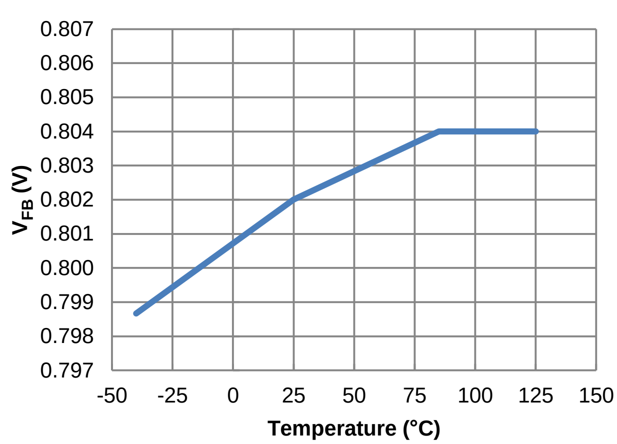


Figure 8. Feedback Voltage vs. Temperature

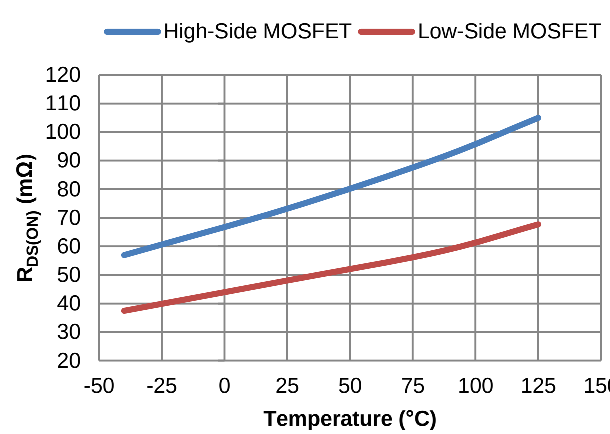


Figure 9. Power MOSFET $R_{DS(ON)}$ vs. Temperature

Typical Performance Characteristics (AP64351Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, C_{SS} = 10nF, unless otherwise specified.) (continued)

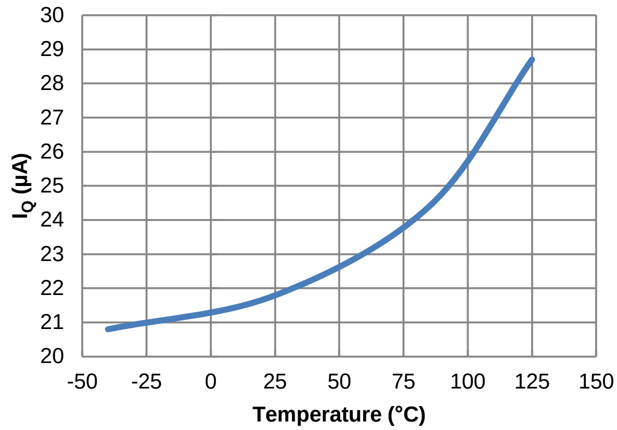


Figure 10. I_Q vs. Temperature

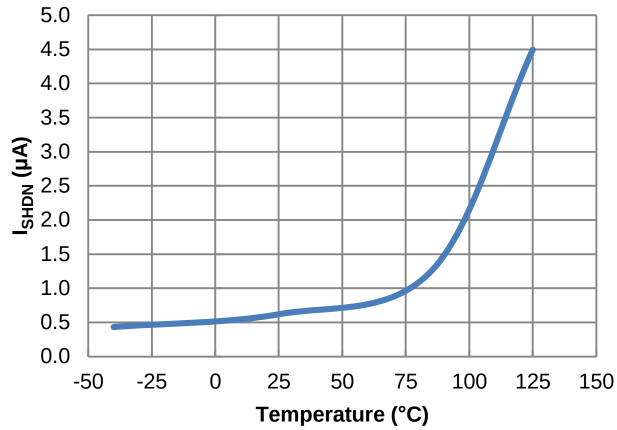


Figure 11. I_{SHDN} vs. Temperature

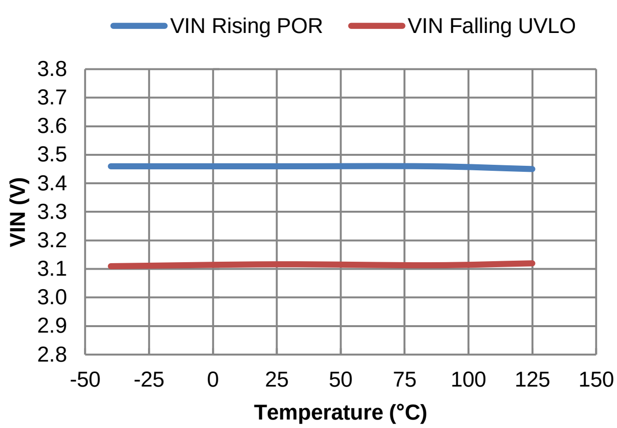


Figure 12. VIN Power-On Reset and UVLO vs. Temperature

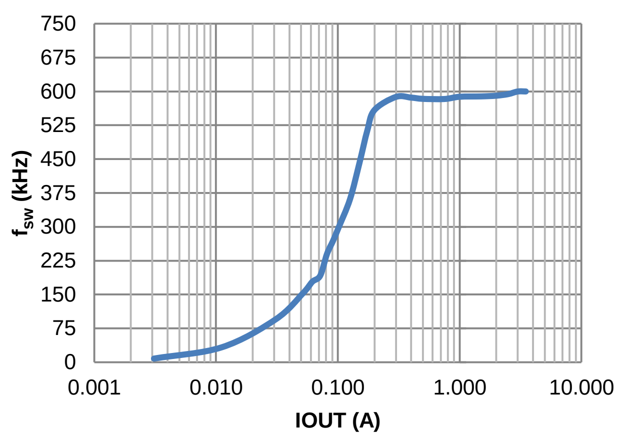


Figure 13. f_{SW} vs. Load

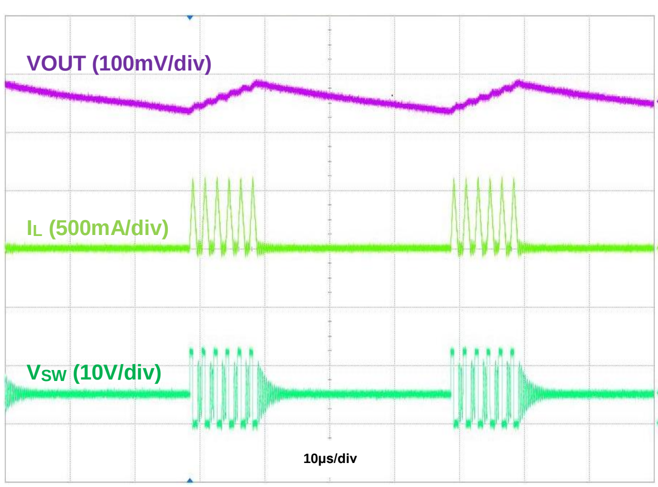


Figure 14. Output Voltage Ripple, IOUT = 50mA

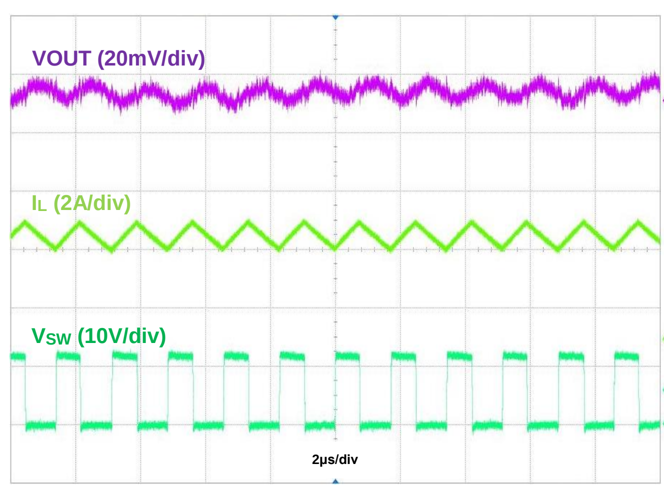


Figure 15. Output Voltage Ripple, IOUT = 3.5A

Typical Performance Characteristics (AP64351Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, C_{SS} = 10nF, unless otherwise specified.) (continued)

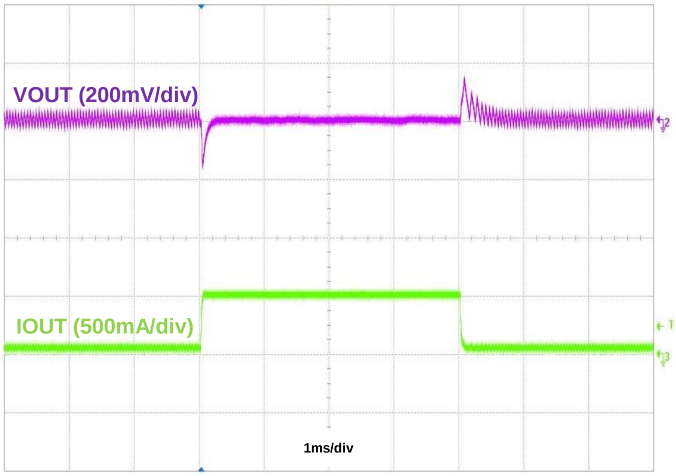


Figure 16. Load Transient, IOUT = 50mA to 500mA to 50mA

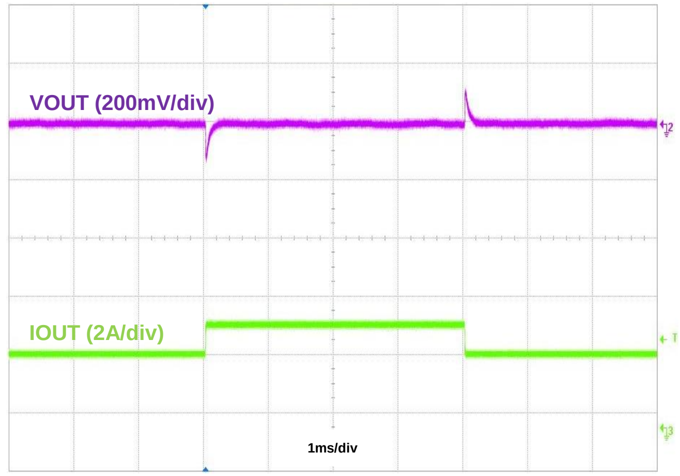


Figure 17. Load Transient, IOUT = 2A to 3.5A to 2A

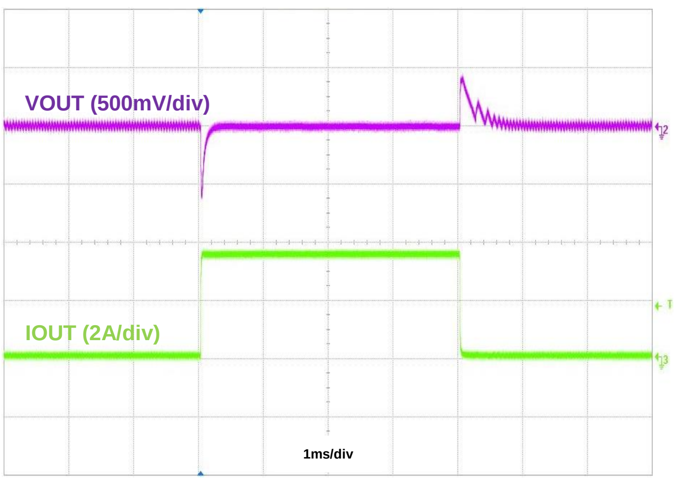


Figure 18. Load Transient, IOUT = 50mA to 3.5A to 50mA

Typical Performance Characteristics (AP64351Q at T_A = +25°C, VIN = 12V, VOUT = 5V, C_{SS} = 10nF, unless otherwise specified.) (continued)

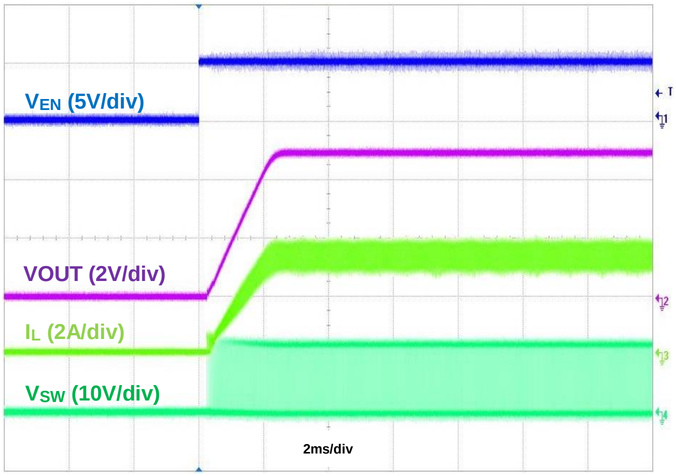


Figure 19. Startup Using EN, IOUT = 3.5A

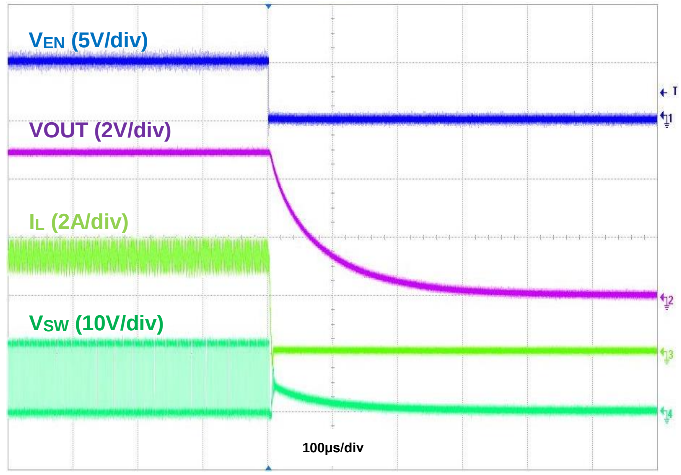


Figure 20. Shutdown Using EN, IOUT = 3.5A

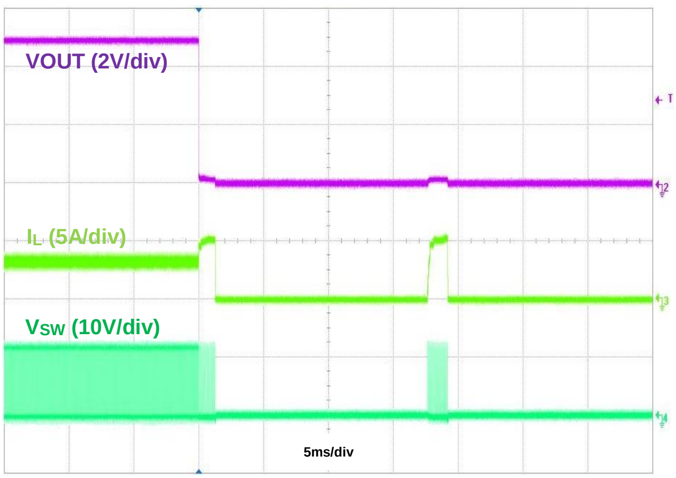


Figure 21. Output Short Protection, IOUT = 3.5A

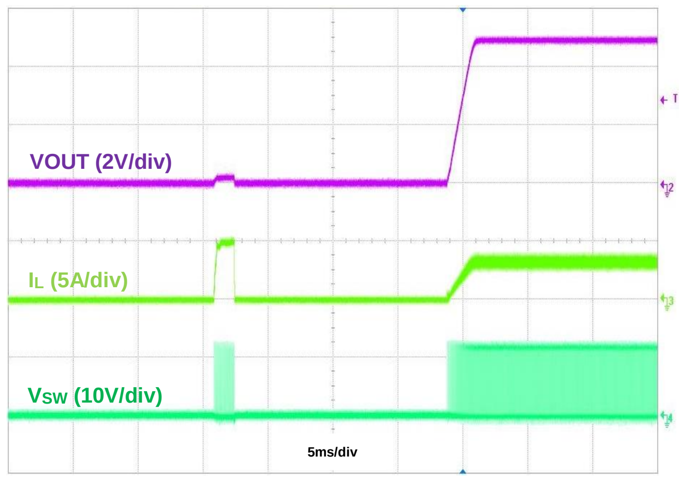


Figure 22. Output Short Recovery, IOUT = 3.5A

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP64351Q device is an automotive-compliant, 3.8V-to-40V input, 3.5A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 3. The device employs fixed-frequency peak current mode control. The internal 570kHz clock's rising edge initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The peak current mode control simplifies the AP64351Q footprint.

2 Pulse Frequency Modulation (PFM) Operation

In heavy load conditions, the AP64351Q operates in forced PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 750mA PFM peak inductor current limit. As the load current approaches zero, the AP64351Q enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 0mA, zero cross detection circuitry on the low-side power MOSFET, Q2, forces it off. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP64351Q works in PFM during light load conditions, it can achieve power efficiency of up to 85% at a 5mA load condition.

The quiescent current of AP64351Q is 22µA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1µA. When applying a voltage greater than the EN logic high threshold (typical 1.18V, rising), the AP64351Q enables all functions and the device initiates the soft-start phase. The EN pin is a high-voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases. An internal 1.5µA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP64351Q has a programmable soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.09V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Alternatively, a small ceramic capacitor can be added from EN to GND. When EN is not driven externally, this capacitor increases the time needed for the EN pin voltage to reach its logic high threshold, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. When the EN pin voltage starts from 0V, the amount of capacitance for a given delay time is approximated by:

$$\mathbf{C_d[nF] \approx 1.27 \cdot t_d[ms]} \qquad \textbf{Eq. 1}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

Application Information (continued)

4 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node and Frequency Spread Spectrum (FSS)

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP64351Q device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

To further improve EMI reduction, the AP64351Q device also implements FSS with a switching frequency jitter of ±6%. FSS reduces conducted and radiated interference at a particular frequency by spreading the switching noise over a wider frequency band and by not allowing emitted energy to stay in any one frequency for a significant period of time.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP64351Q device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP64351Q disables if the input voltage falls below 3.1V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 4µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 23.

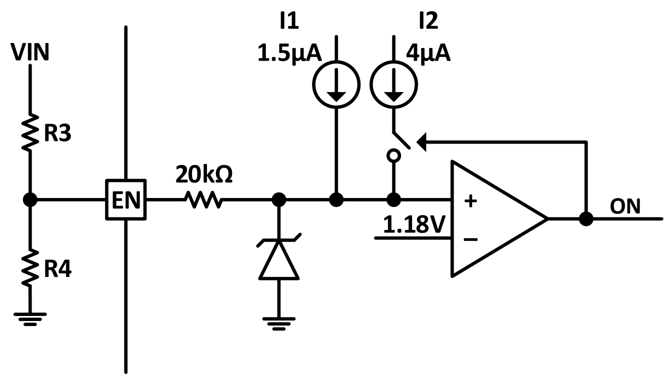


Figure 23. Programming UVLO

The resistive divider resistor values are calculated by:

$$\mathbf{R3} = \frac{\mathbf{0.924 \cdot V_{ON} - V_{OFF}}}{\mathbf{4.114\mu A}} \qquad \textbf{Eq. 2}$$

$$\mathbf{R4} = \frac{\mathbf{1.09 \cdot R3}}{\mathbf{V_{OFF} - 1.09V + 5.5\mu A \cdot R3}} \qquad \textbf{Eq. 3}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 3.7V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.3V

6 Output Overvoltage Protection (OVP)

The AP64351Q implements output OVP circuitry to minimize output voltage overshoots during decreasing load transients. The high-side power MOSFET turns off, and the low-side power MOSFET turns on when the output voltage exceeds its target by 5% in order to prevent the output voltage from continuing to increase.

Application Information (continued)

7 Overcurrent Protection (OCP)

The AP64351Q has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. Once the current through Q1 exceeds the peak current limit, Q1 immediately turns off. If Q1 consistently hits the peak current limit for 512 cycles, the buck converter enters hiccup mode and shuts down. After 8192 cycles of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

8 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP64351Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+135°C typical), the device initiates a normal power-up cycle with soft-start.

9 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 4}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

For the SO-8EP package, the θ_{JA} is 45°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 24 shows a typical derating curve versus ambient temperature.

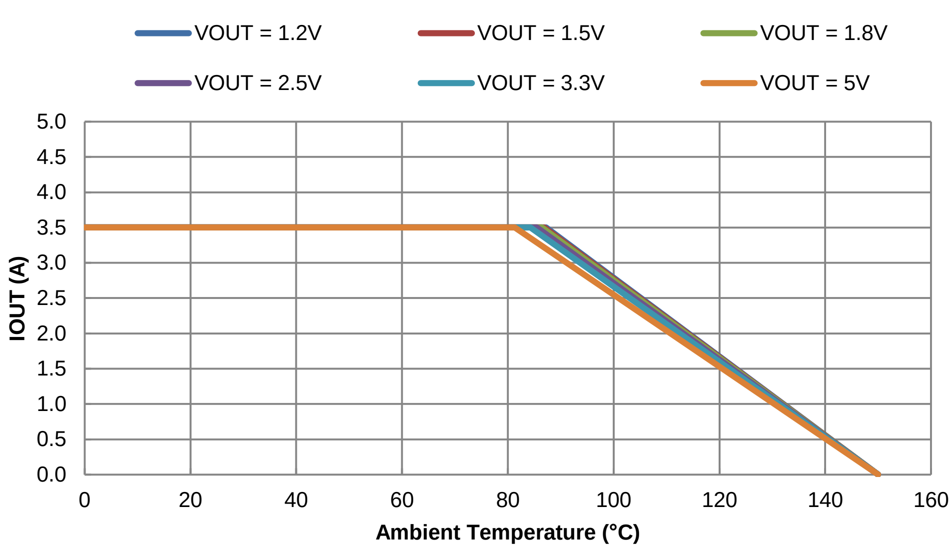


Figure 24. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

Application Information (continued)

10 Setting the Output Voltage

The AP64351Q has adjustable output voltages starting from 0.8V using an external resistive divider. An optional external capacitor, C4 in Figure 1, of 10pF to 220pF improves the transient response. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1} = \mathbf{R2} \cdot \left(\frac{\mathbf{VOUT}}{\mathbf{0.8V}} - \mathbf{1}\right) \qquad \textbf{Eq. 6}$$

Table 1 shows a list of recommended component selections for common AP64351Q output voltages referencing Figure 1.

Table 1. Recommended Components Selections

AP64351Q										
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**	**C3 (nF)**	**C4 (pF)**	**R5 (kΩ)**	**C5 (nF)**	**C6 (pF) (Optional)**
1.2	11.0	22.1	3.3	2 × 10	2 × 22	100	OPEN	3.32	3.3	180
1.5	19.6	22.1	3.3	2 × 10	2 × 22	100	OPEN	4.22	3.3	120
1.8	27.4	22.1	3.3	2 × 10	2 × 22	100	OPEN	4.99	3.3	120
2.5	47.5	22.1	4.7	2 × 10	2 × 22	100	OPEN	6.98	3.3	82
3.3	69.8	22.1	4.7	2 × 10	2 × 22	100	OPEN	9.31	3.3	56
5.0	115.8	22.1	5.5	2 × 10	2 × 22	100	OPEN	14.00	3.3	39
12.0	309.0	22.1	10.0	2 × 10	2 × 22	100	OPEN	33.20	3.3	18

11 Programming Soft-Start Time

The AP64351Q features a programmable soft-start time to prevent inrush current during the start-up sequence. Connect an external soft-start capacitor, C_{SS}, from the SS pin to ground.

The SS pin sources an internal 4µA current to charge C_{SS} when the EN pin exceeds the device's turn-on threshold. AP64351Q uses the lower voltage between the SS pin voltage and the internal 0.8V reference voltage as the input reference voltage for the error amplifier to regulate the output. Soft-start finishes when the SS pin voltage exceeds the 0.8V internal reference. The C_{SS} capacitance required for a given soft-start time is calculated by:

$$\mathbf{C_{SS}[nF] = 3.7 \cdot t_{SS}[ms]} \qquad \textbf{Eq. 7}$$

Where:

- C_{SS} is the capacitance in nF and is at least 10nF
- t_{SS} is the soft-start time in ms and is at least 2ms

Application Information (continued)

12 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{SW}}} \qquad \text{Eq. 8}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP64351Q, choose ΔI_L to be 30% to 50% of the maximum load current of 3.5A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \qquad \text{Eq. 9}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 2.2µH to 10µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 30mΩ. Use a larger inductance for improved efficiency under light load conditions.

13 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 20µF or greater is sufficient for most applications.

Application Information (continued)

14 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{SW}} \cdot \mathbf{COUT}} \right) \quad \text{Eq. 10}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \text{Eq. 11}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

15 Bootstrap Capacitor and Low-Dropout (LDO) Operation

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins. A 100nF ceramic capacitor is sufficient. If the bootstrap capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 300ns to refresh the bootstrap capacitor and raise its voltage back above 2.55V. The bootstrap capacitor threshold voltage is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event that requires the refreshing of the bootstrap capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low-dropout mode by holding Q1 on for multiple clock cycles. To prevent the bootstrap capacitor from discharging, Q2 is forced to refresh. The effective duty cycle is approximately 100% so that it acts as an LDO to maintain the output voltage regulation.

Application Information (continued)

16 External Loop Compensation Design

When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses a constant frequency, peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. Thus, the system becomes a single-order system. For loop stabilization, it is simpler to design a Type II compensator for current mode control than it is to design a Type III compensator for voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 25 shows the small signal model of the synchronous buck regulator.

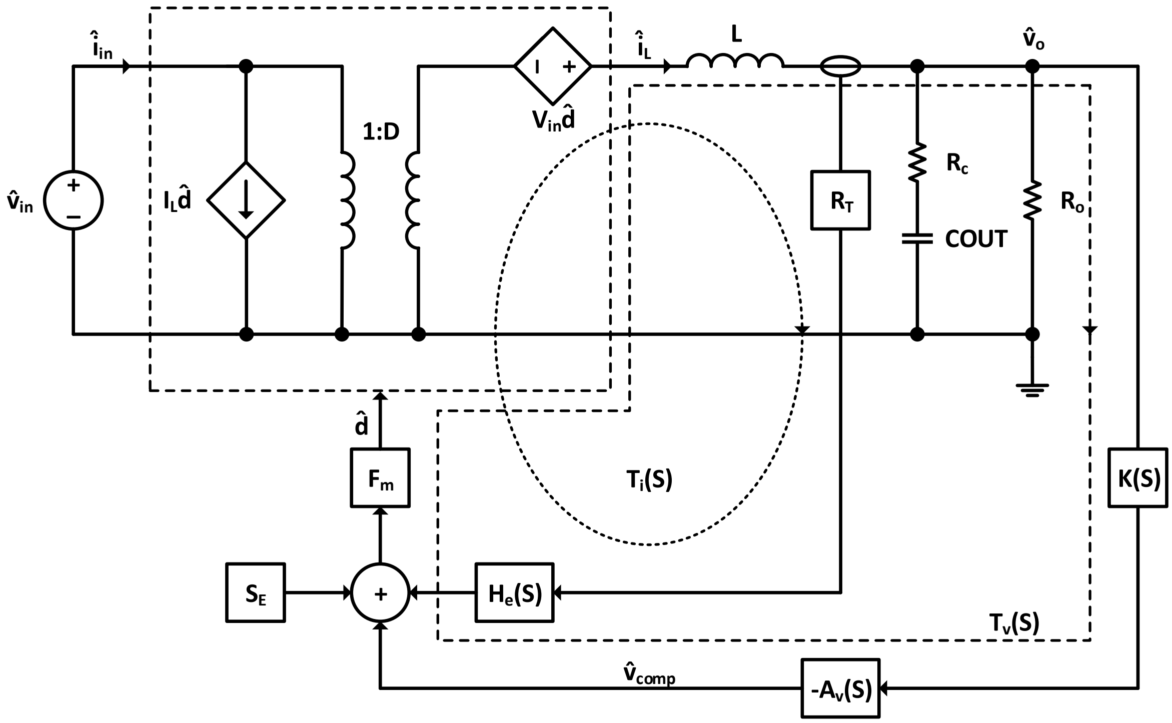


Figure 25. Small Signal Model of Buck Regulator

Where:

- $T_V(S)$ is the voltage loop
- $T_i(S)$ is the current loop
- K(S) is the voltage sense gain
- $-A_V(S)$ is the feedback compensation gain
- $H_e(S)$ is the current sampling function
- F_m is the PWM comparator gain
- V_{in} is the DC input voltage
- D is the duty cycle
- R_c is the ESR of the output capacitor, COUT
- R_o is the output load resistance
- $\hat{v}_{in}$ is the AC small-signal input voltage
- $\hat{i}_{in}$ is the AC small-signal input current
- $\hat{d}$ is the modulation of the duty cycle
- $\hat{i}_L$ is the AC small signal of the inductor current
- $\hat{v}_o$ is the AC small signal of output voltage
- $\hat{v}_{comp}$ is the AC small signal voltage of the compensation network

Application Information (continued)

16 External Loop Compensation Design (continued)

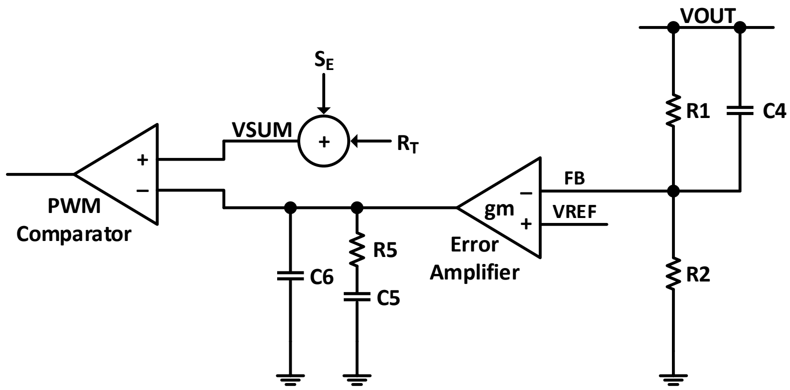


Figure 26. Type II Compensator

Figure 26 shows a Type II compensator. Its transfer function is expressed in the following equation:

$$\mathbf{A_v(S) \cdot K(S) = \frac{gm \cdot R5}{S \cdot (C5 + C6) \cdot (R1 + R2)} \frac{\left(1 + \frac{S}{\omega_{z1}}\right)\left(1 + \frac{S}{\omega_{z2}}\right)}{\left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)}} \quad \textbf{Eq. 12}$$

Where the poles and zeroes are:

$$\mathbf{\omega_{z1} = \frac{1}{R5 \cdot C5}} \quad \textbf{Eq. 13}$$

$$\mathbf{\omega_{z2} = \frac{1}{R1 \cdot C4}} \quad \textbf{Eq. 14}$$

$$\mathbf{\omega_{p1} = \frac{C5 + C6}{R5 \cdot C5 \cdot C6}} \quad \textbf{Eq. 15}$$

$$\mathbf{\omega_{p2} = \frac{R1 + R2}{R1 \cdot R2 \cdot C4}} \quad \textbf{Eq. 16}$$

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_C) less than 10% of f_{SW}

Application Information (continued)

16 External Loop Compensation Design (continued)

The loop gain at the crossover frequency has unity gain. Therefore, the compensator resistance, R5, is determined by:

$$\mathbf{R5} = \frac{2\pi \cdot f_c \cdot VOUT \cdot C_O \cdot R_T}{g_m \cdot V_{FB}} = 4.67x10^3 [\frac{\Omega}{A}] \cdot f_c \cdot VOUT \cdot COUT \qquad \text{Eq. 17}$$

Where:

- g_m is 0.15mS
- R_T is 0.089V/A
- V_{FB} is 0.8V
- f_c is the desired crossover frequency

Be aware that most ceramic capacitors will degrade with voltage stress or temperature extremes. Refer to its datasheet and use its worst case capacitance value for calculations.

The compensation capacitors C5 and C6 are then equal to:

$$C5 = \frac{VOUT \cdot COUT}{IOUT \cdot R5} \qquad \text{Eq. 18}$$

$$C6 = \max\left(\frac{R_C \cdot C_O}{R5}, \frac{1}{\pi \cdot f_{sw} \cdot R5}\right) \qquad \text{Eq. 19}$$

Where:

- IOUT is the output load current

The inclusion of C6 can increase gain margin and can decrease phase margin. In most cases, C6 is optional and may be omitted.

The zero, ω_{z2}, is optional as it can increase both the phase margin and gain bandwidth and can decrease gain margin. If used, place this zero at around two to five times f_C. Thus, C4 is in the approximate range of:

$$C4 = \left[\frac{1}{10\pi \cdot f_C \cdot R1}, \frac{1}{4\pi \cdot f_C \cdot R1}\right] \qquad \text{Eq. 20}$$

Application Information (continued)

16 External Loop Compensation Design (continued)

The following is an example of how to choose component values for external loop compensation. Actual component values used in the application circuit may vary slightly from the calculated first-order approximation equations.

Let the following conditions be defined:

- VIN = 12V
- VOUT = 5V
- IOUT = 3.5A
- f_{SW} = 570kHz
- f_c = 20kHz
- R1 = 115kΩ
- R2 = 22.1kΩ
- L = 5.5µH
- C2 = 2 × 22µF (Effectively, COUT ≈ 30µF)
- R_C ≈ 2mΩ

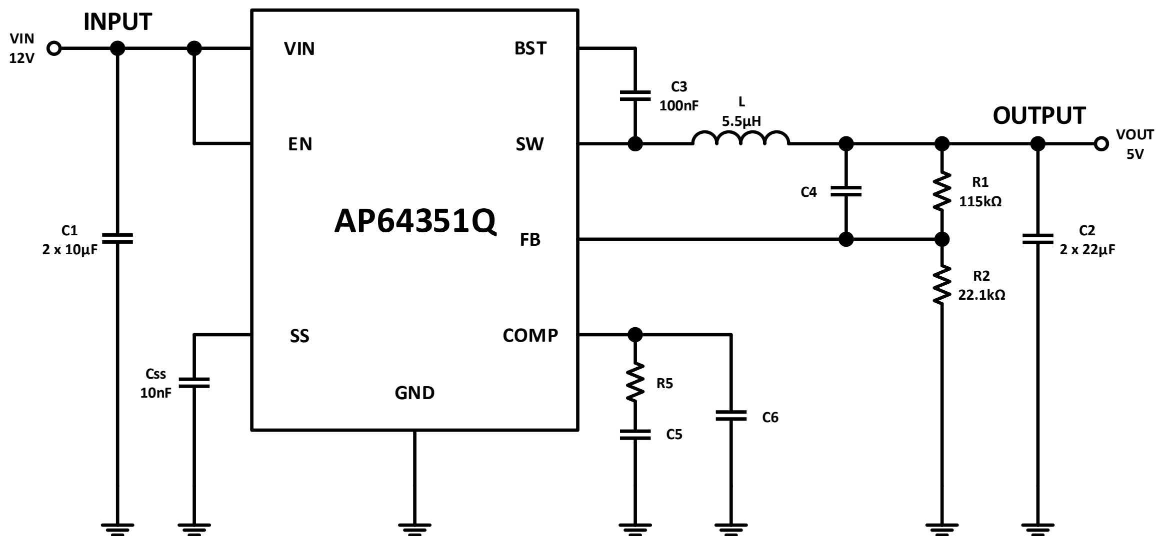


Figure 27. Example Circuit for Loop Compensation Calculations

The calculations of the main component values involved in the external loop compensation, R5 and C5, are required. If the optional C4 and C6 capacitors are used, their calculations are also required.

Application Information (continued)

16 External Loop Compensation Design (continued)

From Eq. 17, the value of R5 is calculated as:

$$\begin{aligned} R5 &= 4.67x10^{3}[\frac{\Omega}{A}] \cdot f_c \cdot VOUT \cdot COUT \\ &= 4.67x10^{3}[\frac{\Omega}{A}] \cdot 20kHz \cdot 5V \cdot 30\mu F \\ &\approx 14.01k\Omega \end{aligned}$$

Choose a standard resistor value for R5 close to its calculated value. For example, choose R5 to be 14kΩ.

From Eq. 18, C5 is calculated as:

$$\begin{aligned} C5 &= \frac{VOUT \cdot COUT}{IOUT \cdot R5} \\ &= \frac{5V \cdot 30\mu F}{3.5A \cdot 14k\Omega} \\ &\approx 3.1nF \end{aligned}$$

Choose a standard capacitor value for C5 close to its calculated value. For example, choose C5 to be 3.3nF.

From Eq. 19, C6 is calculated as:

$$\begin{aligned} C6 &= \max\left(\frac{R_C \cdot COUT}{R5}, \frac{1}{\pi \cdot f_{sw} \cdot R5}\right) \\ &= \max\left(\frac{2m\Omega \cdot 30\mu F}{14k\Omega}, \frac{1}{\pi \cdot 570kHz \cdot 14k\Omega}\right) \\ &\approx \max(4.3pF, 39.9pF) \\ &= 39.9pF \end{aligned}$$

C6 is optional. If used, choose a standard capacitor value for C6 close to its calculated value. For example, choose C6 to be 39pF.

From Eq. 20, the approximate range of C4 is calculated as:

$$\begin{aligned} C4 &= \left[\frac{1}{10\pi \cdot f_C \cdot R1}, \frac{1}{4\pi \cdot f_C \cdot R1}\right] \\ &= \left[\frac{1}{10\pi \cdot 20kHz \cdot 115k\Omega}, \frac{1}{4\pi \cdot 20kHz \cdot 115k\Omega}\right] \\ &= [13.8pF, 34.6pF] \end{aligned}$$

C4 is optional. If used, choose a standard capacitor value for C4 that is close to its calculated range. For example, choose C4 to be 33pF.

Application Information (continued)

16 External Loop Compensation Design (continued)

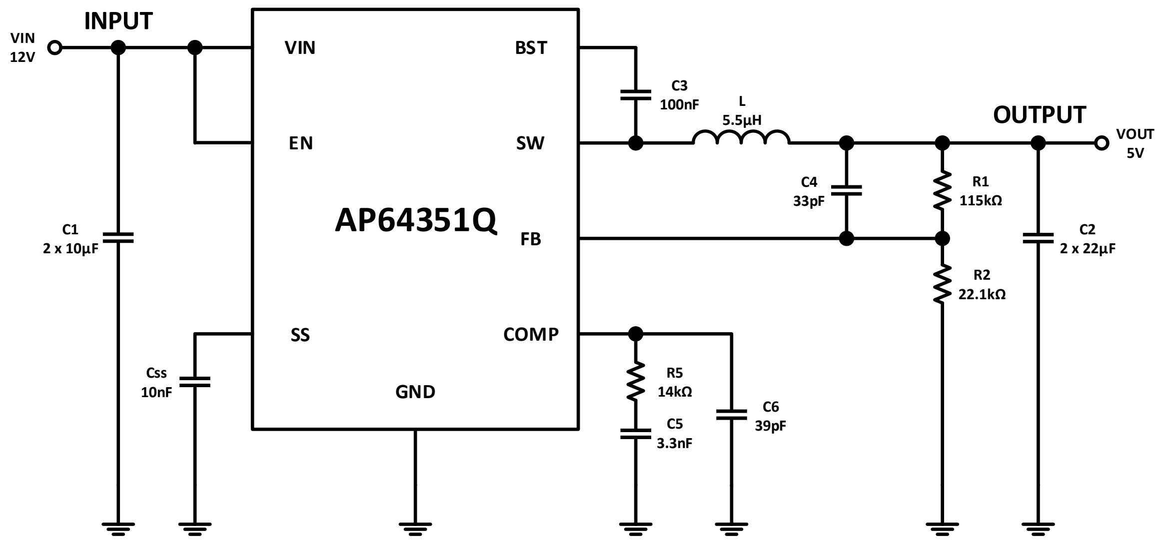


Figure 28. Example Circuit with Calculated Component Values for Loop Compensation

The first-order calculated loop response has the following characteristics:

- Bandwidth is around 16.6kHz
- Phase Margin is around 82.0°
- Gain Margin is around -27.1dB

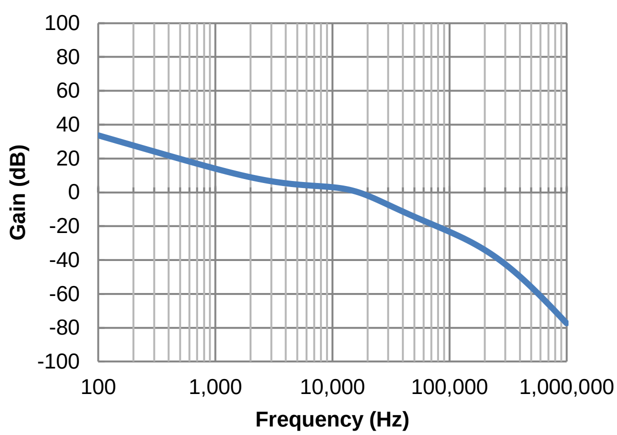


Figure 29. Closed-Loop Bandwidth

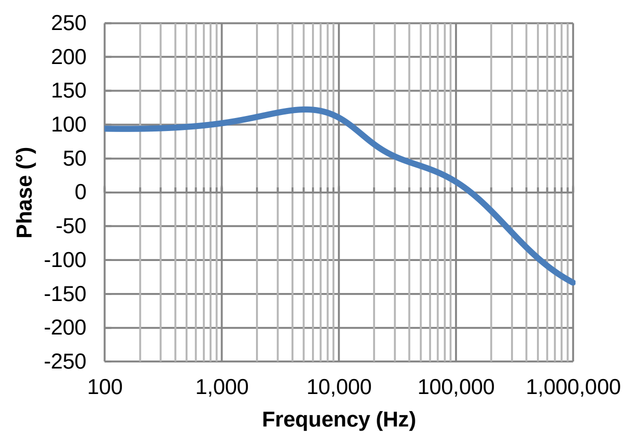


Figure 30. Closed-Loop Phase Margin

Layout

PCB Layout

1. The AP64351Q works at 3.5A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 31 for more details.

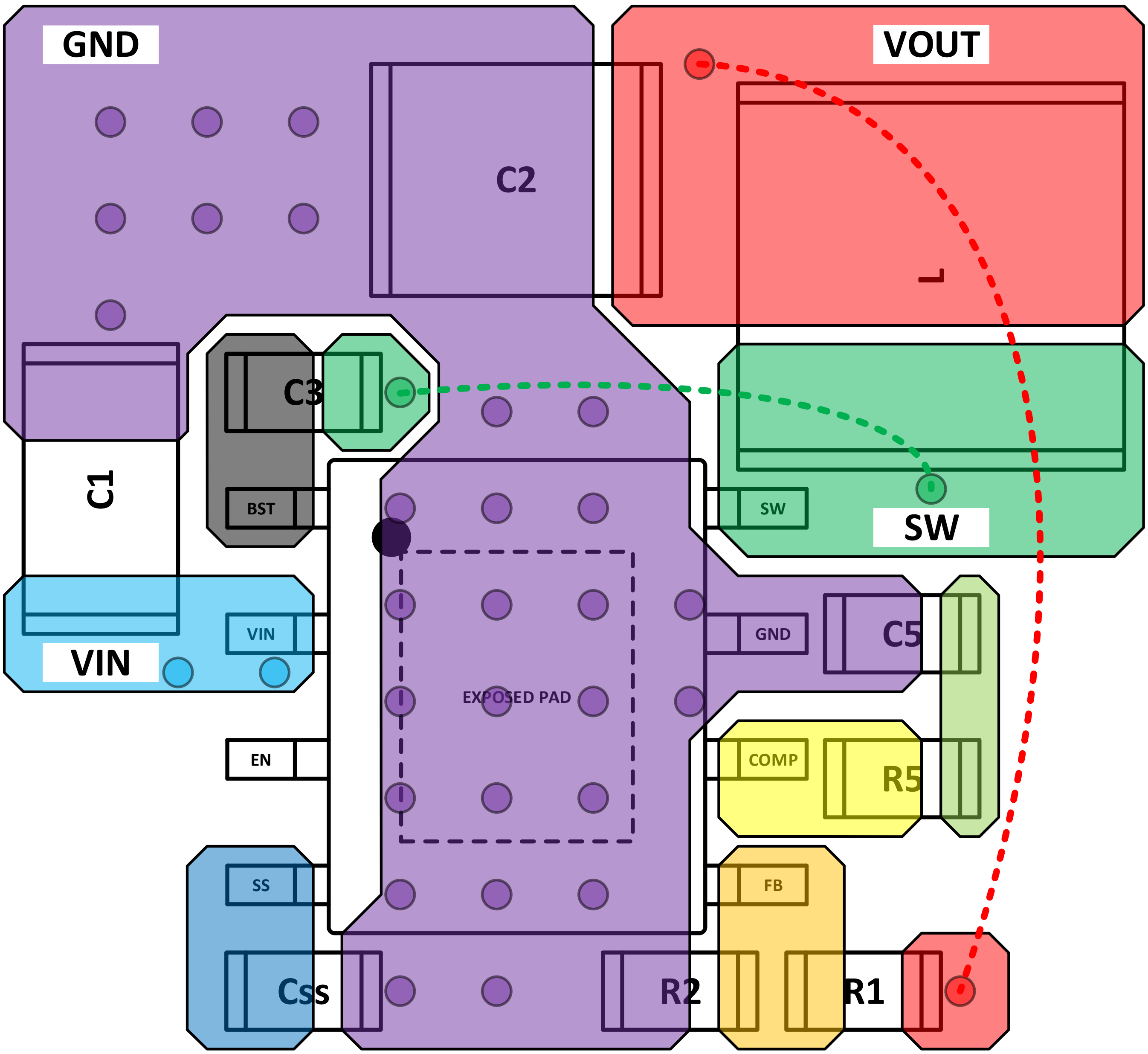
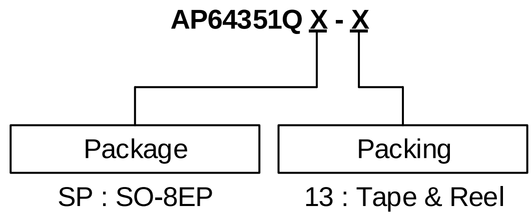


Figure 31. Recommended PCB Layout

Ordering Information

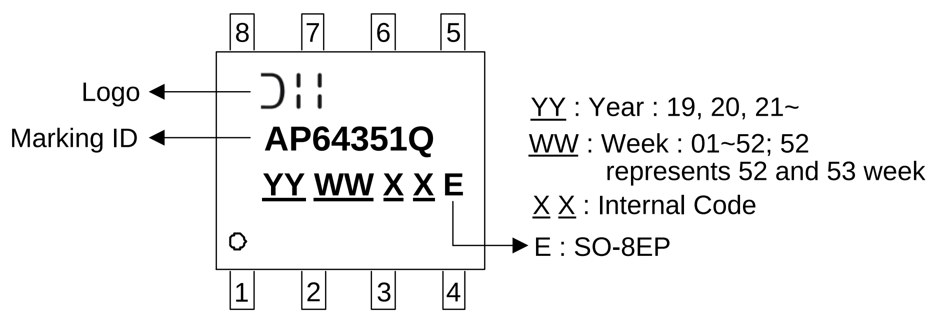


Part Number	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP64351QSP-13	SP	4000	-13

Marking Information

SO-8EP

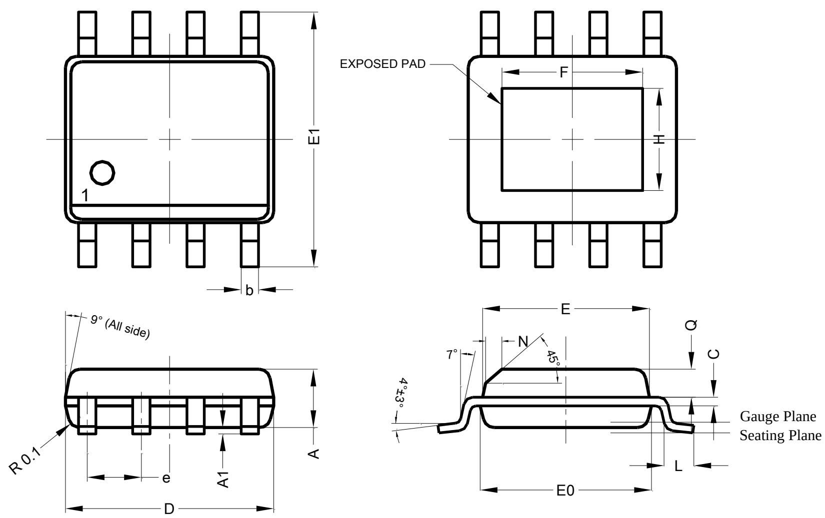
(Top View)



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP

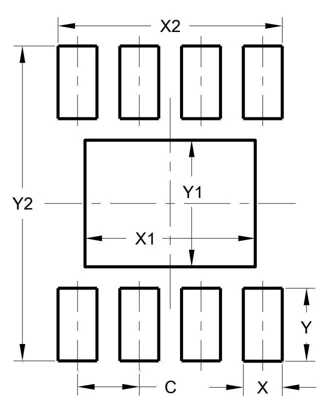


SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.078 grams (Approximate)