

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>A</sub> = +25°C
-20V	45mΩ @ V <sub>GS</sub> = -4.5V	-4.2A
	65mΩ @ V <sub>GS</sub> = -2.5V	-3.5A

## Description

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>), and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Applications

- General Purpose Interfacing Switch
- Power Management Functions

## Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

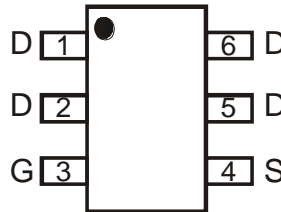
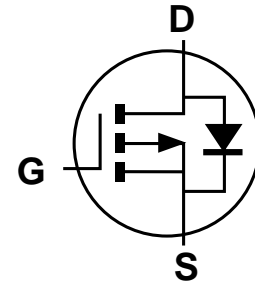
## Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.013 grams (Approximate)

TSOT26



Top View


 Top View  
Pin Configuration


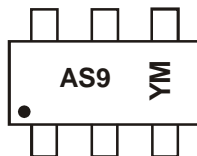
Equivalent Circuit

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2067LVT-7	TSOT26	3,000/Tape & Reel
DMP2067LVT-13	TSOT26	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



AS9 = Product Type Marking Code  
 YM = Date Code Marking  
 Y or Y = Year (ex: F = 2018)  
 M = Month (ex: 9 = September)

### Date Code Key

Year	2018	2019	2020	2021	2022	2023	2024	2025	2026
Code	F	G	H	I	J	K	L	M	N

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-20	V	
Gate-Source Voltage	V <sub>GSS</sub>	±8	V	
Drain Current (Note 5) Continuous	I <sub>D</sub>	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	-4.2 -3.4	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I <sub>DM</sub>	-30	A
Body-Diode Continuous Current (Note 5)	I <sub>S</sub>	-1.4	A	

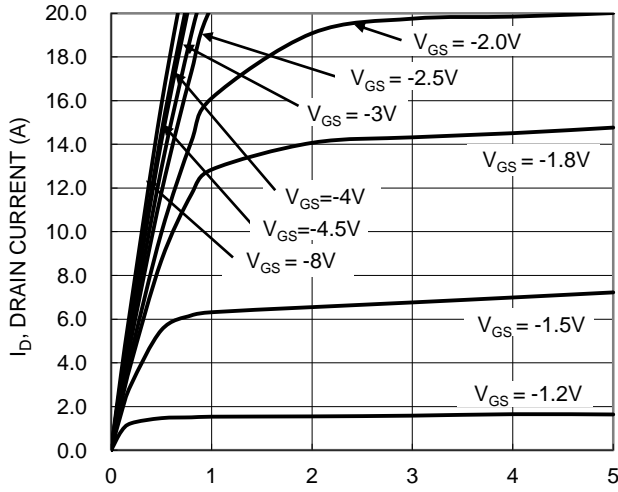
**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	105	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.6	W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	78	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

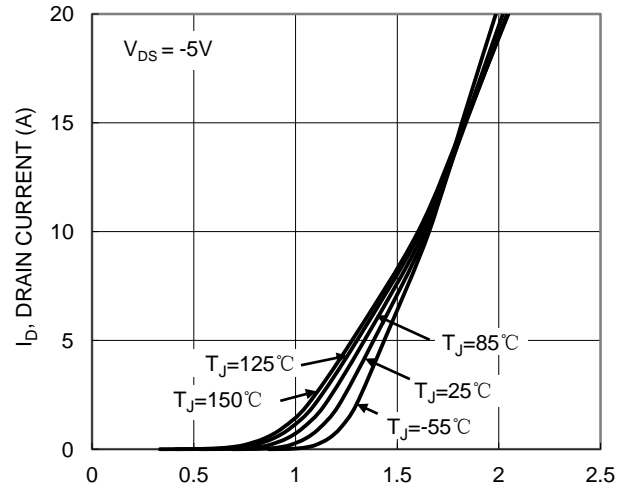
**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>STATIC PARAMETERS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	I <sub>D</sub> = -250µA, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	-1	µA	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
Gate-Body Leakage Current	I <sub>GSS</sub>	—	—	±100	nA	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±8V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	—	-1.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	22 27	45 65	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.5A V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.8A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.7	-1.4	V	I <sub>S</sub> = -2.1A, V <sub>GS</sub> = 0V
<b>DYNAMIC PARAMETERS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	1575	—	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	124	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	89	—	pF	
Gate Resistance	R <sub>g</sub>	—	10	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	15	—	nC	V <sub>DS</sub> = -10V, I <sub>D</sub> = -4.5A
Total Gate Charge (V <sub>GS</sub> = -8V)	Q <sub>g</sub>	—	28	—		
Gate-Source Charge	Q <sub>gs</sub>	—	1.6	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	3.4	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	5.2	—	ns	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A, R <sub>g</sub> = 6.0Ω
Rise Time	t <sub>r</sub>	—	12	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	103	—		
Fall Time	t <sub>f</sub>	—	31	—		
Body Diode Reverse Recovery Time	t <sub>RR</sub>	—	13	—	ns	I <sub>F</sub> = -8.9A, di/dt = -100A/µs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	—	6.7	—	nC	I <sub>F</sub> = -8.9A, di/dt = -100A/µs

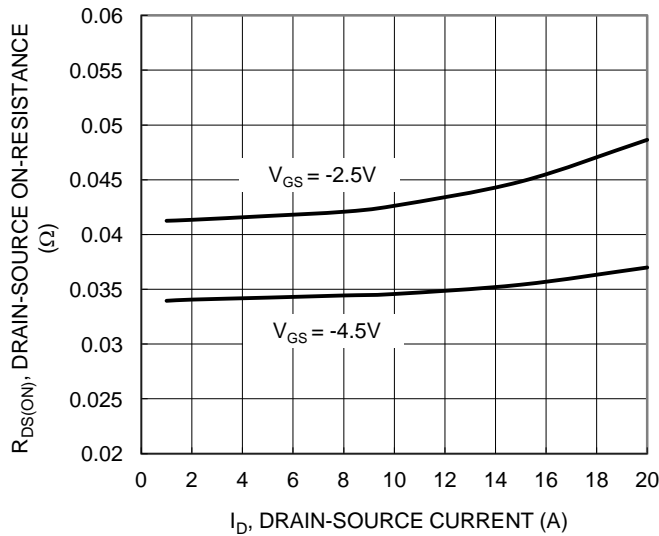
- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  7. Short duration pulse test used to minimize self-heating effect.
  8. Guaranteed by design. Not subject to product testing.



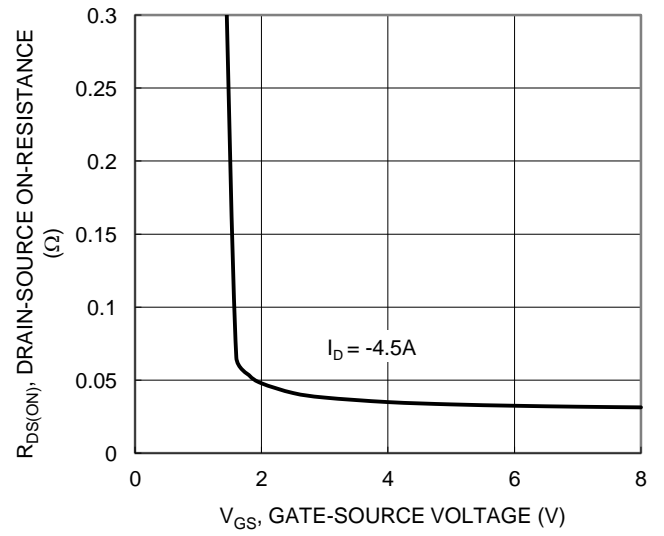
$V_{DS}$ , DRAIN-SOURCE VOLTAGE (V)  
Figure 1. Typical Output Characteristic



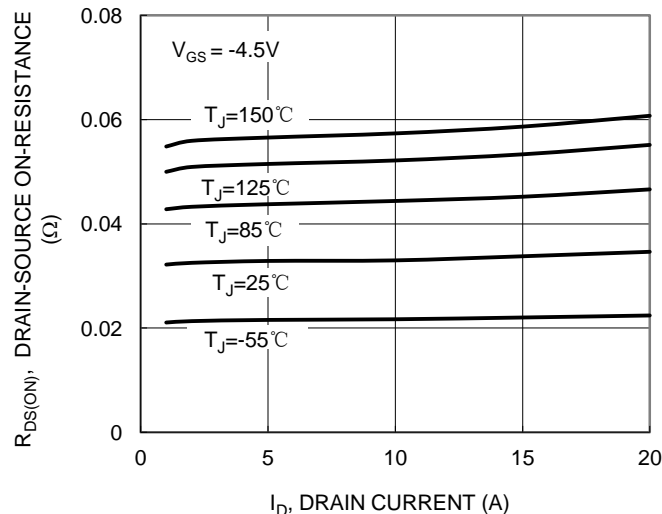
$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 2. Typical Transfer Characteristic



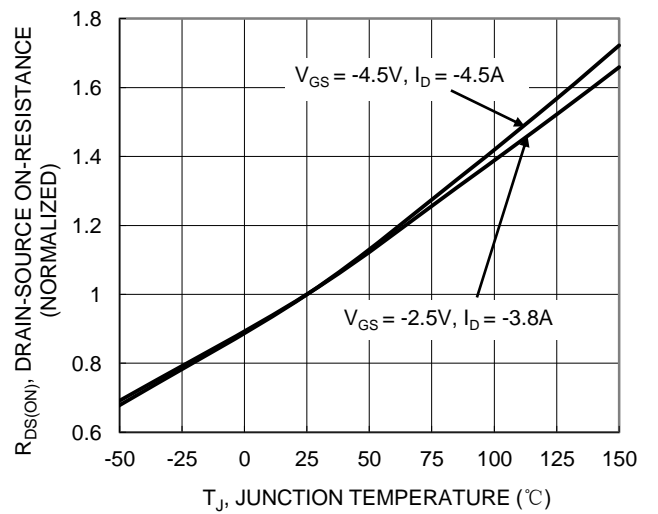
$I_D$ , DRAIN-SOURCE CURRENT (A)  
Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage



$V_{GS}$ , GATE-SOURCE VOLTAGE (V)  
Figure 4. Typical Transfer Characteristic



$I_D$ , DRAIN CURRENT (A)  
Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature



$T_J$ , JUNCTION TEMPERATURE (°C)  
Figure 6. On-Resistance Variation with Junction Temperature

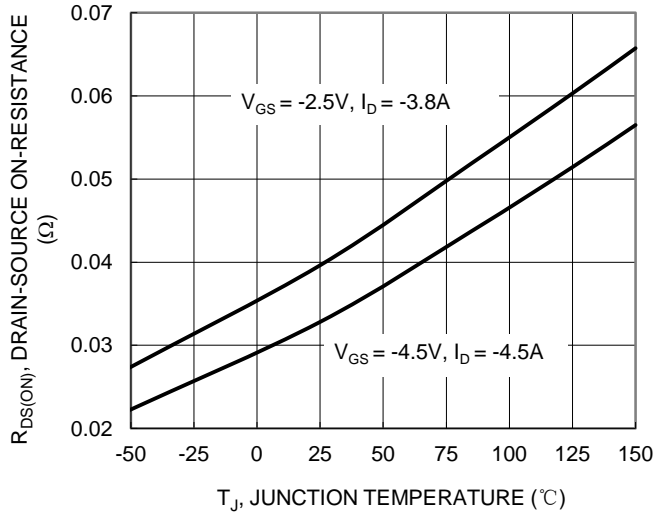


Figure 7. On-Resistance Variation with Junction Temperature

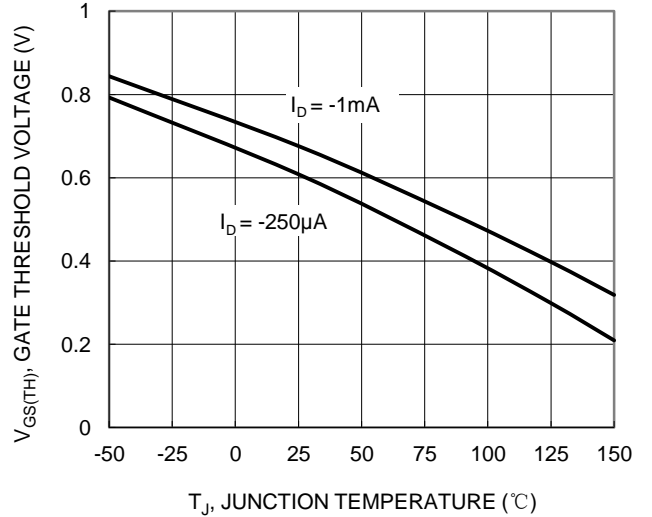


Figure 8. Gate Threshold Variation vs. Junction Temperature

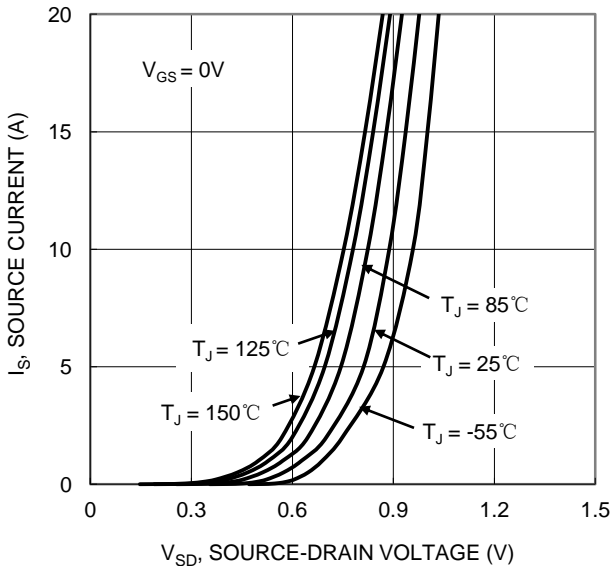


Figure 9. Diode Forward Voltage vs. Current

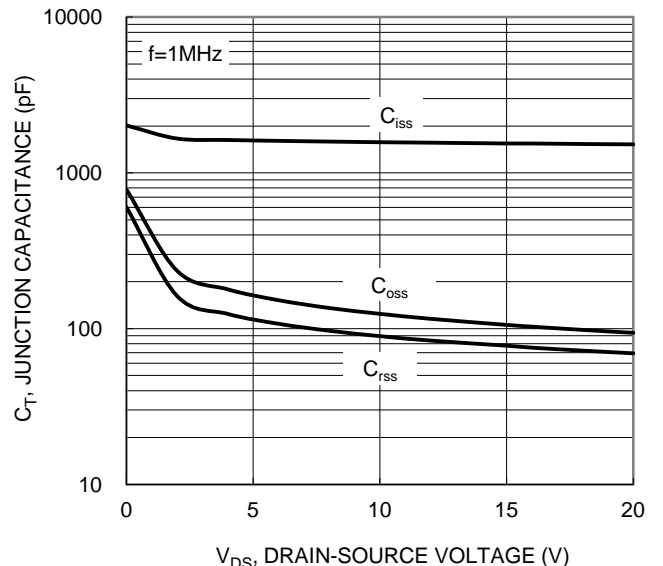


Figure 10. Typical Junction Capacitance

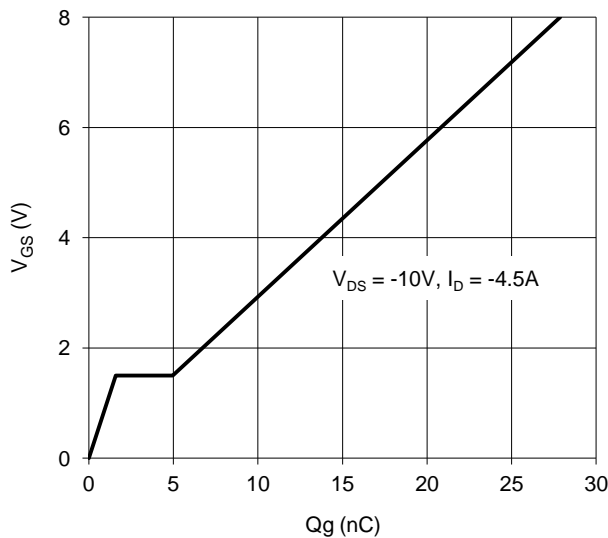


Figure 11. Gate Charge

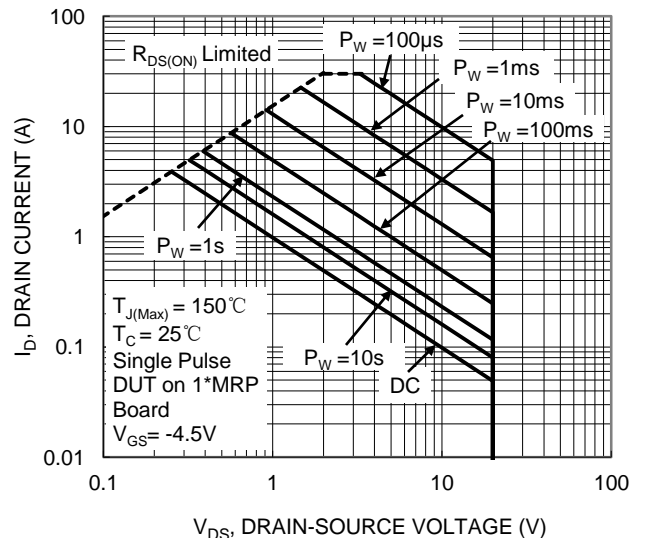


Figure 12. SOA, Safe Operation Area

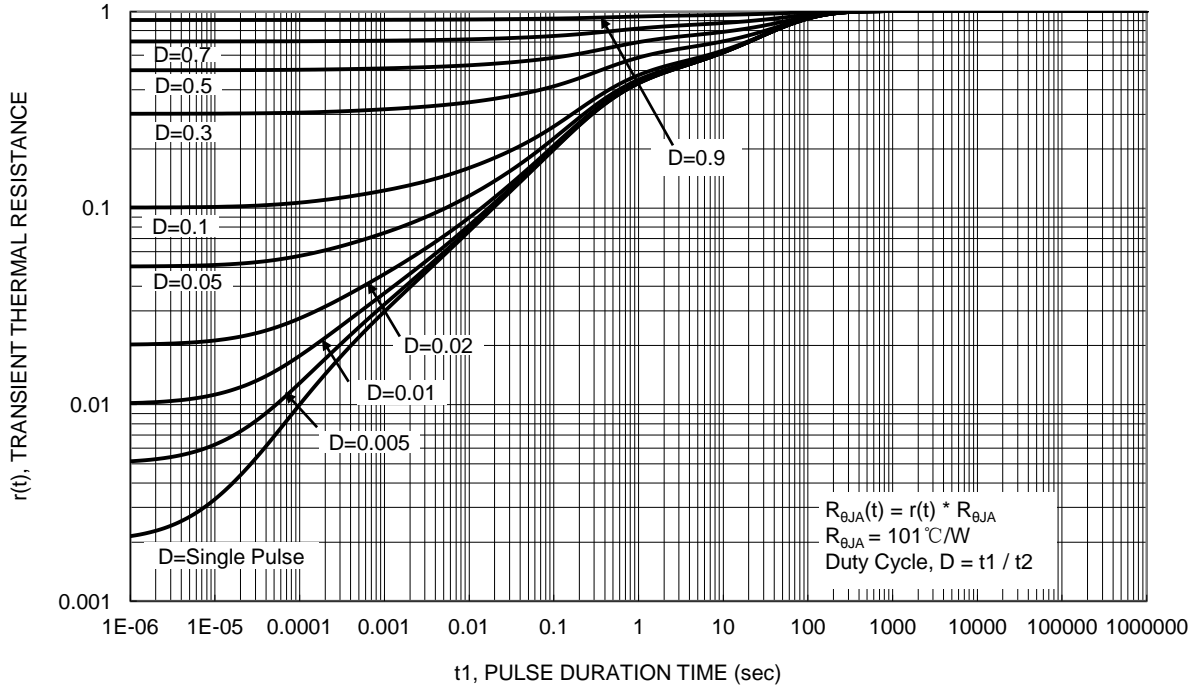
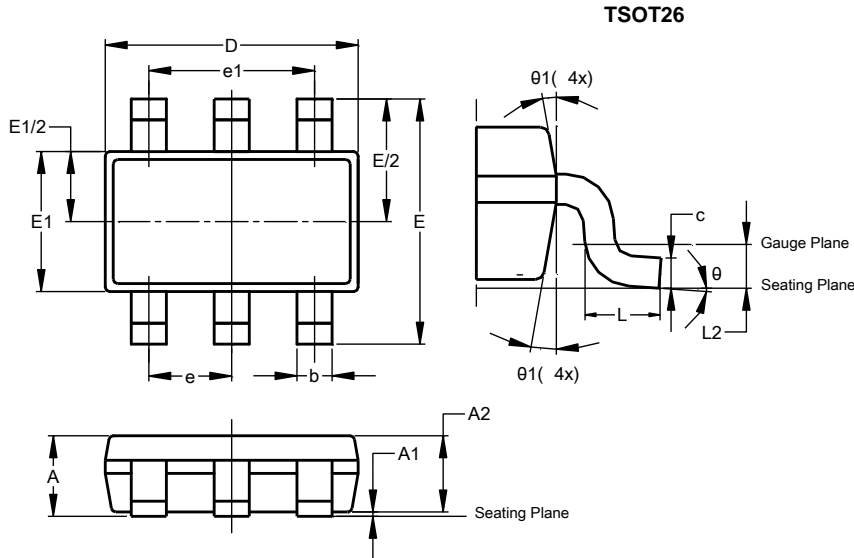


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

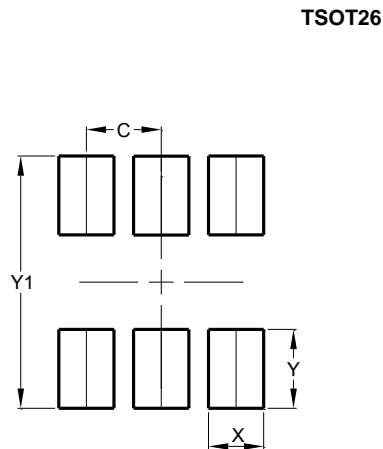
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



TSOT26			
Dim	Min	Max	Typ
A	–	1.00	–
A1	0.010	0.100	–
A2	0.840	0.900	–
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	–
c	0.120	0.200	–
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	–
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	–
<b>All Dimensions in mm</b>			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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