

## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$ Max	$I_D$ Max $T_C = +25^\circ C$
100V	15m $\Omega$ @ $V_{GS} = 10V$	34A
	19.5m $\Omega$ @ $V_{GS} = 6V$	32A

## Description and Applications

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize  $R_{DS(ON)}$  and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Load switch.

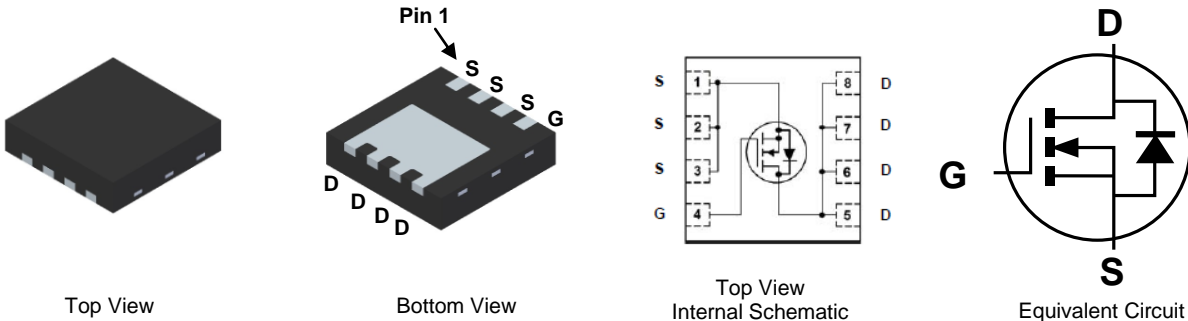
- Backlighting
- Power Management Functions
- DC-DC Converters

## Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- High Conversion Efficiency
- Low  $R_{DS(ON)}$  – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Mechanical Data

- Case: V-DFN3333-8 (Type B)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram  
Terminals: Finish –NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.03 grams (Approximate)

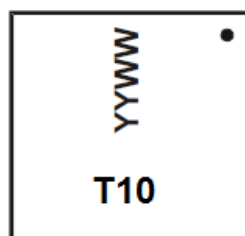


## Ordering Information (Note 4)

Part Number	Case	Packaging
DMT10H015LCG-7	V-DFN3333-8 (Type B)	2,000/Tape & Reel
DMT10H015LCG-13	V-DFN3333-8 (Type B)	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



T10 = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Year (ex: 18 = 2018)  
 WW = Week (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	100	V
Gate-Source Voltage			V <sub>GSS</sub>	±20	V
Continuous Drain Current, V <sub>GS</sub> = 10V (Note 6)	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	9.4	A
		T <sub>A</sub> = +70°C		7.5	
Continuous Drain Current, V <sub>GS</sub> = 10V	Steady State	T <sub>C</sub> = +25°C	I <sub>D</sub>	34	A
		T <sub>C</sub> = +100°C		21	
Maximum Continuous Body Diode Forward Current (Note 6)			I <sub>S</sub>	1.6	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	54	A
Avalanche Current, L = 3mH (Note 8)			I <sub>AS</sub>	7.5	A
Avalanche Energy, L = 3mH (Note 8)			E <sub>AS</sub>	85	mJ

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	1	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	118	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	2.1	W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	59	°C/W
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	4.5	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.4	2	3.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	12.1	15	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A
		—	15	19.5		V <sub>GS</sub> = 6V, I <sub>D</sub> = 20A
		—	18.9	26		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A
Diode Forward Voltage	V <sub>SD</sub>	—	0.9	1.3	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iSS</sub>	—	1871	—	pF	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>oSS</sub>	—	261	—		
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	6.9	—		
Gate Resistance	R <sub>g</sub>	—	0.75	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	33.3	—	nC	V <sub>DD</sub> = 50V, I <sub>D</sub> = 10A, V <sub>GS</sub> = 10V
Gate-Source Charge	Q <sub>gs</sub>	—	6.9	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	5.1	—		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	6.5	—	ns	V <sub>DD</sub> = 50V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A, R <sub>g</sub> = 6Ω
Turn-On Rise Time	t <sub>r</sub>	—	7	—		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	19.7	—		
Turn-Off Fall Time	t <sub>f</sub>	—	8.1	—		
Reverse Recovery Time	t <sub>RR</sub>	—	37.9	—	ns	I <sub>F</sub> = 10A, di/dt = 100A/μs
Reverse Recovery Charge	Q <sub>RR</sub>	—	51.9	—	nC	

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  7. Short duration pulse test used to minimize self-heating effect.
  8. Guaranteed by design. Not subject to product testing.

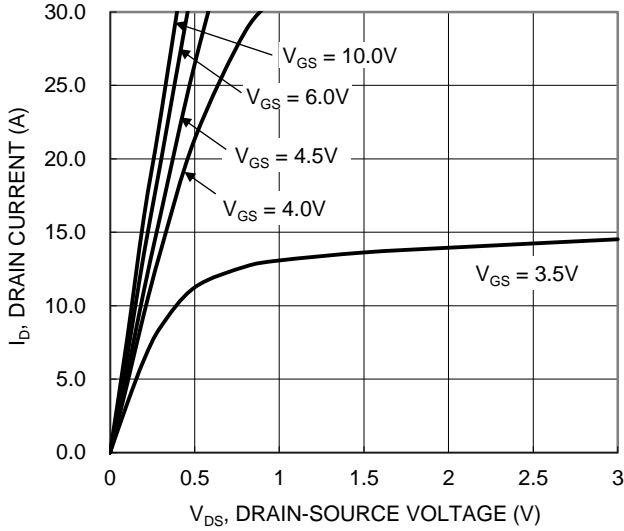


Figure 1. Typical Output Characteristic

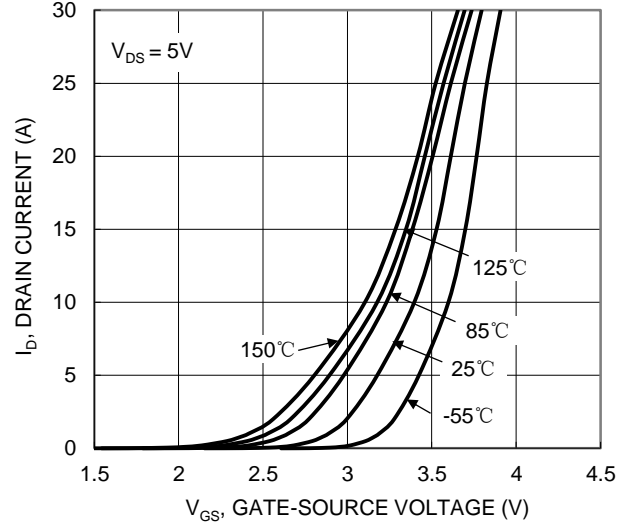


Figure 2. Typical Transfer Characteristic

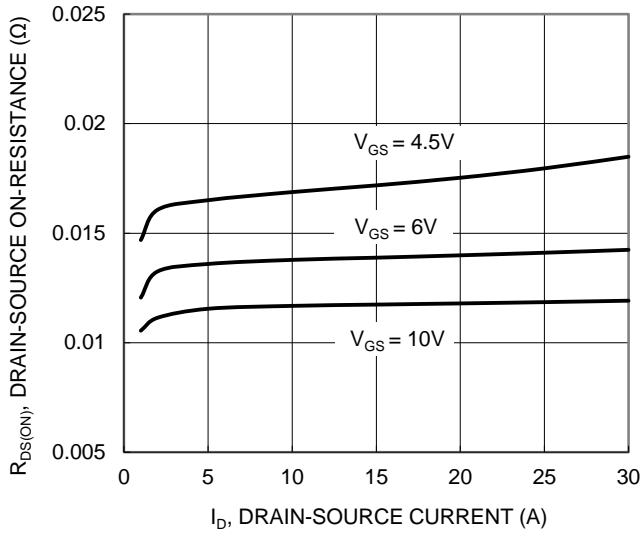


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

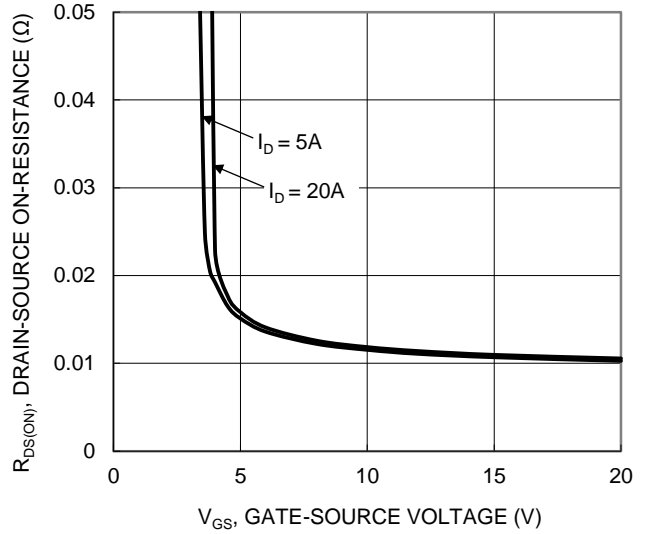


Figure 4. Typical Transfer Characteristic

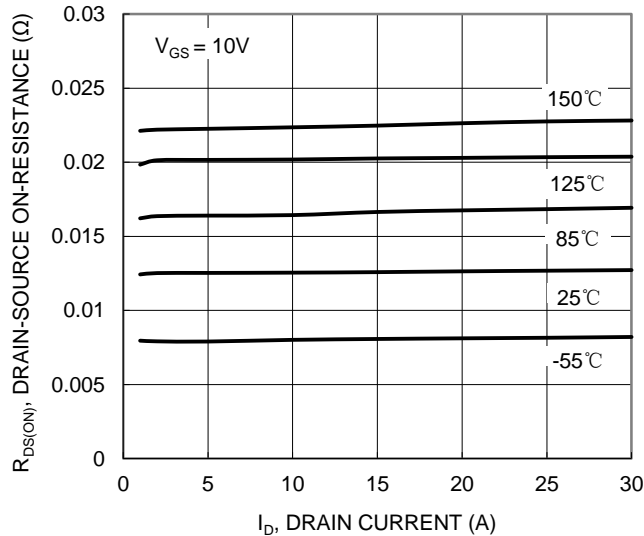


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

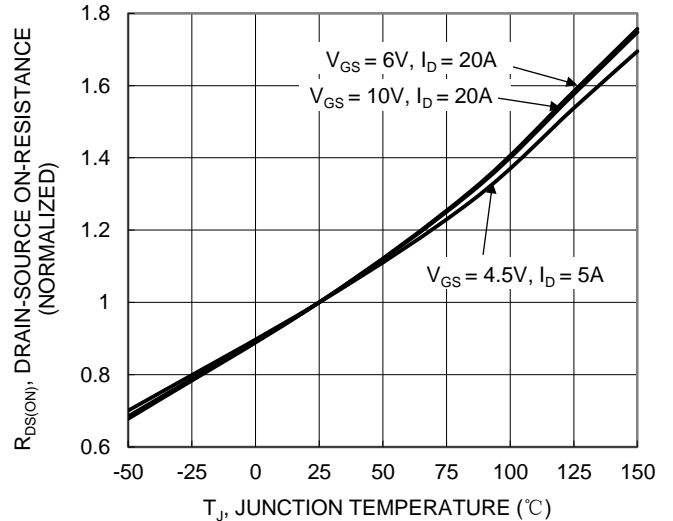


Figure 6. On-Resistance Variation with Junction Temperature

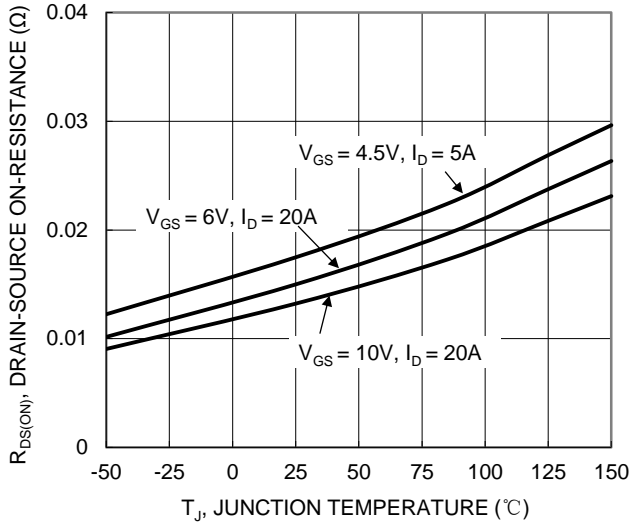


Figure 7. On-Resistance Variation with Junction Temperature

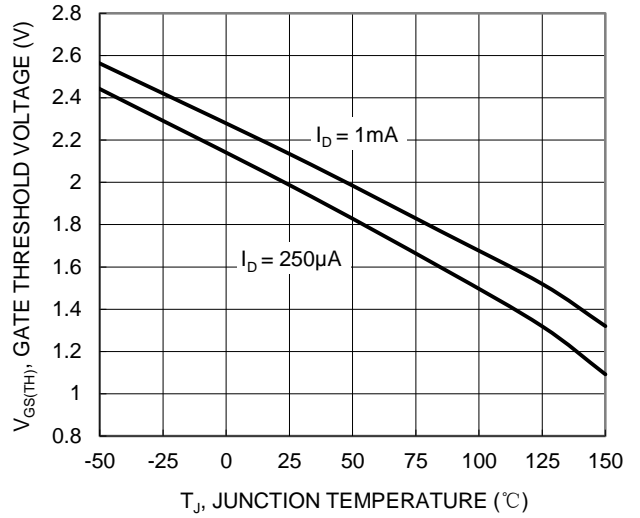


Figure 8. Gate Threshold Variation vs. Junction Temperature

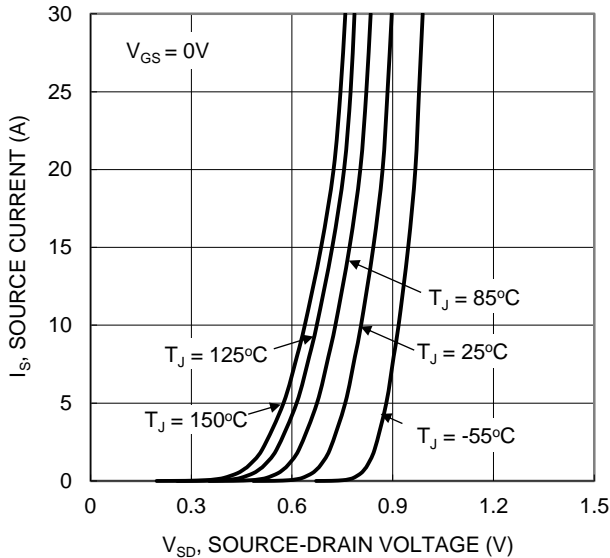


Figure 9. Diode Forward Voltage vs. Current

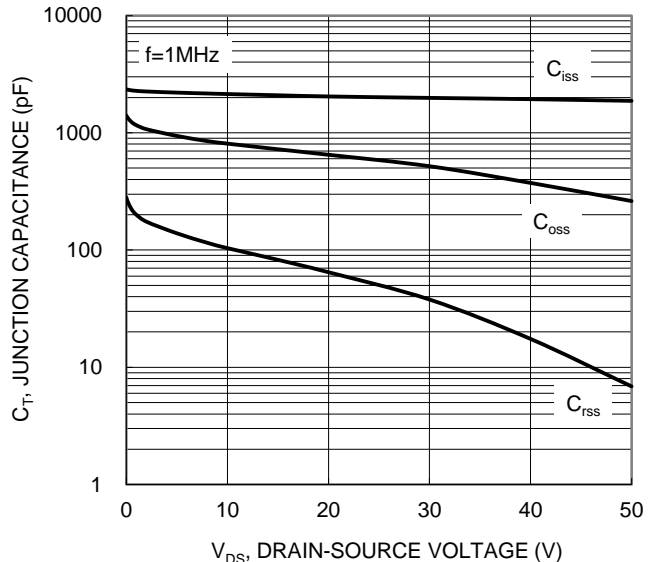


Figure 10. Typical Junction Capacitance

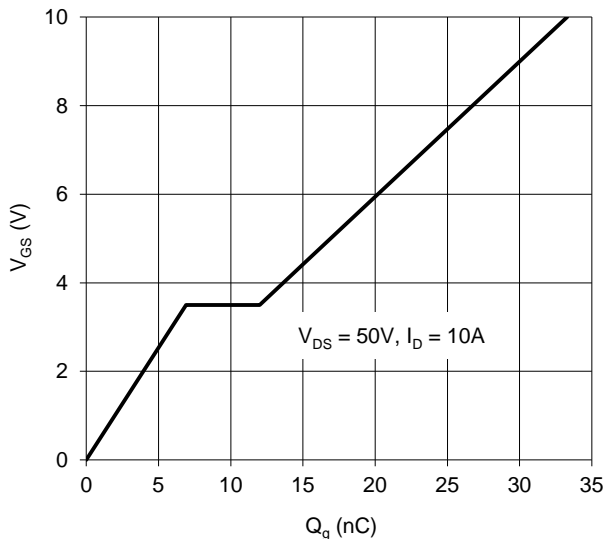


Figure 11. Gate Charge

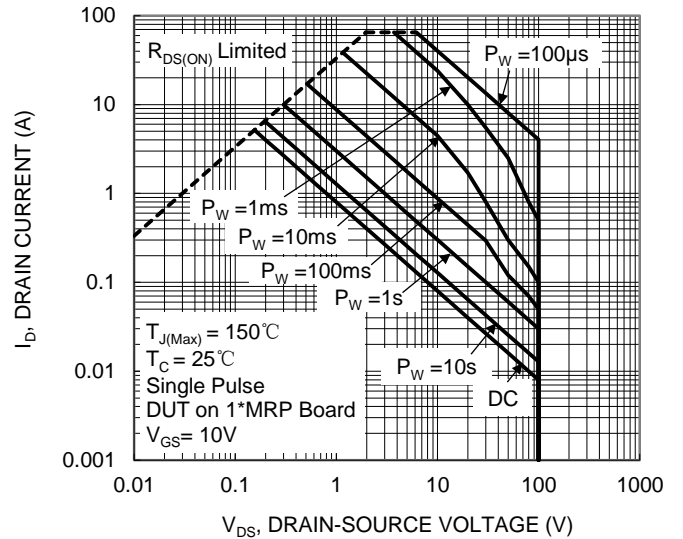


Figure 12. SOA, Safe Operation Area

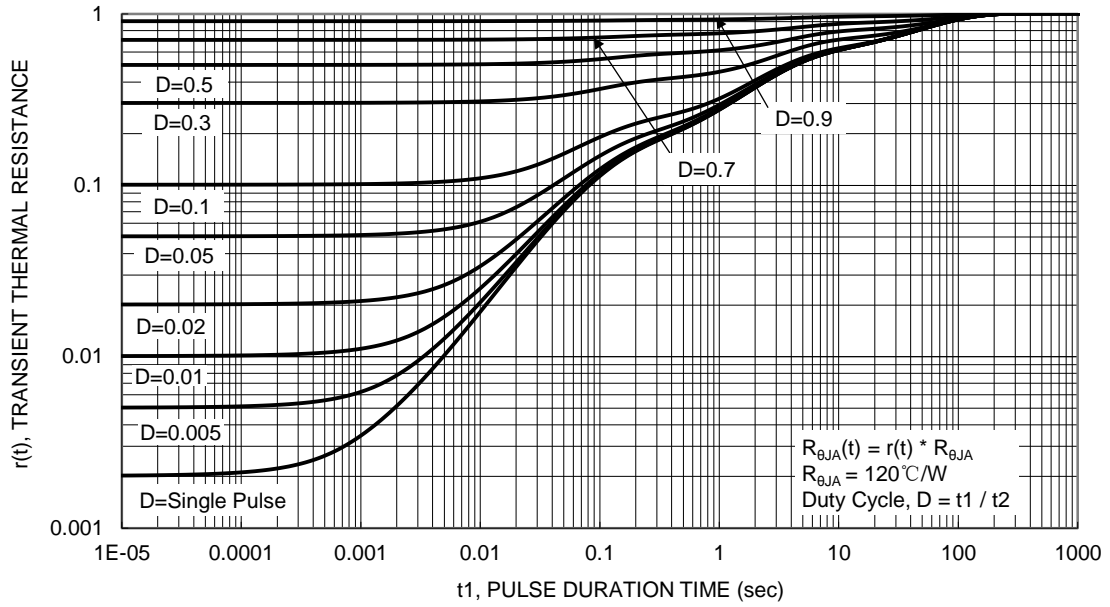
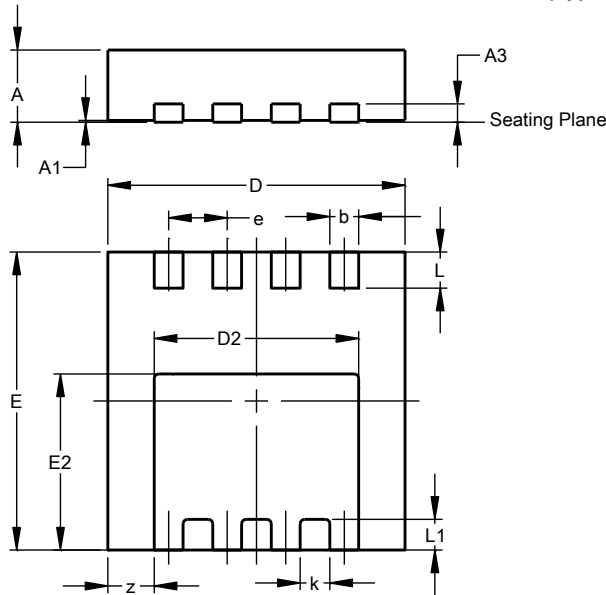


Figure 13. Transient Thermal Resistance

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3333-8 (Type B)

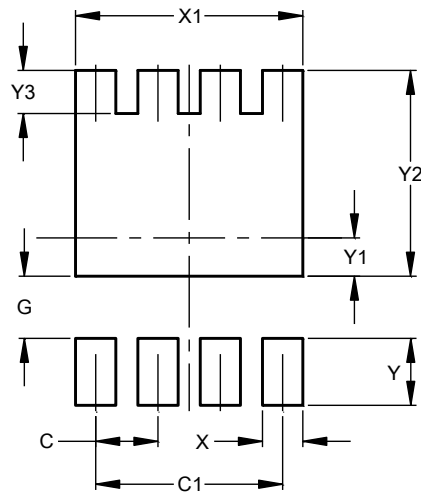


V-DFN3333-8 (Type B)			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	--	--	0.203
b	0.27	0.37	0.32
D	3.25	3.35	3.30
D2	2.17	2.37	2.27
E	3.25	3.35	3.30
E2	1.85	2.05	1.95
e	--	--	0.65
k	--	--	0.33
L	0.35	0.45	0.40
L1	--	--	0.34
z	--	--	0.515
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3333-8 (Type B)



Dimensions	Value (in mm)
C	0.650
C1	1.950
G	0.650
X	0.420
X1	2.370
Y	0.700
Y1	0.400
Y2	2.150
Y3	0.450

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