A Product Line of
Diodes Incorporated

PI6C20800B

PCI Express® 3.0 1:8 HCSL Clock Buffer

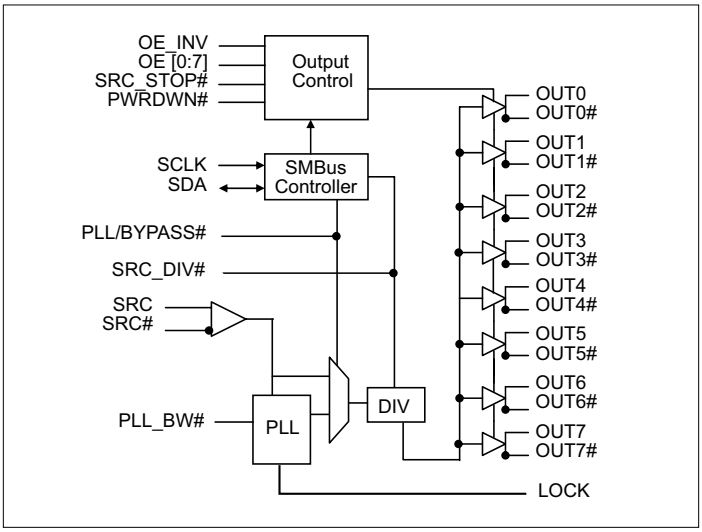
Features

- Phase jitter filter for PCIe 3.0 application
- Eight Pairs of Differential Clocks
- Low skew < 50ps (PI6C20800B), <60ps (PI6C20800BI)
- Low Cycle-to-cycle jitter < 60ps
- Output Enable for all outputs
- Outputs Tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or Fanout operation
- 3.3V Operation
- Industrial Temperature Option - PI6C20800BI
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-Free & Green):
  — 48-Pin TSSOP (A)

Description

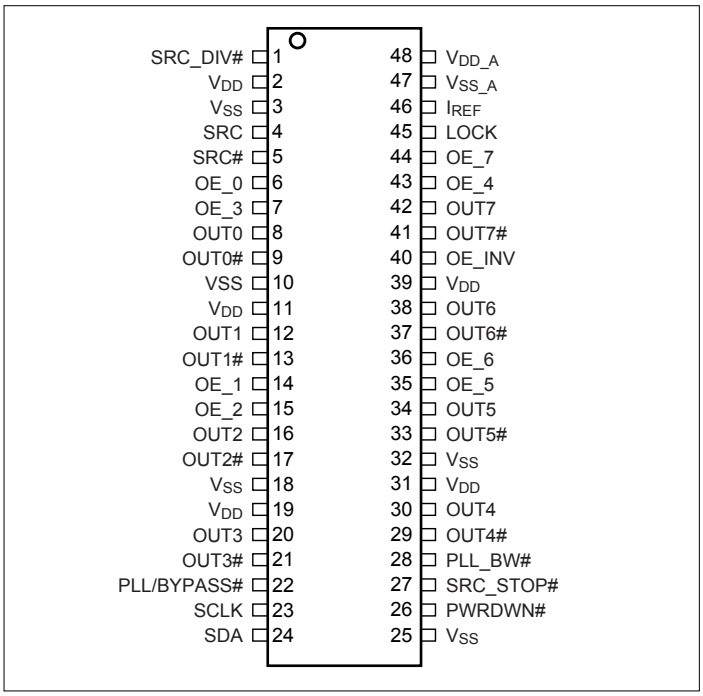
PI6C20800B is a PCIe 3.0 compliant, high-speed, low-noise differential clock buffer designed to be a companion to PCI Express 3.0 clock generator for Intel server chipsets. The device distributes the differential SRC clock from PCIe clock generator to eight differential pairs of clock outputs either with or without PLL. The input SRC clock can be divided by 2 when SRC_DIV# is LOW. The clock outputs are controlled by input selection of SRC_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC_STOP# or PWRDWN# is LOW, the output clocks are Tristated. When PWRDWN# is LOW, the SDA and SCLK inputs must be Tristated.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration (48-Pin TSSOP)



Pin Description

Pin #	Pin Name	Type	Descriptions
1	SRC_DIV#	Input	3.3V LVTTL input for selecting input frequency divide by 2, active LOW.
4, 5	SRC & SRC#	Input	0.7V Differential SRC input from PI6C410 clock synthesizer
6, 7, 14, 15, 35, 36, 43, 44	OE [0:7]	Input	3.3V LVTTL input for enabling outputs, active HIGH.
40	OE_INV	Input	3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE[0:7], SRC_STOP#, PWRDWN# inverted.
8, 9, 12, 13, 16 17, 20, 21, 29, 30, 33, 34, 37, 38, 41, 42	OUT[0:7] & OUT[0:7]#	Output	0.7V Differential outputs
22	PLL/BYPASS#	Input	3.3V LVTTL input for selecting fan-out of PLL operation.
23	SCLK	Input	SMBus compatible SCLOCK input
24	SDA	I/O	SMBus compatible SDATA
46	I_{REF}	Input	External resistor connection to set the differential output current
27	SRC_STOP#	Input	3.3V LVTTL input for SRC stop, active LOW
28	PLL_BW#	Input	3.3V LVTTL input for selecting the PLL bandwidth
26	PWRDWN#	Input	3.3V LVTTL input for Power Down operation, active LOW

Pin Description Cont.

Pin #	Pin Name	Type	Descriptions
45	LOCK	Output	3.3V LVTTL output, transition high when PLL lock is achieved (Latched output)
2, 11, 19, 31, 39	V_{DD}	Power	3.3V Power Supply for Outputs
3, 10, 18, 25, 32	V_{SS}	Ground	Ground for Outputs
47	V_{SS_A}	Ground	Ground for PLL
48	V_{DD_A}	Power	3.3V Power Supply for PLL

Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

Data Write Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1	8 bits	1	1 bit
Start bit	Slave Addr	W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte Offset	Ack	Data Byte N - 1	Ack	Stop bit

Note: Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Read Protocol

1 bit	7 bits	1	1	8 bits	1	1	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1	1 bit
Start bit	Slave Addr	W	Ack	Register offset	Ack	Repeat Start	Slave Addr	R	Ack	Byte Count = N	Ack	Data Byte Offset	Ack	Data Byte N - 1	Not Ack	Stop bit

Note: Register offset for indicating the starting register for indexed block write and indexed block read.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	SRC_DIV# 0 = Divide by 2 1 = Normal	RW	1 = x1	OUT[0:7], OUT[0:7]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:7], OUT[0:7]#	NA
2	PLL Bandwidth 0 = HIGH Bandwidth, 1 = LOW Bandwidth	RW	1 = Low	OUT[0:7], OUT[0:7]#	NA
3	RESERVED				
4	RESERVED				
5	RESERVED				
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:7], OUT[0:7]#	NA

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	OUTPUTS enable 1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT0, OUT0#	NA
1		RW	1 = Enabled	OUT1, OUT1#	NA
2		RW	1 = Enabled	OUT2, OUT2#	NA
3		RW	1 = Enabled	OUT3, OUT3#	NA
4		RW	1 = Enabled	OUT4, OUT4#	NA
5		RW	1 = Enabled	OUT5, OUT5#	NA
6		RW	1 = Enabled	OUT6, OUT6#	NA
7		RW	1 = Enabled	OUT7, OUT7#	NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT0, OUT0#	NA
1		RW	0 = Free running	OUT1, OUT1#	NA
2		RW	0 = Free running	OUT2, OUT2#	NA
3		RW	0 = Free running	OUT3, OUT3#	NA
4		RW	0 = Free running	OUT4, OUT4#	NA
5		RW	0 = Free running	OUT5, OUT5#	NA
6		RW	0 = Free running	OUT6, OUT6#	NA
7		RW	0 = Free running	OUT7, OUT7#	NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	RESERVED	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

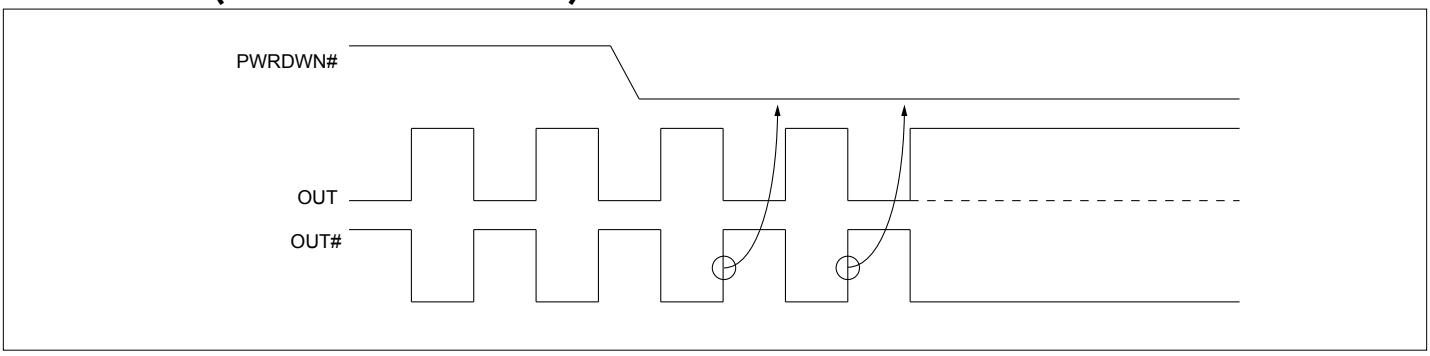
Data Byte 4: Pericom ID Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

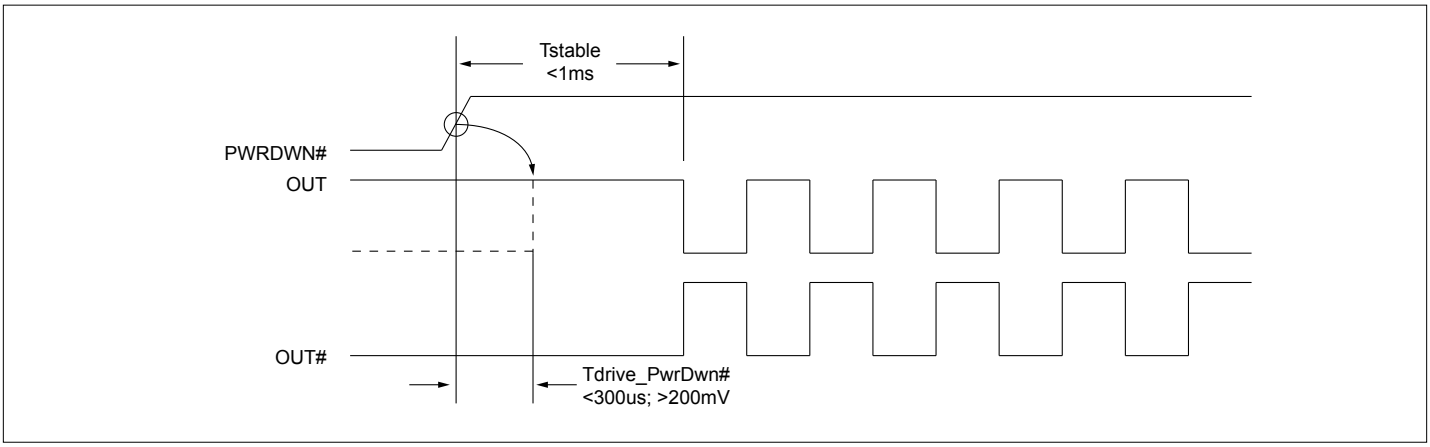
Functionality

PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	$I_{REF} \times 2$ or Float	LOW	0	$I_{REF} \times 6$ or Float	LOW

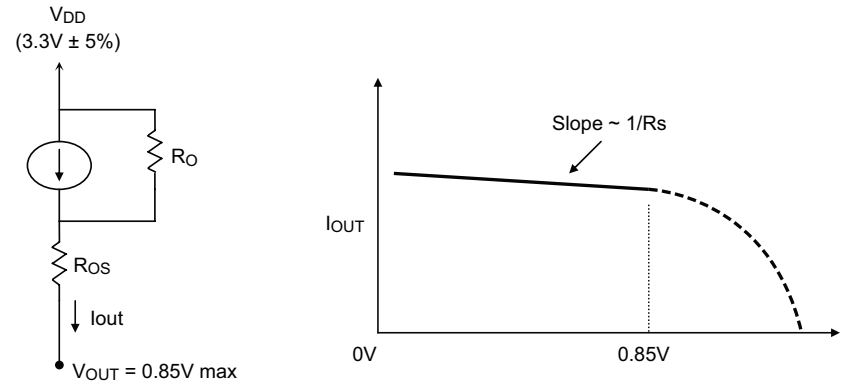
Power Down (PWRDWN# Assertion)



Power Down (PWRDWN# De-assertion)



Current-mode Output Buffer Characteristics of OUT[0:7], OUT[0:7]#



Differential Clock Buffer Characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	V_{DD} = 3.30 ±5%	R_{REF} = 475Ω 1% I_{REF} = 2.32mA	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note: $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3xRr)	Output Current	V_{OH} @ Z
100Ω (100Ω differential ≈ 15% coupling ratio)	R_{REF} = 475Ω 1%, I_{REF} = 2.32mA	I_{OH} = 6 x I_{REF}	0.7V @ 50

Absolute Maximum Ratings[1] (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input HIGH Voltage		4.6	
V_{IL}	Input LOW Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V
T_J	Junction Temperature		125	°C

Note:

1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics (VDD = 3.3±5%, VDD_A = 3.3±5%)

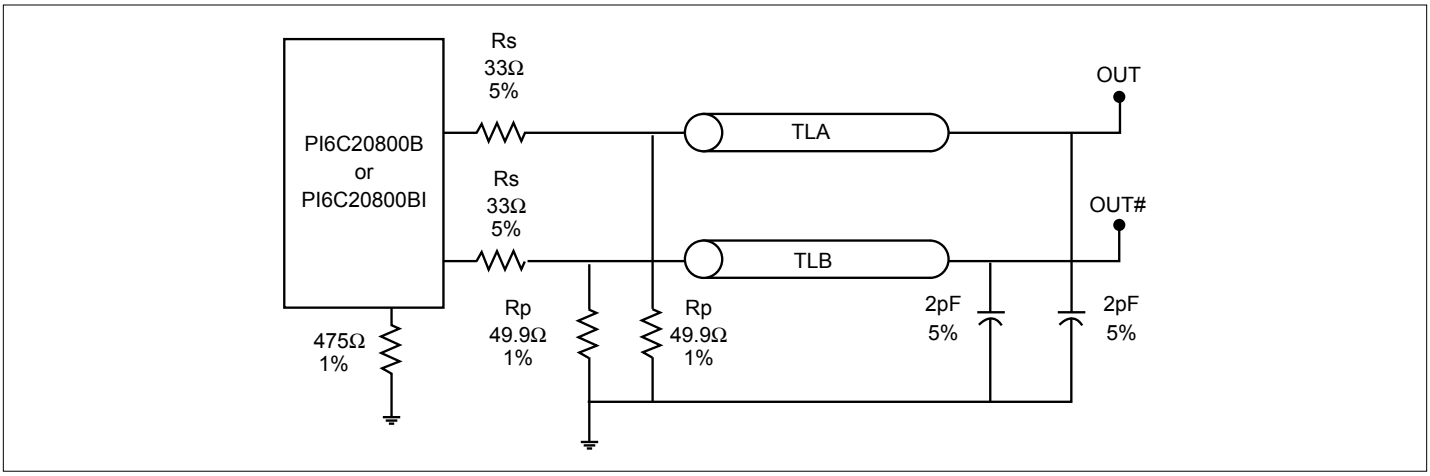
Symbol	Parameters	Condition	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V_{IH}	3.3V Input HIGH Voltage		2.0	V_{DD} + 0.3	
V_{IL}	3.3V Input LOW Voltage		V_{SS} – 0.3	0.8	
I_{IK}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	µA
V_{OH}	3.3V Output HIGH Voltage	I_{OH} = -1mA	2.4		V
V_{OL}	3.3V Output LOW Voltage	I_{OL} = 1mA		0.4	
I_{OH}	Output HIGH Current	$I_{OH} = 6 \times I_{REF}$,	12.2		mA
		I_{REF} = 2.32mA		15.6	
C_{IN}	Logic Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	
L_{PIN}	Pin Inductance			7	nH
I_{DD}	Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 100MHz		250	mA
I_{SS}	Power Down Current	Driven outputs		80	
I_{SS}	Power Down Current	Tristate outputs		12	
T_A	Ambient Temperature	Commercial (PI6C20800B)	0	70	°C
		Industrial (PI6C20800BI)	-40	85	

AC Switching Characteristics[1,2,3] (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

Symbol	Parameters			Min.	Typ.	Max.	Units	Notes
F_{in}	SRC/SRC# Input Frequency PLL Mode			95		105	MHz	6
	SRC/SRC# Input Frequency Bypass Mode			95		400	MHz	6
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)			175		700	ps	2
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation					125		2
T_{pd}	Input to Output Propagation Delay	PLL Mode	PI6C20800B	-250		250	ps	
			PI6C20800BI	-450		450		
		Bypass Mode	PI6C20800B	-7.5		7.5	ns	
			PI6C20800BI	-8		8		
T_{skew}	Output-to-Output Skew (PI6C20800B)					50	ps	3
	Output-to-Output Skew (PI6C20800BI)					65		3
V_{HIGH}	Voltage HIGH (Measured at 100MHz @ 3.3V)			600		900	mV	2
V_{OVS}	Max. Voltage					1150		
V_{UDS}	Min. Voltage			-300				
V_{LOW}	Voltage LOW			-150		+150		2
V_{cross}	Absolute crossing point voltages			250		550		2
ΔV_{cross}	Total Variation of V_{cross} over all edges					140		2
T_{DC}	Duty Cycle (Measured at 100 MHz)			45		55	%	3
$T_{jcyc-cyc}$	Jitter, Cycle-to-cycle (PLL Mode, Measurement for differential waveform)					60	ps	4
	Jitter, Cycle-to-cycle (BYPASS mode as additive jitter)							
J_{add}	Additive RMS phase jitter for PCIe 2.0			<0		1	ps	5
J_{add}	RMS phase jitter for PCIe 3.0	PLL L-BW @ 2M & 5M 1st H3			1.115	3	ps	
		PLL L-BW @ 2M & 4M 1st H3			1.211	3		
		PLL L-BW @ 2M & 5M 1st H3			1.116	3		
		PLL L-BW @ 2M & 4M 1st H3			1.425	3		
		PLL H-BW @ 2M & 5M 1st H3			0.646	1		
		PLL H-BW @ 2M & 4M 1st H3			0.644	1		
		PLL H-BW @ 2M & 5M 1st H3			0.646	1		
		PLL H-BW @ 2M & 4M 1st H3			0.579	1		

Notes:
1. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measured using M1 timing analyzer from Amherst.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($J_{add} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)
6. –0.5% downnspread input

Configuration Test Load Board Termination

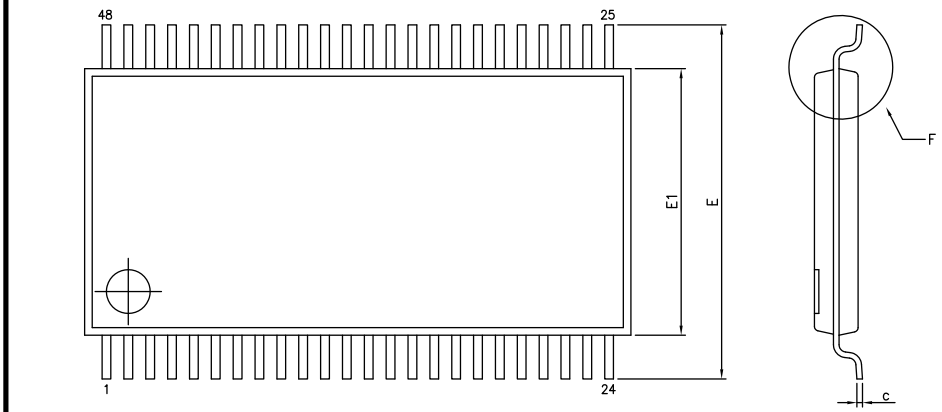


Part Marking

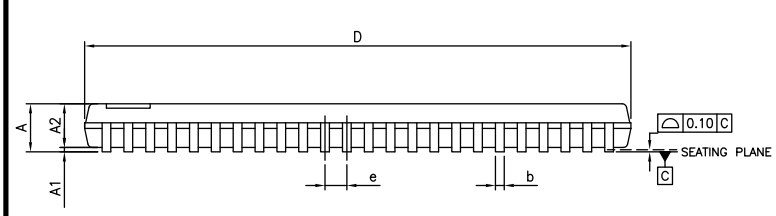
Y: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

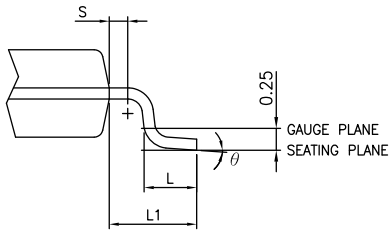
Y: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 48-TSSOP (A)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.17	–	0.27
c	0.09	–	0.20
D	12.40	12.50	12.60
E1	6.00	6.10	6.20
E	7.90	8.10	8.30
e		0.50 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





DETAIL F

Notes:
1. Controlling Dimension in Millimeters. Angle in Degrees.
2. Refer JEDEC MO–153F
3. Package Outline Exclusive of Mold Flash and Metal Burr.

PERICOM Enabling Serial Connectivity

DATE: 03/30/16

DESCRIPTION: 48-Pin, 240mil Wide TSSOP

PACKAGE CODE: A (A48)

DOCUMENT CONTROL #: PD-1501 REVISION: H

16-0065

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI6C20800BAEX	A	48-pin, 240mil Wide (TSSOP)
PI6C20800BIAEX	A	48-pin, 240mil Wide (TSSOP) (Industrial)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES ("DIODES") MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

www.diodes.com

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)