PI6LC48S04

HiFlex Serial Interface Clock

Features

- Selectable 250MHz, 156.25MHz, 125MHz or 100MHz output clock synthesized from a 25MHz fundamental mode crystal
- Four differential clock outputs (two LVDS and two low power HCSL outputs)
- Crystal interface designed for 25MHz, parallel resonant crystal
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1MHz - 20MHz): 0.21ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz - 20MHz): 0.32ps (typical)
- Power supply noise rejection PSNR: -50dB (typical)
- LVCMOS interface levels for the frequency select input
- Full 3.3V or 2.5V supply voltage
- Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

Description

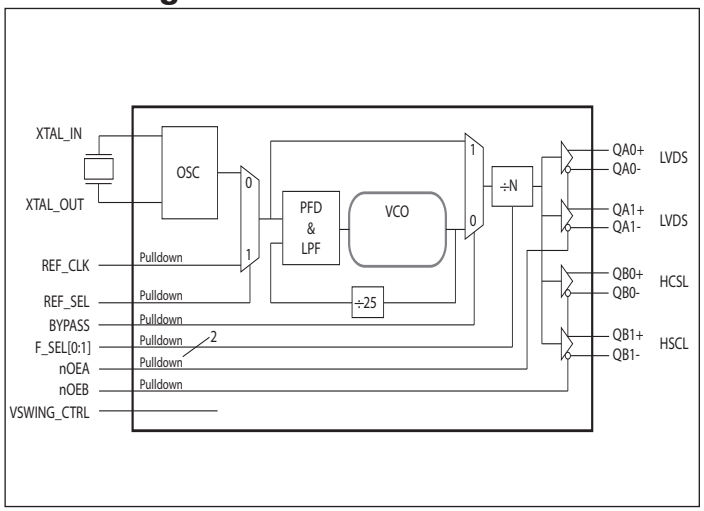
The PI6LC48S04 is a 4-output clock synthesizer designed for serial reference clock applications. The device generates four copies of a selectable 250MHz, 156.25MHz, 125MHz or 100MHz clock signal with 0.34ps phase jitter performance. The four outputs are organized in two banks of two LVDS and two low power HCSL ouputs.The device supports 3.3V and 2.5V voltage supplies and is packaged in a small 32-lead TQFN package.

Function Table

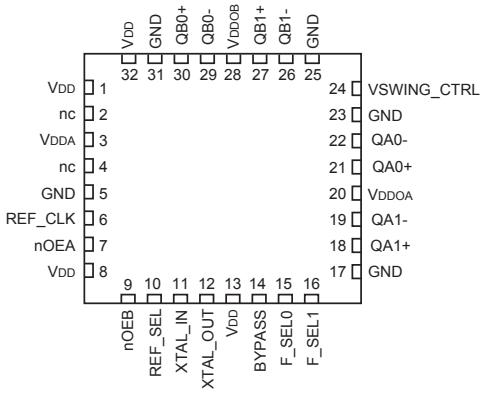
Inputs		Output Frequency with f_{XTAL} = 25MHz
F_SEL [1]	F_SEL [0]	
0 (default)	0 (default)	156.25MHz
0	1	125MHz
1	0	100MHz
1	1	250MHz

Note: F_SEL[1:0] are asynchronous controls.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1, 8, 13, 32	V_{DD}	Power		Core supply pins.
2, 4	nc	Unused		No connect.
3	V_{DDA}	Power		Analog power supply.
5, 17, 23, 25, 31	GND	Power		Power supply ground.
6	REF_CLK	Input	Pulldown	Alternative single-ended reference clock input. LVCMOS/LVTTL interface levels.
7	nOEA	Input	Pulldown	Output enable input. See Table 3D for function. LVCMOS/LVTTL interface levels.
9	nOEB	Input	Pulldown	Output enable input. See Table 3E for function. LVCMOS/LVTTL interface levels.
10	REF_SEL	Input	Pulldown	Reference select input. See Table 3B for function. LVCMOS/LVTTL interface levels.
11, 12	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
14	BYPASS	Input	Pulldown	Bypass mode select pin. See Table 3C for function. LVCMOS/LVTTL interface levels.
15, 16	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
18, 19	QA1+, QA1-	Output		Differential clock output. LVDS interface levels.
20	V_{DDOA}	Power		Output supply pin for QAx outputs.
21, 22	QA0+, QA0-	Output		Differential clock output. LVDS interface levels.
24	VSWING_CTRL	Input	Pull up and Pull-down	VOH selection pin for low power HCSL outputs. Tri-level selction for different voltage swings.
26, 27	QB1-, QB1+	Output		Differential clock output. Low power HCSL interface levels.
28	V_{DDOB}	Power		Output supply pin for QBx outputs.
29, 30	QB0-, QB0+	Output		Differential clock output. Low power HCSL interface levels.

NOTE: Pulldown refers to intetrnal input resistors.

Pin Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
CIN	Input Capacitance			4		pF
RPULLDOWN	Input Pulldown Resistor			100		kΩ

Function Table

Output Divider and Output Frequency

Inputs		Operation	f_{OUT} with f_{REF} = 25MHz
F_SEL [1]	F_SEL [0]		
0 (default)	0 (default)	$f_{OUT} = f_{REF} * 25 \div 4$	156.25MHz
0	1	$f_{OUT} = f_{REF} * 5$	125MHz
1	0	$f_{OUT} = f_{REF} * 4$	100MHz
1	1	$f_{OUT} = f_{REF} * 10$	250MHz

Note: F_SEL[1:0] are asynchronous controls.

PLL Reference Clock Select Fuction Table

Input	
REF_SEL	Operation
0 (default)	The crystal interface is selected as reference clock
1	The REF_CLK input is selected as reference clock

NOTE: REF_SEL is an asynchronous control.

PLL BYPASS Function Table

Input	
BYPASS	Operation
0 (default)	PLL is enabled. The reference frequency is multiplied by the PLL feedback divider of 25 and then divided by the selected output divider N.
1	PLL is bypassed. The reference frequency is divided by the selected output divider N. AC specifications do not apply in PLL bypass mode.

NOTE: BYPASS is an asynchronous control.

nOEA Output Enable Function Table

Input	
nOEA	Operation
0 (default)	QA0+, QA0- and QA1+, QA1- outputs are enabled
1	QA0+, QA0- and QA1+, QA1- outputs are disabled (high-impedance)

NOTE: nOEA is an asynchronous control.

nOEB Output Enable Function Table

Input	
nOEB	Operation
0 (default)	QB0+, QB0- and QB1+, QB1- outputs are enabled
1	QB0+, QB0- and QB1+, QB1- outputs are disabled (high-impedance)

NOTE: nOEB is an asynchronous control.

Table 3: VSWING_CTRL Select Table

VSWING_CTRL	**Output Amplitude (V)**
0	0.63
Open (default)	0.75
1	0.87

Maximum Ratings

Supply Voltage, $V_{DD,}$ $V_{DDA,}$ V_{DDOx} 4.6V
Inputs ..... -0.5V to V_{DD} + 0.5V
Storage Temperature, T_{STG} ..... -65°C to 150°C
Inputs (Referenced to GND) .....-0.5 to VDD+0.5V
Clock Output (Referenced to GND) ..... -0.5 to 2V
Latch up ..... .200mA
ESD Protection (Input).....2000 V min (HBM)

Note:

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

Power Supply DC Characteristics (VDD = VDDOA = VDDOB = 3.3V±5% or 2.5V±5%, TA = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDA}	Output Supply Voltage		V_{DD} – 0.30	3.3	V_{DD}	V
			V_{DD} – 0.30	2.5	V_{DD}	V
$V_{DDOA\&B}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DDA}	Analog Supply Current				30	mA
I_{DD}	Power Supply Current				25	mA
$I_{DDOA\&B}$	Output Supply Current				72	mA

LVCMOS/LVTTL Input DC Characteristics (VDD = VDDOA = VDDOB = 3.3V±5% or 2.5V±5%, TA = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
		VSWING_CTRL @ V_{DD}= 3.3V and 2.5V	V_{DD} x 0.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 2.5V	-0.3		0.7	V
		VSWING_CTRL @ V_{DD}= 3.3V and 2.5V	GND - 0.3		V_{DD} x 0.3	V
I_{IH}	Input High Current	nOEA, nOEB, BYPASS, REF_SEL, REF_CLK, F_SEL[1:0] V_{DD} = V_{IN} = 2.625V or 3.465V			150	µA
		VSWING_CTRL with V_{IN} = V_{DD}			150	µA
I_{IL}	Input Low Current	nOEA, nOEB, BYPASS, REF_SEL, REF_CLK, F_SEL[1:0] V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-5			µA
		VSWING_CTRL with V_{IN} = 0V	-150			µA

LVDS DC Characteristics (VDD = VDDOA = 3.3V ± 5% or 2.5V ± 5%, TA = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Crystal Characteristics

Parameter	Test Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency		F_SEL [1:0] = 00		156.25		MHz
			F_SEL [1:0] = 01		125		MHz
			F_SEL [1:0] = 10		100		MHz
			F_SEL [1:0] = 11		250		MHz
f_{REF}	Reference Frequency		REF_CLK		25		MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1		156.25MHz, Integration Range: 1MHz – 20MHz		0.21		ps
			156.25MHz, Integration Range: 12kHz – 20MHz		0.32		ps
			125MHz, Integration Range: 1MHz – 20MHz		0.21		ps
			125MHz,Integration Range: 12kHz – 20MHz		0.32		ps
Φ_N	Single-Side Band Noise Power		156.25MHz, Offset: 100Hz		-91.6		dBc/Hz
			156.25MHz, Offset: 1kHz		-120.8		dBc/Hz
			156.25MHz, Offset: 10kHz		-132.2		dBc/Hz
			156.25MHz, Offset: 100kHz		-135.0		dBc/Hz
PSNR	Power Supply Noise Rejection		From DC to 50MHz		-50		dB
tsk(o)	Output Skew	NOTE 2, 3	Between QAx+/QAx- & QBx+/QBx-		1.8	2.7	ns
tsk(b)	Bank Skew	NOTE 3, 4				55	ps
tR / tF	Output Rise/Fall Time	QAx+, QAx-	20% to 80%	100		400	ps
t_{LOCK}	PLL Lock Time					20	ms
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	QBx+, QBx-		-100		100	mV
t_{STABLE}	Time before VRB is Allowed; NOTE 5, 6	QBx+, QBx-		500			ps
V_{MAX}	Absolute Maximum Output Voltage; NOTE 7, 8	QBx+, QBx-				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 7, 9	QBx+, QBx-		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	QBx+, QBx-		250		550	mV
ΔV_{CROSS}	Total Variation of VCROSS over all edges; NOTE 7, 10, 12	QBx+, QBx-				140	mV
	Rise/Fall Edge Rate; NOTE 5, 13	QBx+, QBx-	Measured between -150mV to 150mV	0.6		5.5	V/ns
odc	Output Duty Cycle			47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized using a 25MHz crystal.

NOTE 1: Please refer to the phase noise plots.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the VRB ±100mV differential range.

NOTE 7: Measurement taken from single ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ.

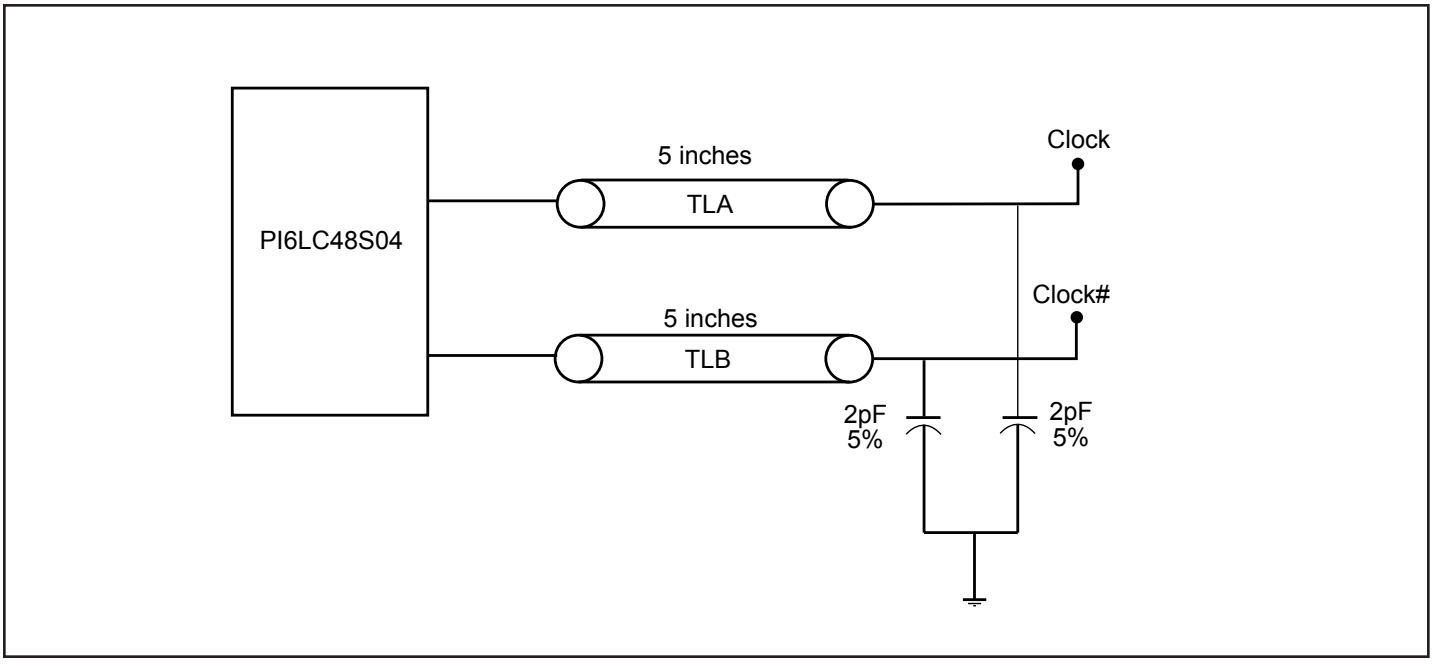
See Parameter Measurement Information Section.

NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 12: Defined as the total variation of all crossing voltage of rising Q and falling nQ. This is the maximum allowed variance in the VCROSS for any particular system. See Parameter Measurement Information Section.

NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

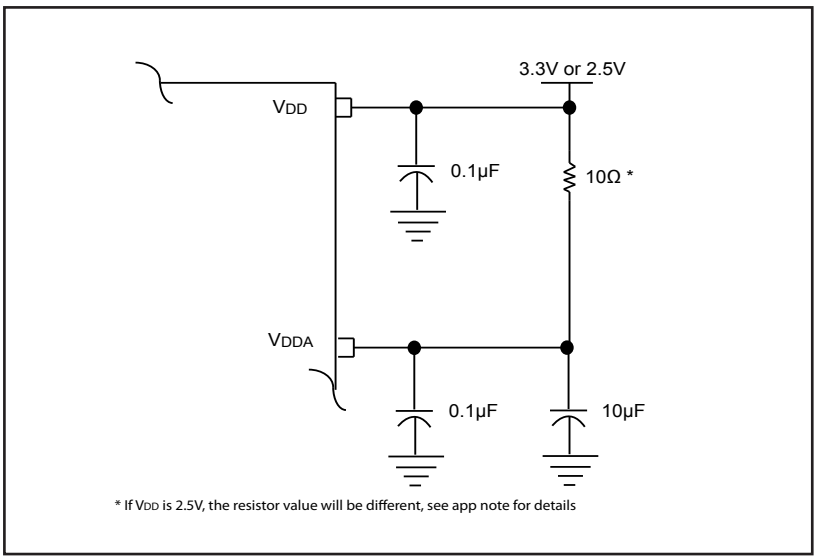
Configuration test load board termination for low power HCSL Outputs



Configuration Test Load Board Termination

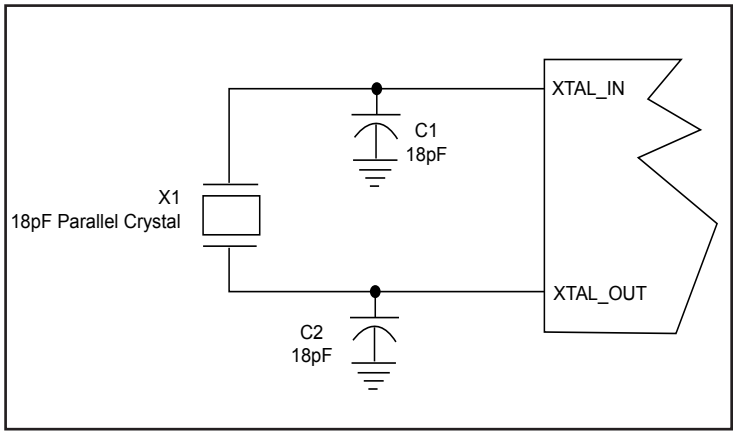
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48S04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



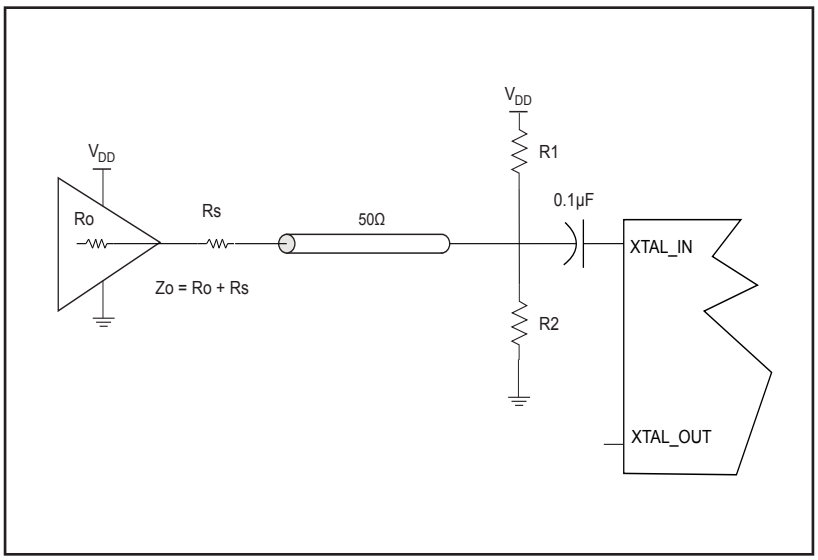
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



LVCMOS to XTAL Interface

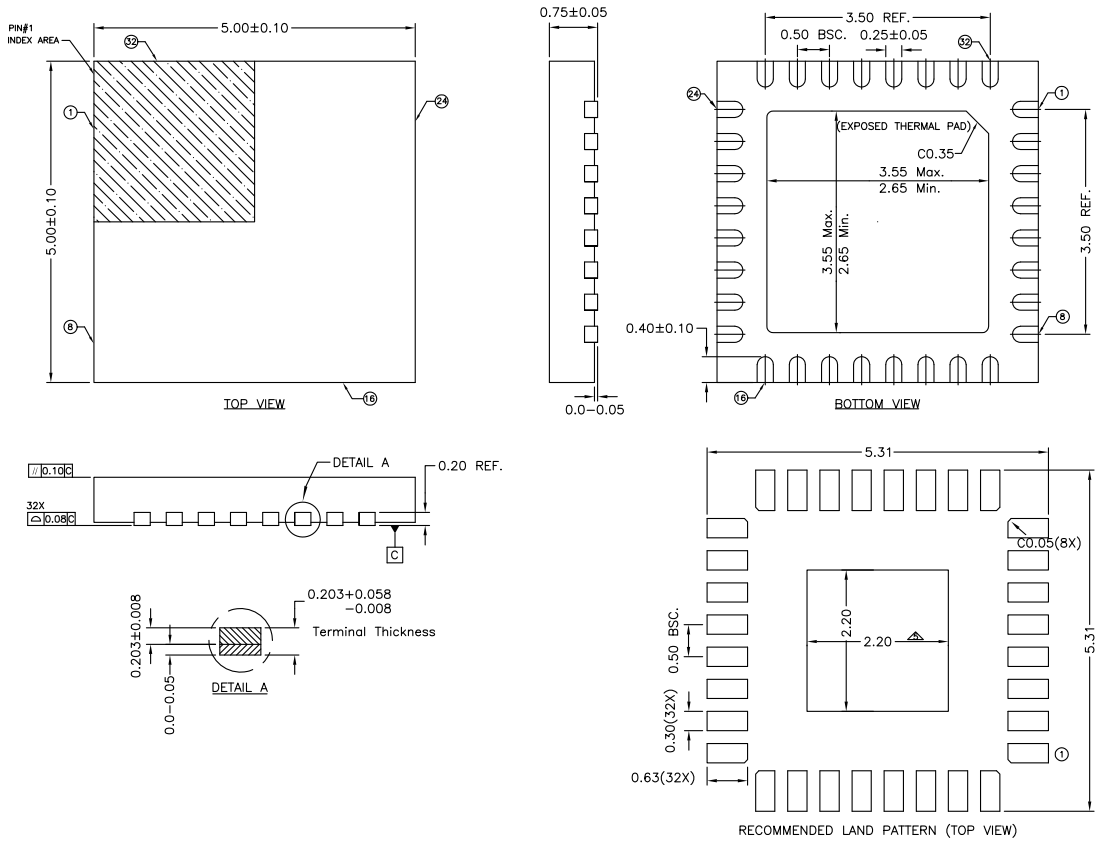
The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



Thermal Information

Symbol	Description	
Θ_{JA}	Junction-to-ambient thermal resistance	44.7 °C/W
Θ_{JC}	Junction-to-case thermal resistance	21.7°C/W

Packaging Mechanical:



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencile design is recommended)

PERICOM Enabling Serial Connectivity — **DATE: 06/30/11**

DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH32

DOCUMENT CONTROL #: PD-2070 — **REVISION: B**

Ordering Information

Ordering Code	Package Code	Package Type
PI6LC48S04ZHIE	ZH	Pb-free & Green, 32-pin TQFN
PI6LC48S04ZHIEX	ZH	Pb-free & Green, 32-pin TQFN, Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. "E" denotes Pb-free and Green
3. Adding an "X" at the end of the ordering code denotes tape and Reel packaging

单击下面可查看定价，库存，交付和生命周期等信息

>>Diodes Incorporated(达迩科技（美台）)