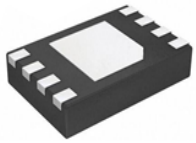
Ultra low-power 2Kbit 4Kbit 8Kbit 16Kbit Serial I2C Page EEPROM EV24C02A EV24C04A EV24C08A EV24C16A



Description:

The EV24C02A/EV24C04A/EV24C08A/EV24C16A series stands as an exceptional range of EEPROM storage solutions, offering up to 16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) to meet a diverse array of application needs. Each word comprises 256/512/1024/2048 bits, ensuring efficient data management and seamless integration.

For enhanced efficiency, this series is engineered to operate seamlessly in demanding environments, delivering high-speed data transfer and low power consumption. Its compact design and flexible pin configuration enhance system integration, making it suitable for space-constrained applications.

The EV24C02A/EV24C04A/EV24C08A/EV24C16A series represents the pinnacle of EVASH engineering prowess, boasting robust construction, advanced features, and unparalleled reliability. This series provides engineers with innovative solutions that redefine possibilities for data storage and management.

Key Features:

High-Capacity Storage: Offers a range of storage options from 2K bits to 16K bits, catering to diverse storage needs across various applications.

High-Speed Operation: Supports operation speeds of up to 1 MHz, ensuring rapid data read and write operations to enhance system responsiveness and performance.

Flexible Read Modes: Supports both random and sequential read modes, ensuring flexibility and convenience in data access to meet the requirements of different application scenarios.

Fast Write Operations: Byte write and page write operations can be completed within 3 milliseconds, ensuring efficient and speedy data programming.

Partial Page Writes: Provides partial page write functionality, effectively utilizing storage space and improving system efficiency.

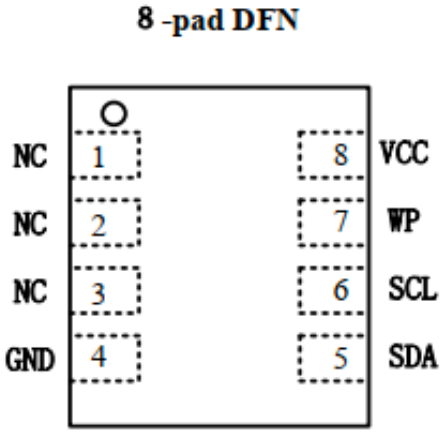
Hardware Data Protection: Incorporates a write protect pin to provide hardware-level security for data, preventing unauthorized write operations.

High Reliability: Undergoes rigorous testing, supporting up to 1 million write cycles and retaining data for up to 100 years, ensuring long-term system stability.

Enhanced ESD/Latch-Up Protection: Offers enhanced ESD protection of up to 8000V, minimizing the risk of damage from electrostatic discharge and ensuring device reliability and stability.

UDFN Packages: Available in compact UDFN packages, suitable for various space-constrained design requirements, enhancing product flexibility and deployability.

Pin Configuration



Pin Descriptions

Pin Name	Type	Functions
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
Vcc	P	Power Supply

Table 1

Block Diagram

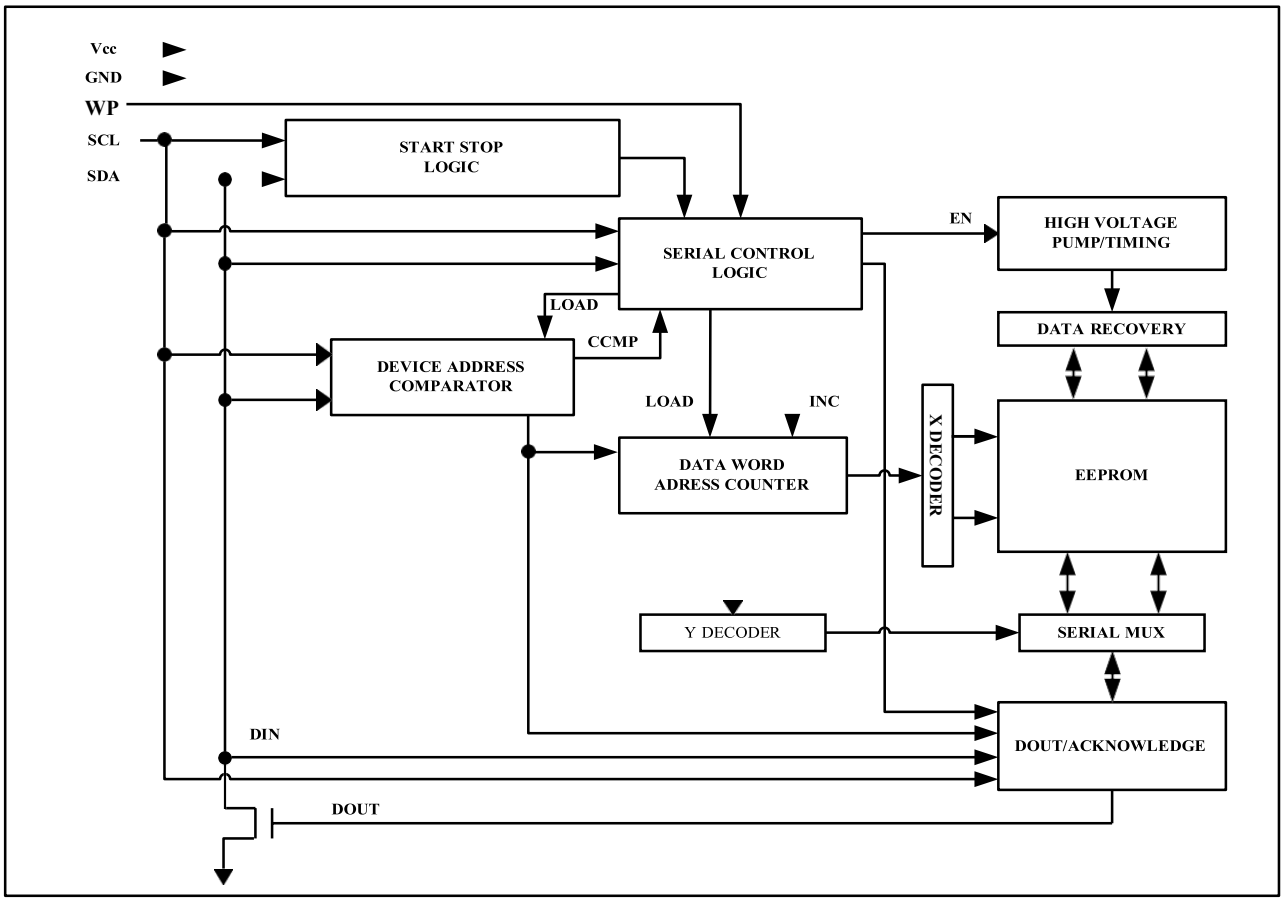


Figure 1

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The EV24C02A/EV24C04A/EV24C08A/EV24C16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following **Table 2**.

WP Pin Status	EV24C02A/EV24C02A/EV24C08A/EV24C16A
At VCC	Full Array
At GND	Normal Read/Write Operations

Table 2

Functional Description

1. Memory Organization

EV24C02A, 2K SERIAL EEPROM: Internally organized with 16 pages of 16 bytes each, the 2K requires an 8-bit data word address for random word addressing.

EV24C04A, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

EV24C08A, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

EV24C16A, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

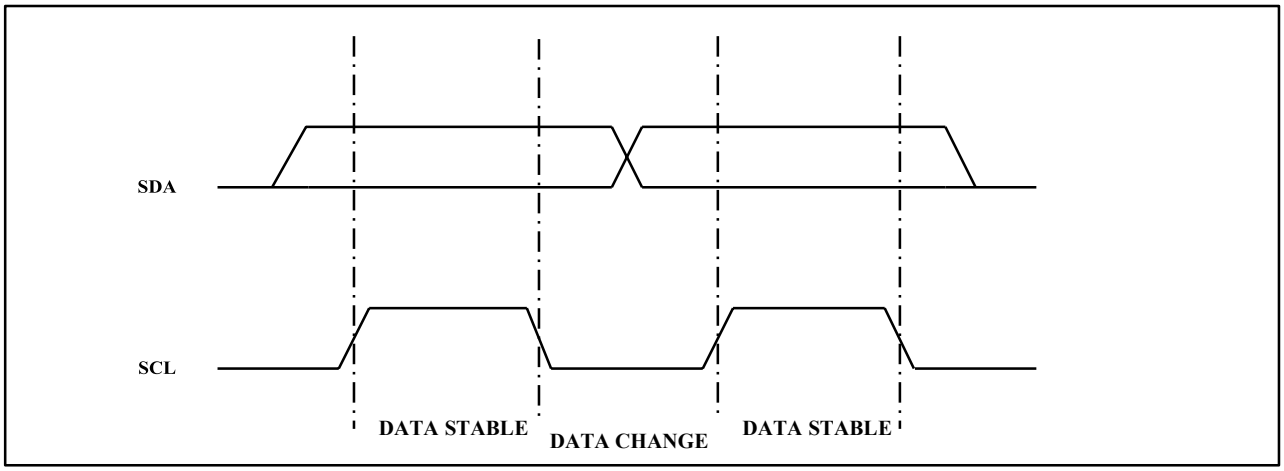


Figure 2. Data Validity

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The EV24C02A/EV24C04A/EV24C08A/EV24C16A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

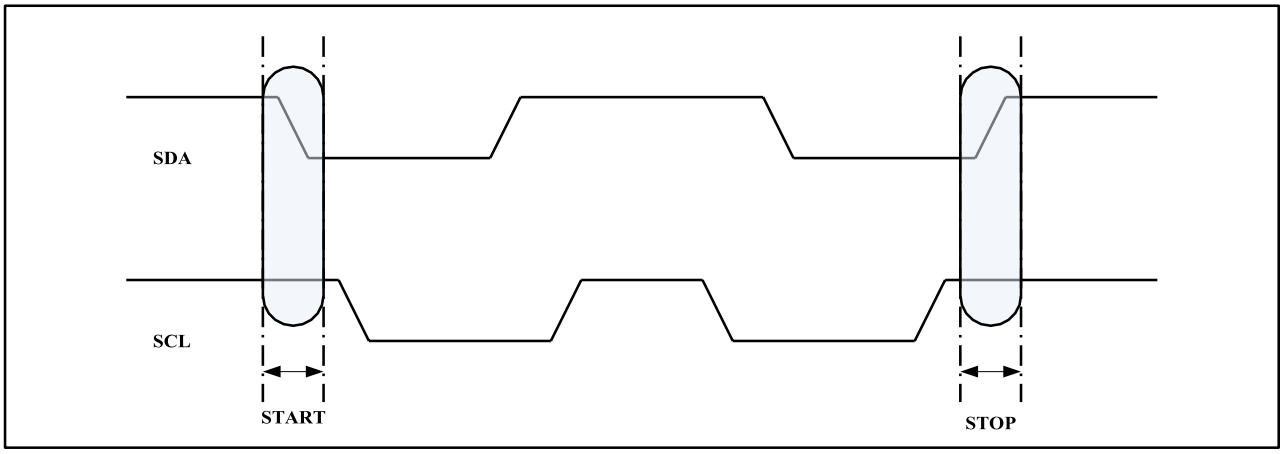


Figure 3. Start and Stop Definition

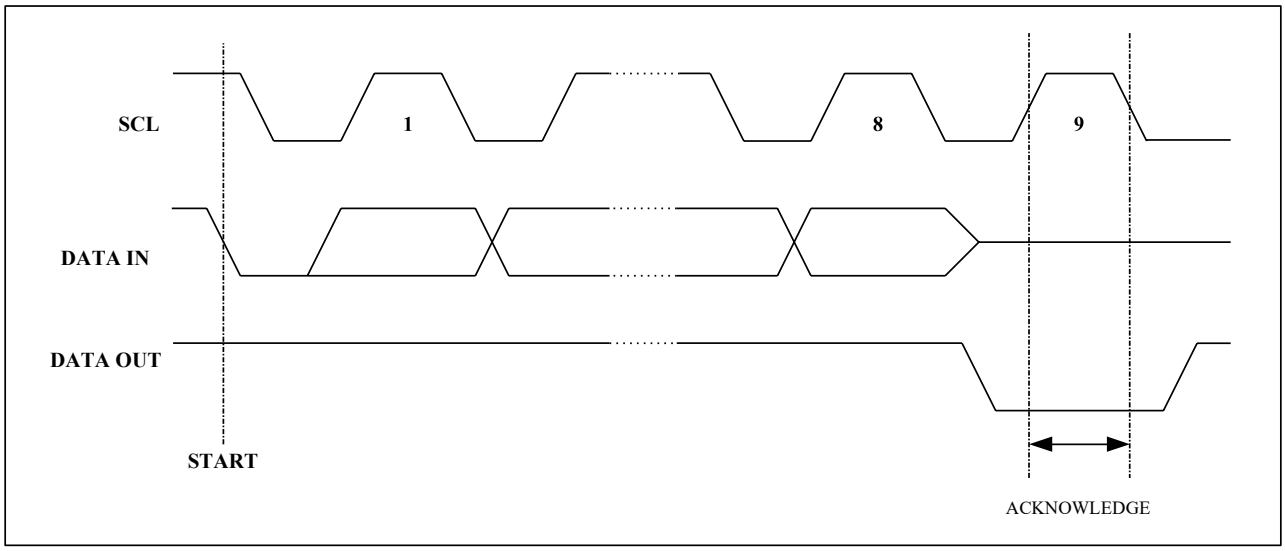


Figure 4. Output Acknowledge

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Lock SDA high in each cycle while SCL is high.
3. Create a start condition.

3. Device Addressing

The 2K/4K/8K/16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are fixed to zero for the 2K EEPROM.

For the 4K EEPROM, the next two bits are fixed to zero and the third bit being a memory page address bit.

For the 8K EEPROM, the next one bit is fixed to zero and the next 2 bits being for memory page addressing.

The 16K does not use any device address bits but instead the 3 bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

	MSB							LSB
2K	1	0	1	0	A2	A1	A0	R/W
4K	1	0	1	0	A2	A1	B8	R/W
8K	1	0	1	0	A2	B9	B8	R/W
16K	1	0	1	0	B10	B9	B8	R/W

Figure 5. Device Address

4. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).

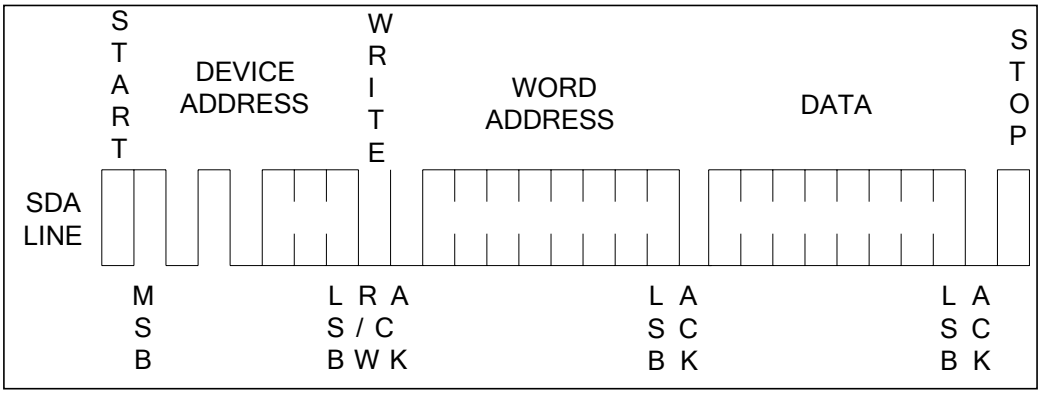


Figure 6. Byte Write

PAGE WRITE: A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 7**).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

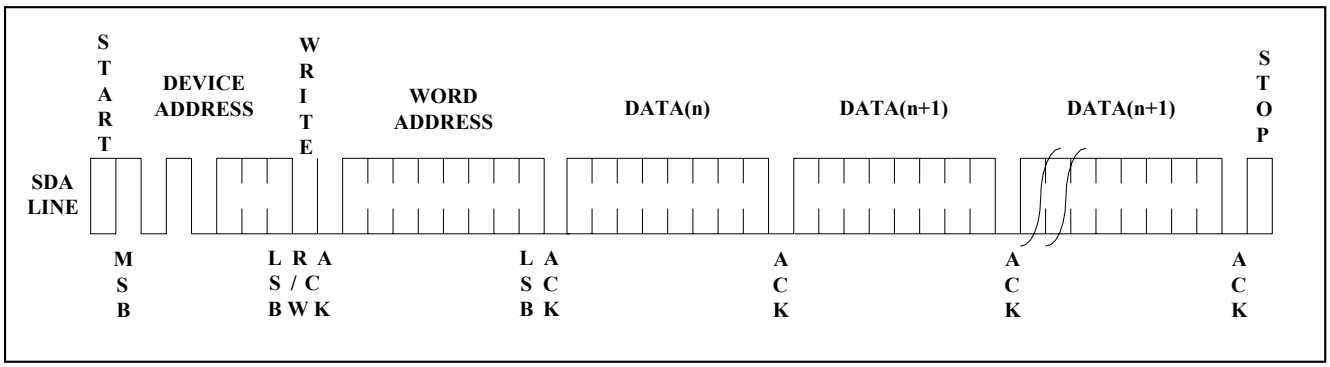


Figure 7. Page Write

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

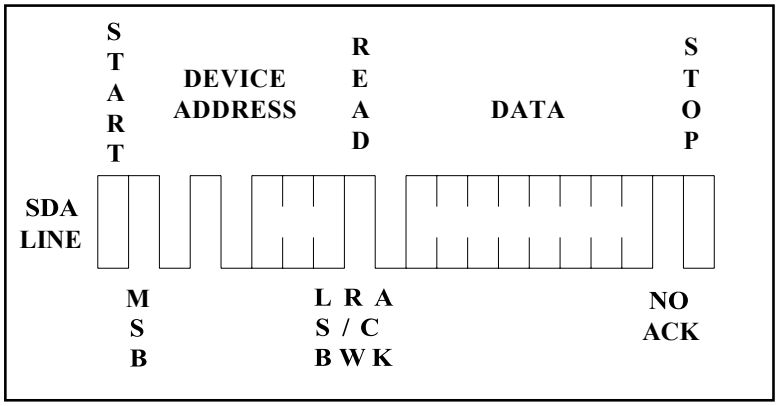


Figure 8. Current Address Read

RANDOM READ:A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**)

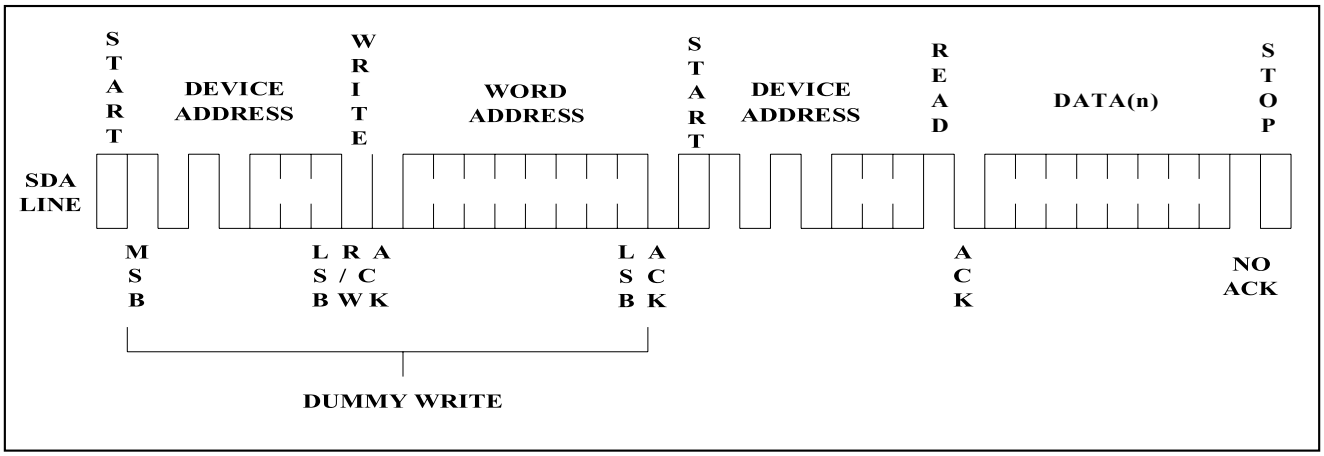


Figure 9. Random Read

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

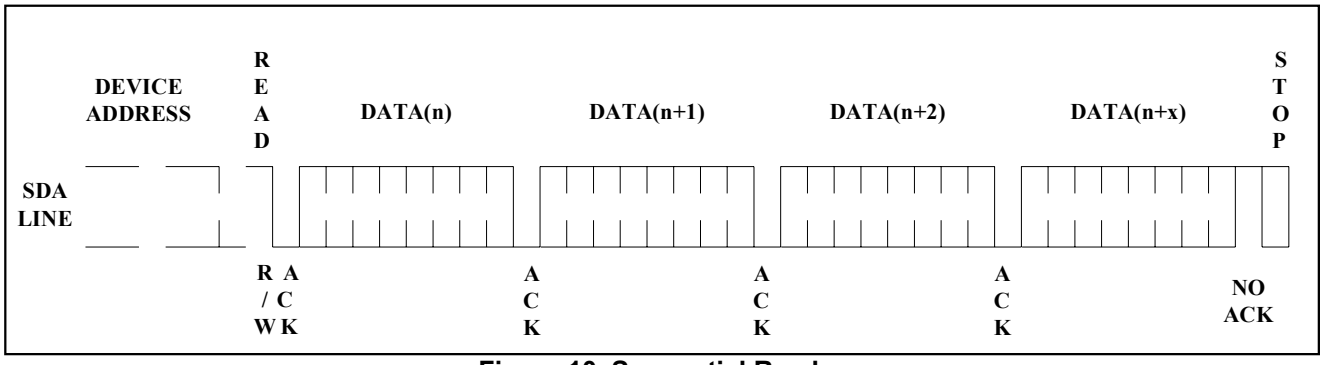


Figure 10. Sequential Read

Electrical Characteristics

Absolute Maximum Stress Ratings：

- DC Supply Voltage .....V to +6.5V
- Input / Output Voltage..... GND-0.3V to VCC+0.3V
- Storage Temperature..... . .-65℃ to +150℃
- Electrostatic pulse (Human Body model) 8000V

Comments：

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from (unless otherwise noted):

EV24C02A/EV24C04A/ EV24C08A/EV24C16A	T_A =-40℃ to +85℃	VCC = +1.7V to +5.5V@400kHz VCC = +2.5V to +5.5V@1MHz CL=100 pF
EV24C02AE1/EV24C04AE1/ EV24C08AE1/EV24C16AE1	T_A =-40℃ to +105℃	
EV24C02AE0/EV24C04AE0/ EV24C08AE0/EV24C16AE0	T_A =-40℃ to +125℃	

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Current VCC=5.0V	I_{CC1}	-	0.14	0.3	mA	READ at 400KHZ
Supply Current VCC=5.0V	I_{CC2}	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=5.0V	I_{SB1}	-	0.03	0.5	μA	V_{IN}=V_{CC} or V_{SS}
Input Leakage Current	I_{L1}	-	0.10	1.0	μA	V_{IN}=V_{CC} or V_{SS}
Output Leakage Current	I_{LO}	-	0.05	1.0	μA	V_{OUT}=V_{CC} or V_{SS}
Input Low Level	V_{IL1}	-0.3	-	V_{CC}×0.3	V	V_{CC}=1.7V to 5.5V
Input High Level	V_{IH1}	V_{CC}×0.7	-	V_{CC}+0.3	V	V_{CC}=1.7V to 5.5V
Output Low Level VCC=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}=0.15mA
Output Low Level VCC=5.0V	V_{OL2}	-	-	0.4	V	I_{OL}=3.0mA

Table 3

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +2.5V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(A0,A1,A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

Table 4

AC Electrical Characteristics

Applicable over recommended operating range from (unless otherwise noted):

EV24C02A/EV24C04A/ EV24C08A/EV24C16A	T_A =-40℃ to +85℃	VCC = +1.7V to +5.5V@400kHz VCC = +2.5V to +5.5V@1MHz CL=100 pF
EV24C02AE1/EV24C04AE1/ EV24C08AE1/EV24C16AE1	T_A =-40℃ to +105℃	
EV24C02AE0/EV24C04AE0/ EV24C08AE0/EV24C16AE0	T_A =-40℃ to +125℃	

Parameter	Symbol	1.7V≤V_{CC} < 2.5V			2.5V≤V_{CC} < 5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	f_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD:STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU:STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data in Setup Time	$t_{SU:DAT}$	100	-	-	100	-	-	ns
Input Rise Time(1)	t_R	-	-	0.3	-	-	0.12	μs
Input Fall Time(1)	t_F	-	-	0.3	-	-	0.12	μs
Stop Setup Time	$t_{Su:STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	-	1M	-	-	Write Cycle

Table 5

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

Bus Timing

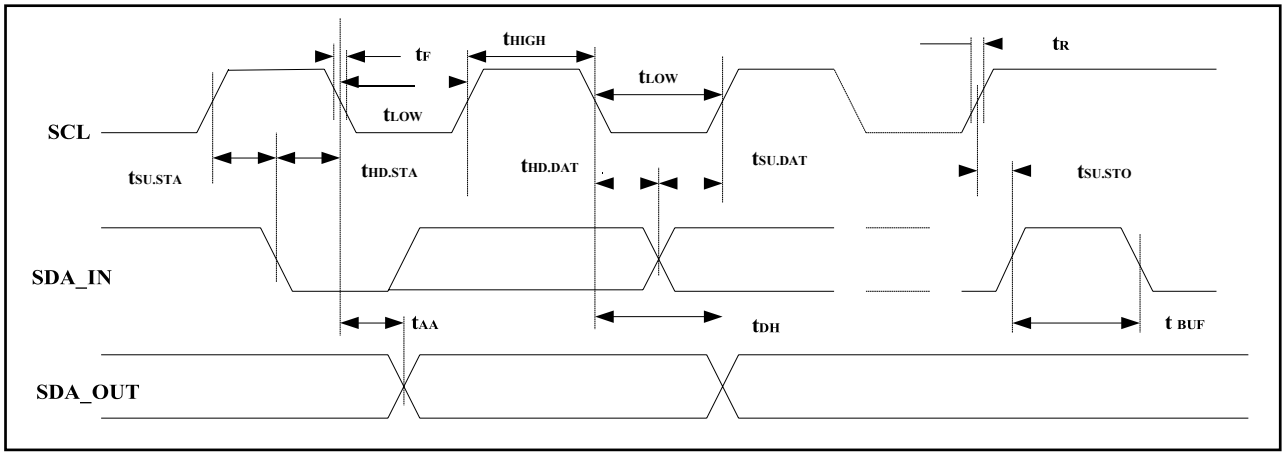


Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

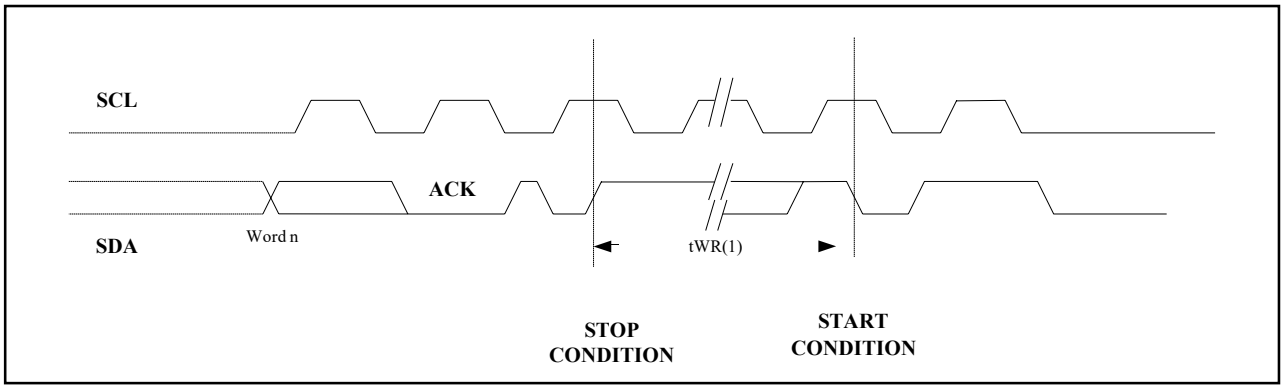


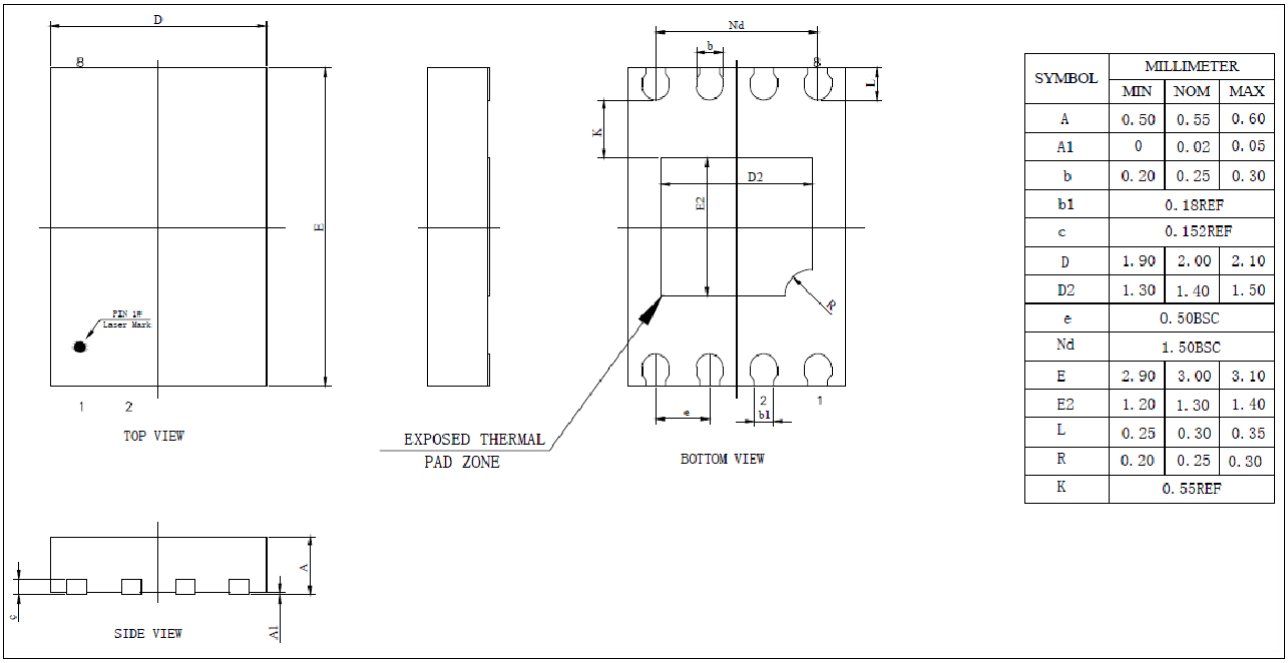
Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

Notes:

The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

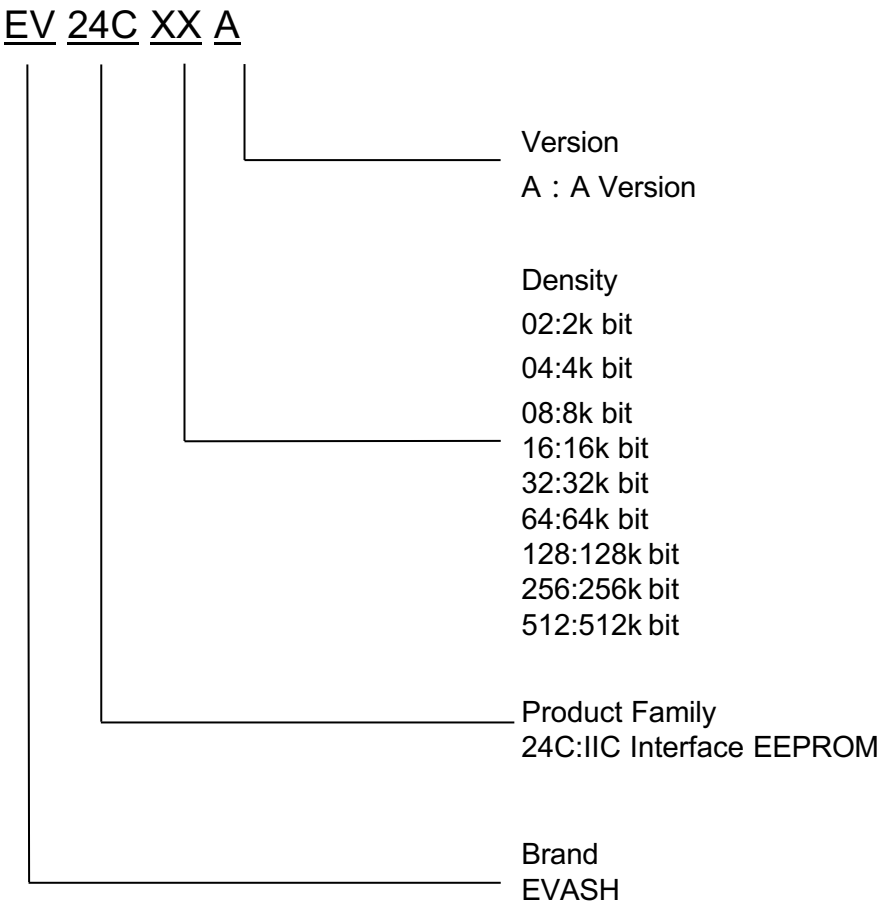
Package Information

UDFN



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.152REF		
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
L	0.25	0.30	0.35
R	0.20	0.25	0.30
K	0.55REF		

BL	Packaging House Identifier
XX	02:2K 2K bit EEPROM 08: 8K bit EEPROM 04:4K 4K bit EEPROM 16: 16K bit EEPROM
YY	Year
WW	Week



Ordering Information

Device	Package	Shipping (Qty/Packing)
EV24C02A	UDFN	3000/Tape &Reel
EV24C04A	UDFN	3000/Tape &Reel
EV24C08A	UDFN	3000/Tape &Reel
EV24C16A	UDFN	3000/Tape &Reel

单击下面可查看定价，库存，交付和生命周期等信息

>>EVASH