650V GaN FET

Datasheet
Preliminary

1. Description

The G1N65 series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

Features

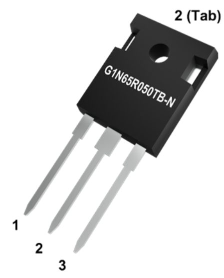
- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_G and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Low Q_{RR} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

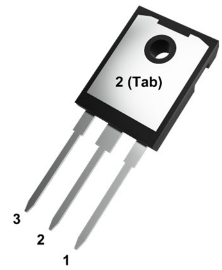
- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements.
- Improved safety & reliability due to cooler operation temperature.
- Higher output power due to the best efficiency and thermal capability.

Applications

- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits.
- High-efficiency/High-frequency phase-shift, LLC or other soft-switching topologies.

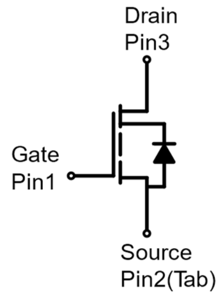


Top View



Bottom View

Gate	Pin1
Source	Pin2(Tab)
Drain	Pin3



Schematic Symbol

- **RoHS Compliant**
- **REACH Compliant**
- **Halogen-Free**

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DSS(PK)}$ (V) [a)]	800
$R_{DS(ON)}$ (mΩ) typical [b)]	50
Q_{OSS} (nC)	120
Q_G (nC)	16

[a)] Duty < 1%, spike duration < 30μs, nonrepetitive
[b)] Dynamic on-resistance

Part Number & Package Information

Part #	Package	Package Base
G1N65R050TB-N	TO-247	Source

2. Maximum Ratings

Name	Parameter	Value
V_{DSS} (V)	Maximum drain-to-source voltage (T_J = -55°C to 150°C)	650
$V_{DSS(PK)}$ (V)	Maximum drain-to-source peak voltage [a)]	800
V_{GSS} (V)	Maximum gate-to-source voltage	±20
P_D (W)	Maximum power dissipation (T_C = 25°C)	119
I_{DS} (A)	Maximum continuous drain current (T_C = 25°C)	34
	Maximum continuous drain current (T_C = 100°C)	22
$I_{DS\ (Pulse)}$ (A)	Maximum pulse drain current (T_C = 25°C) [b)]	150
T_J (°C)	Junction temperature	-55 to +150
T_S (°C)	Storage temperature	-55 to +150
T_{SOLD} (°C)	Soldering peak temperature [c)]	260
-	Mounting Torque (N·cm)	80

[a)] Duty cycle < 1%, spike duration < 30μs, nonrepetitive
[b)] Pulse width = 10μs
[c)] For 10 seconds, 1.6 mm from the case

3. Thermal Characteristics

Name	Parameter	Value
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	1.05
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance	40

4. Device Characteristics

T_J = 25°C unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DSS}	Maximum drain-to-source voltage	650	-	-	V	V_{GS} = 0V
$V_{GS(th)}$	Gate threshold voltage	3.3	4	4.8	V	V_{DS} = V_{GS}, I_D = 0.7mA
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-6.2	-	mV/°C	V_{DS} = V_{GS}, I_D = 0.7mA
$R_{DS(ON)}$	Drain-source on resistance [a)]	-	50	60	mΩ	V_{GS} = 10V, I_D = 22A
		-	105	-	mΩ	V_{GS} = 10V, I_D = 22A, T_J = 150°C
I_{DSS}	Off-state drain-to-source leakage current	-	4	40	μA	V_{DS} = 650V, V_{GS} = 0V
		-	15	-	μA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-source leakage current	-	-	100	nA	V_{GS} = 20V
		-	-	-100	nA	V_{GS} = -20V
C_{ISS}	Input capacitance	-	1000	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz
C_{OSS}	Output capacitance	-	110	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz
C_{RSS}	Reverse switching capacitance	-	6	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz
$C_{O(ER)}$	Equivalent output capacitance (energy related)	-	164	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
$C_{O(TR)}$	Equivalent output capacitance (time related)	-	280	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
Q_G	Total gate charge	-	16	24	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A
Q_{GS}	Gate-source charge	-	6	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A
Q_{GD}	Gate-drain charge	-	5	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A
Q_{OSS}	Output charge	-	120	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
$t_{D(ON)}$	Turn-on delay time	-	49.2	-	ns	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A, R_G = 45Ω, Z_{FB} = 240Ω at 100MHz
t_R	Rise time	-	11.3	-	ns	
$t_{D(OFF)}$	Turn-off delay time	-	88.3	-	ns	
t_F	Fall time	-	10.9	-	ns	

[a)] Dynamic ON-resistance

Reverse Device Characteristics, T_J = 25°C unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
I_S	Reverse current	–	–	22	A	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle
$I_{S\ (Pulse)}$	Reverse pulse current	–	–	77	A	V_{GS} = 0V, V_{SD} = 6V, pulse width ≤ 100µs, T_J = 150°C
V_{SD}	Reverse voltage [a]	–	2.2	2.6	V	V_{GS} = 0V, I_S = 22A
		-	1.6	1.9	V	V_{GS} = 0V, I_S = 11A
t_{RR}	Reverse recovery time	–	50	–	ns	I_S = 22A, V_{DD} = 400V
Q_{RR}	Reverse recovery charge [b]	–	120	–	nC	
$(di/dt)_{RM}$	Reverse diode di/dt [c]	-	-	2500	A/µs	Circuit implementation and parameters in Section 7

[a] Includes dynamic ON-resistance

[b] Including Q_{OSS}

[c] di/dt is automatically satisfied with the recommended circuit in Section 7

5. Typical Characteristics (T_C = 25°C unless specified)

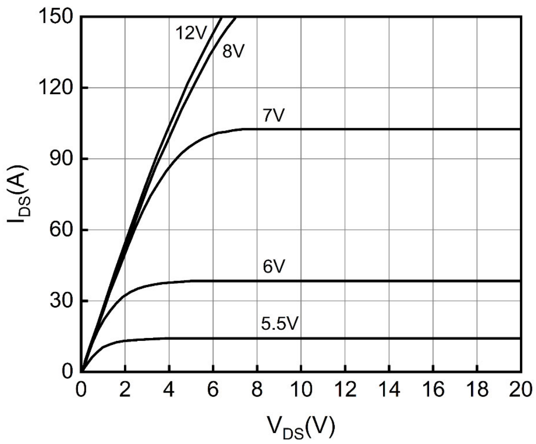


Figure 1. Typical Output Characteristics at T_J = 25°C (Parameter: V_{GS})

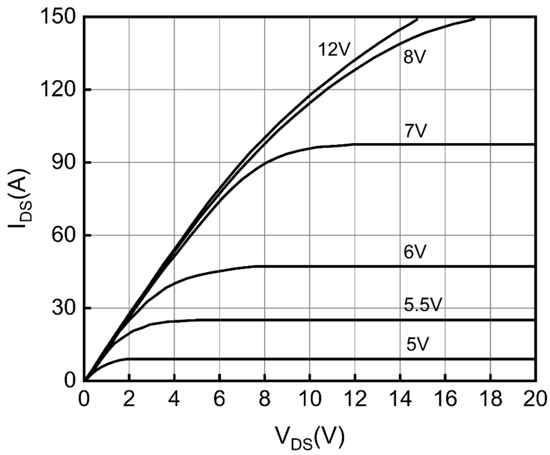


Figure 2. Typical Output Characteristics at T_J = 150°C (Parameter: V_{GS})

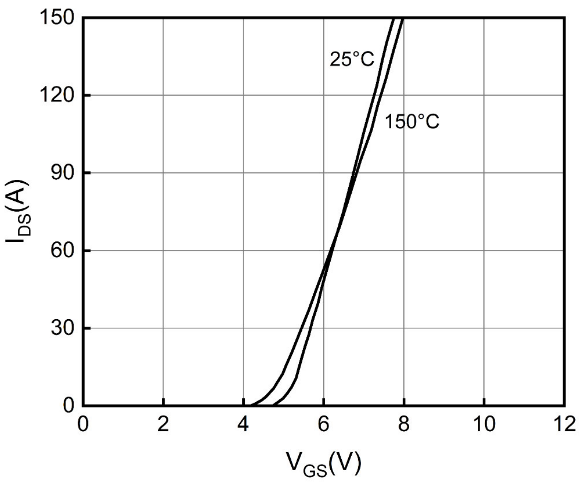


Figure 3. Typical Transfer Characteristics (V_{DS} = 20V, parameter: T_J)

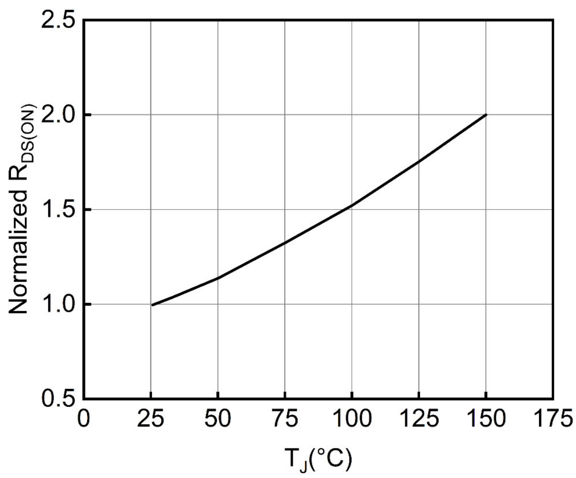


Figure 4. Normalized ON-resistance (I_D = 30A, V_{GS} = 10V)

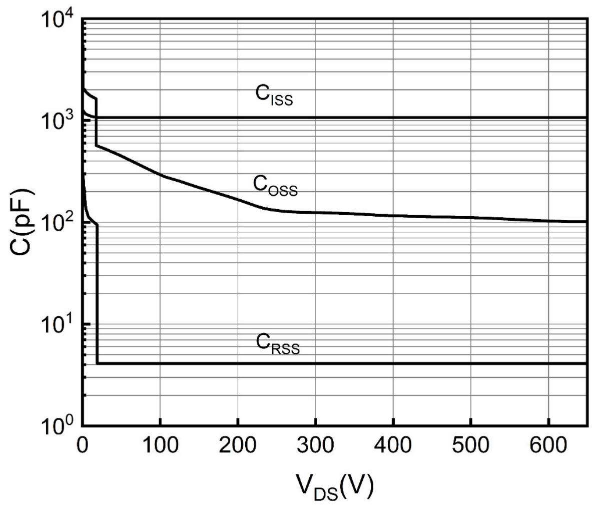


Figure 5. Typical Capacitance
(V_{GS} = 0V, *f* = 1MHz)

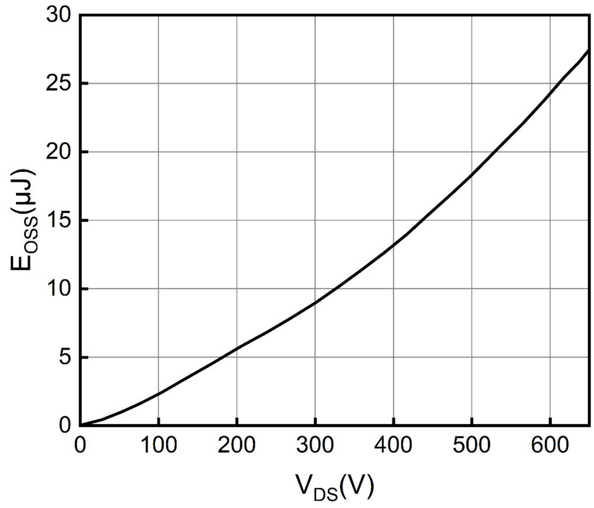


Figure 6. Typical C_{OSS} Stored Energy

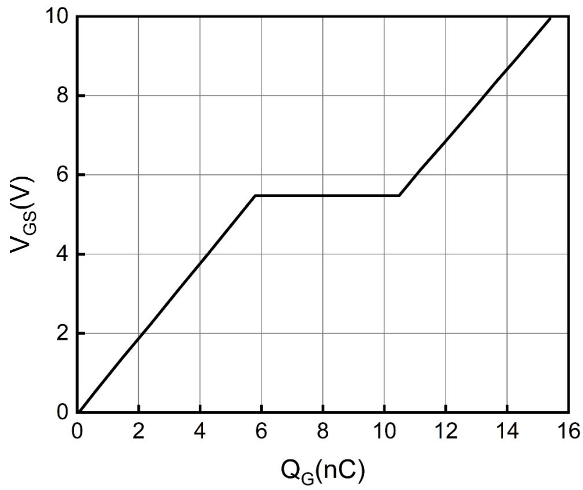


Figure 7. Typical Gate Charge
(I_{DS} = 32A, V_{DS} = 400V)

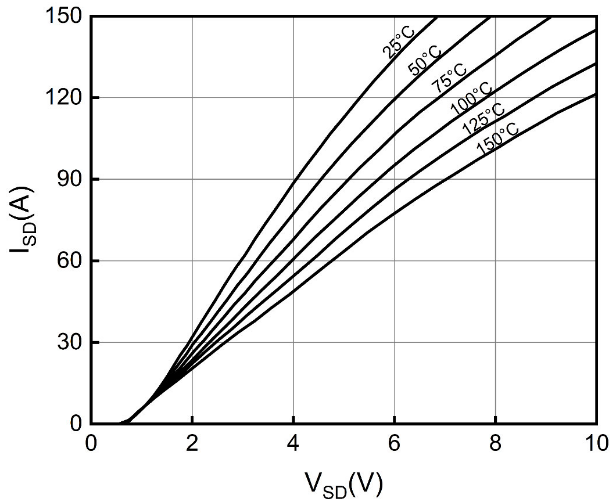


Figure 8. Reverse Conduction Characteristics
(Current pulse width ≤ 100μs, parameter: T_J)

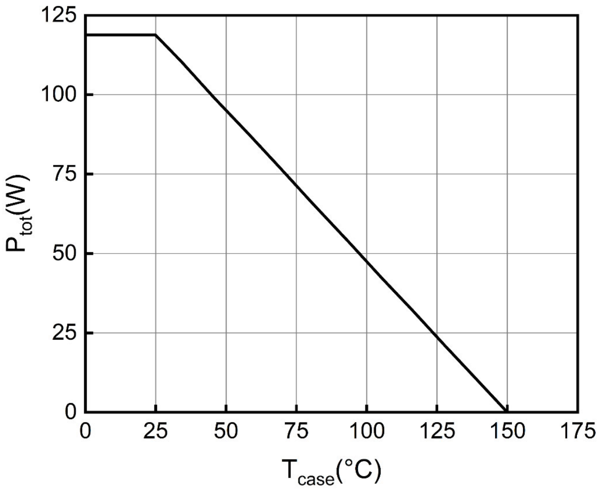


Figure 9. Power Dissipation

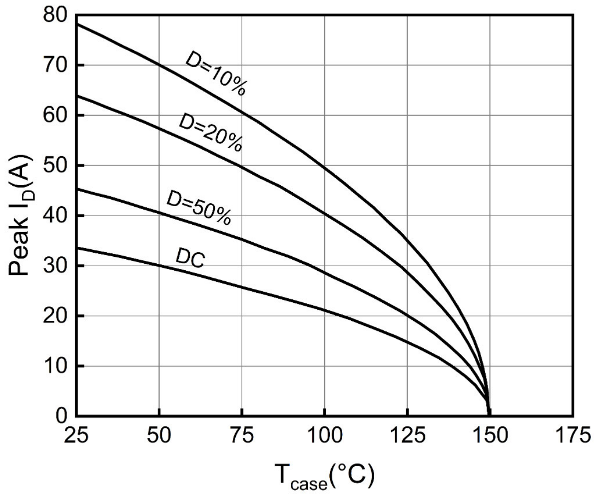


Figure 10. Current Derating
(Pulse width ≤ 10μs, V_{GS} ≥ 10V)

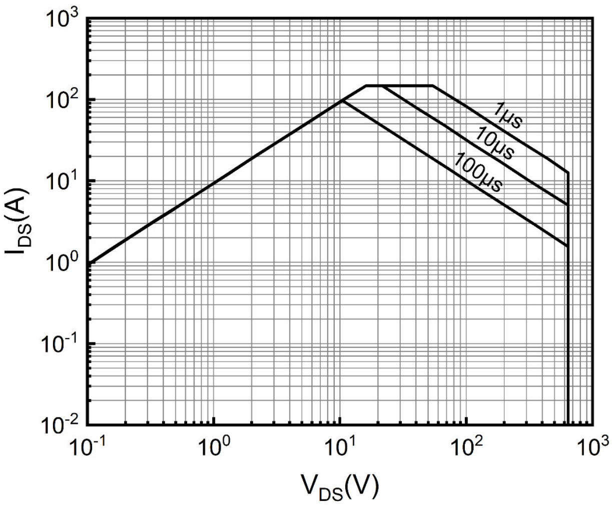


Figure 11. Safe Operating Area at T_C = 25°C

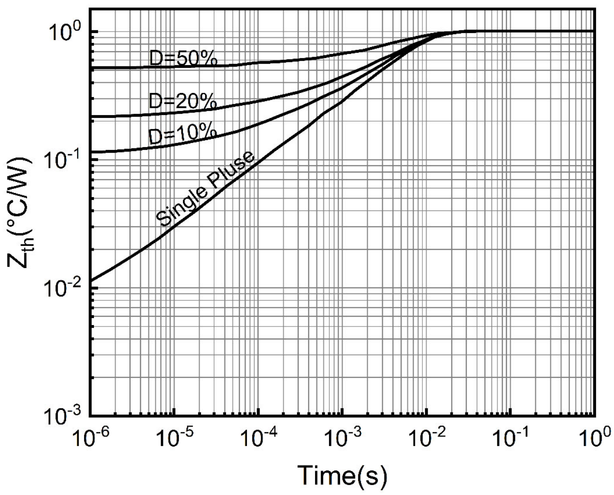


Figure 12. Transient Thermal Resistance

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate driver close to the GaN device and separate input traces from output traces	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor

7. Circuit Implementation

Half-bridge Schematic

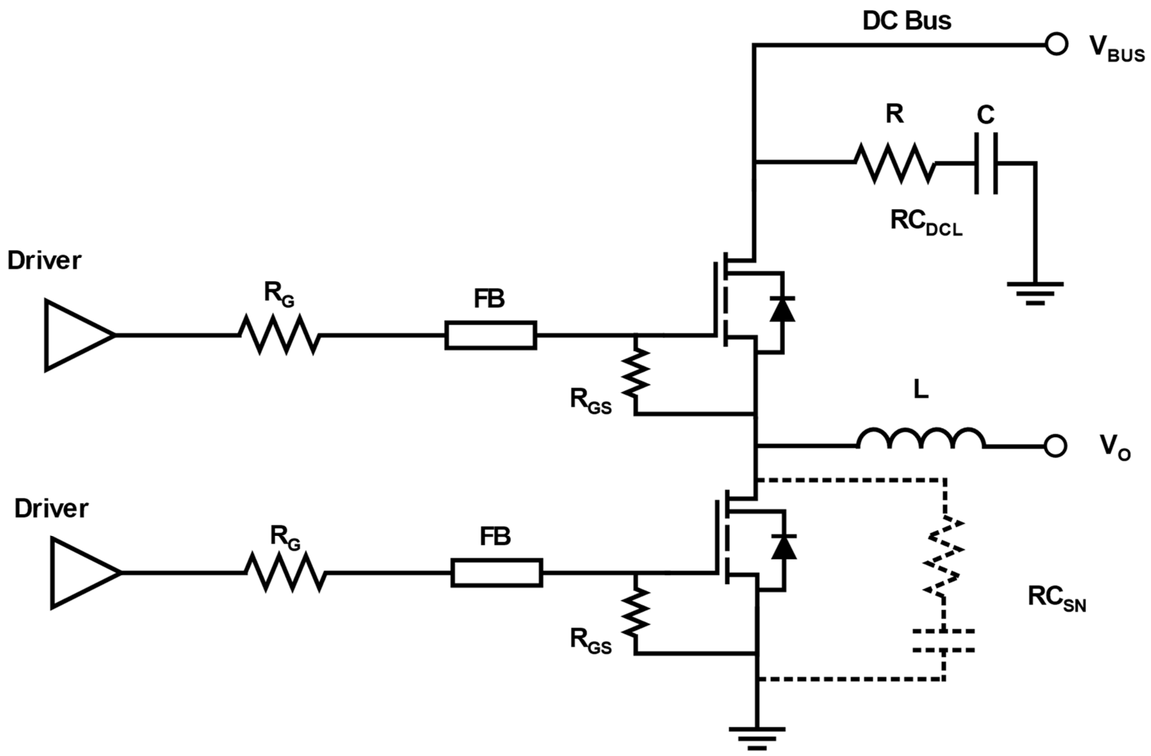


Figure 13. Simplified half-bridge schematic

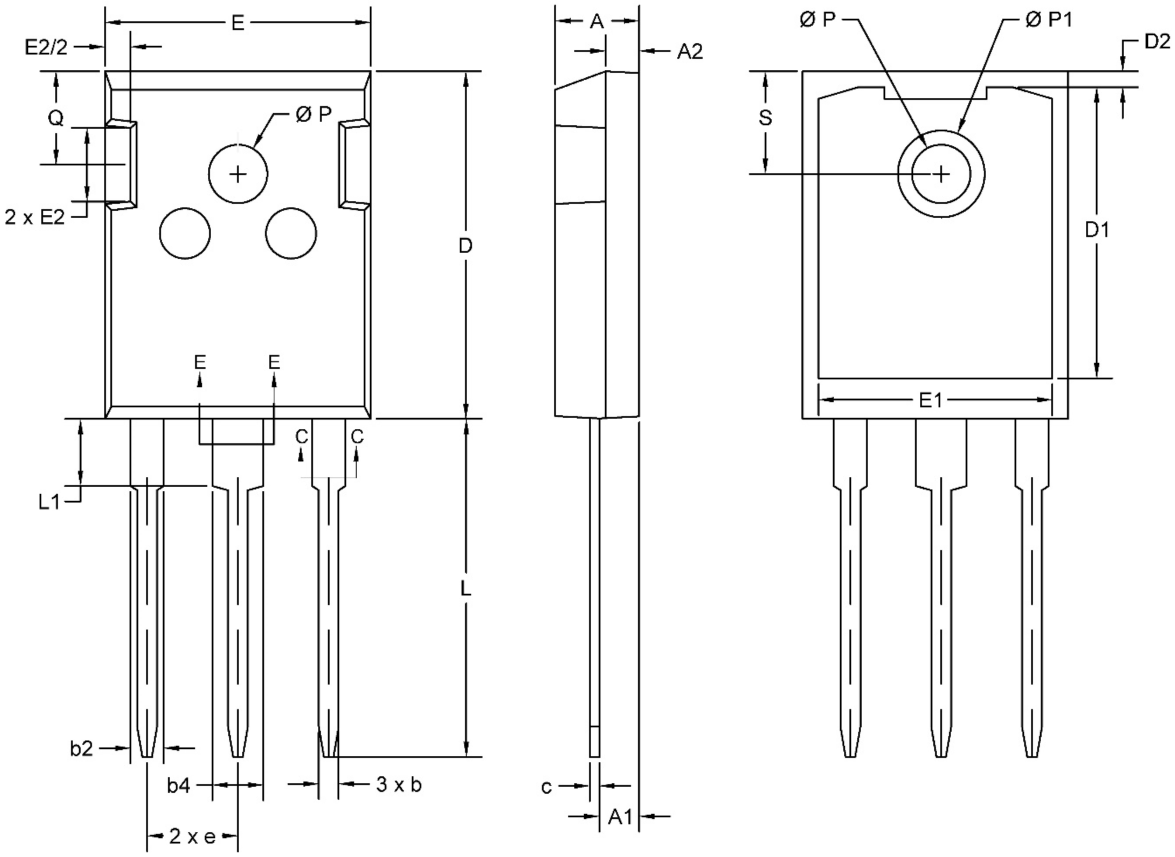
Recommended gate drive: (0V, 12V) with R_G = 45 Ω [a)]

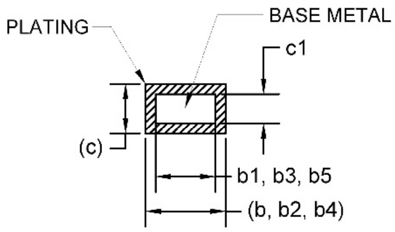
Gate Ferrite Bead (FB) [b)]	Required DC Link RC Snubber (RC_{DCL}) [c)]	Recommended Switching Node RC Snubber (RC_{SN})
180-240Ω @ 100MHz	(10nF + 3-5Ω) × 2	See note d and e below

Notes:

a) For bridge topologies only. R_G could be smaller in single ended topologies.
b) Examples of material selection: MPZ2012S221AT000(TDK), BLM21PG221SZ1D(Murata).
c) RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitor(s) should be located away from the RC_{DCL}.
d) RC_{SN} is needed only if R_G is smaller than recommendations.
e) If required, please use 15Ω+47pF.
f) The typical value of R_{GS} is 10kΩ.

8. Package Dimensions





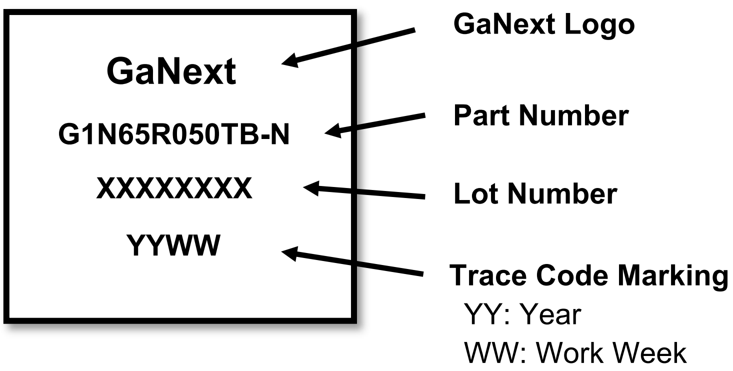
SECTION C-C, E-E

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. LEAD FINISH UNCONTROLLED IN L1.
3. OUTLINE CONFORMS TO JEDEC TO-247-AD.

DIM	mm		
	Min.	Typ.	Max.
A	4.82	5.00	5.19
A1	2.20	2.39	2.57
A2	1.82	2.01	2.18
b	1.09	1.19	1.35
b1	1.09	-	1.30
b2	1.87	2.03	2.31
b3	1.87	-	2.27
b4	2.94	3.05	3.22
b5	2.94	-	3.18
c	0.50	0.58	0.68
c1	0.50	-	0.64
D	20.67	20.85	21.11
D1	17.20	-	17.63
D2	0.81	-	1.20
E	15.72	15.90	16.15
E1	13.79	-	14.25
E2	4.30	-	4.86
e	5.46 BSC		
L	19.55	19.94	20.38
L1	3.93	4.11	4.48
ØP	3.50	3.61	3.69
ØP1	7.08	7.19	7.32
Q	5.41	-	5.85
S	6.15 BSC		
TO-247-3L			
GaNext			
DATE: 2021.11	Rev. 01		

9. Part Marking



10. Revision History

Revision No.	Date	Description of Change(s)
Rev01	2021-09-15	First Edition