GD25LX256E

DATASHEET

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1. FEATURES

- 256M-bit Serial Flash
  - 32M-byte
  - 256 bytes per programmable page

- Standard, Octal SPI, DTR Octal SPI
  - Standard SPI: SCLK, CS#, SI, SO, IO[7:2], WP#, RESET#
  - Octal SPI: SCLK, CS#, IO[7:0], WP#, RESET#
  - OPI DTR (Double Transfer Rate) Read
  - 3- or 4-Byte Address Mode

- High Speed Clock Frequency
  - 200MHz for fast read with 30PF load
  - OPI Mode Data transfer up to 166MBytes/s
  - Octal I/O Data transfer up to 166MBytes/s
  - DTR Octal I/O Data transfer up to 400MBytes/s with DQS

- Allows XIP(execute in place)operation
  - High speed Read reduce overall XiP instruction fetch time
  - Continuous Read with Wrap further reduce data latency to fill up SoC cache

- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Advanced Sector Protection
  - Top or Bottom selection

- Data Integrity Check
  - On-chip ECC (1-bit correction every 8-Byte) (1)
  - CRC detects accidental changes to raw data

- Fast Program/Erase Speed
  - Page Program time: 0.4ms typical
  - Sector Erase time: 30ms typical
  - Block Erase time: 0.1/0.2s typical
  - Chip Erase time: 50s typical

- Flexible Architecture
  - Sector of 4K-Byte
  - Block of 32/64K-Byte
  - Erase/Program Suspend/Resume

- Low Power Consumption
  - 25uA typical stand-by current
  - 5uA typical power-down current

- Advanced Security Features
  - 128-bit Unique ID
  - 4K-Byte Security Registers With OTP Lock

- Single Power Supply Voltage
  - Full voltage range: 1.65~2.0V

- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical

- Package Information
  - SOP16 300mil
  - TFBGA-24ball (5x5 Ball Array)
  - WLCSP

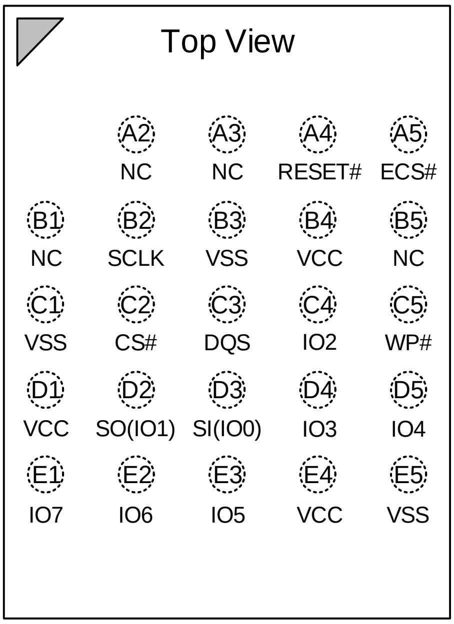
Note:

1. When ECC is enabled, it is required to program minimum one or multiple aligned 8-Byte granularities. Every aligned 8-Byte granularity should only be programmed once before Erase to ensure correct ECC operations.

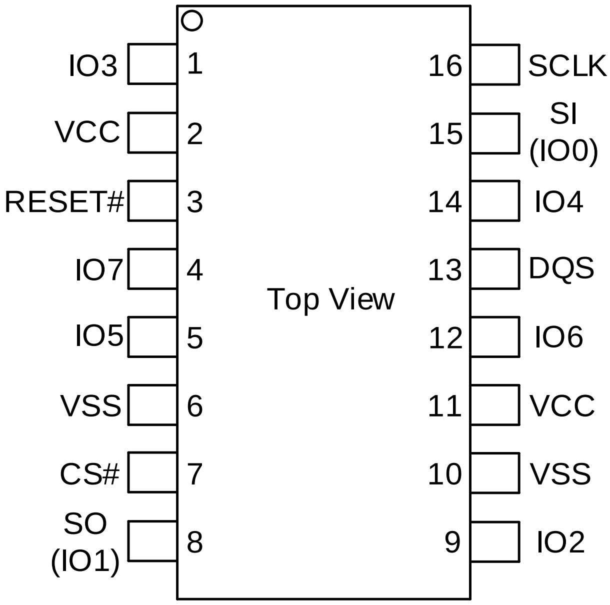
2. GENERAL DESCRIPTION

The GD25LX256E (256M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Octal SPI and DTR mode: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, I/O3 ,I/O4, I/O5, I/O6, I/O7, RESET#, WP# and DQS. The Octal I/O & Octal output data is transferred with speed of 166MBytes/s, and the DTR Octal I/O data is transferred with speed of 400MBytes/s.

CONNECTION DIAGRAM



24-BALL TFBGA (5x5 ball array)



16-LEAD SOP

Note: CS# must be driven high if chip is not selected. Please don’t leave CS# floating any time after power is on.

PIN DESCRIPTION

Table 1. Ball Description for TFBGA24 (5x5 ball array) package

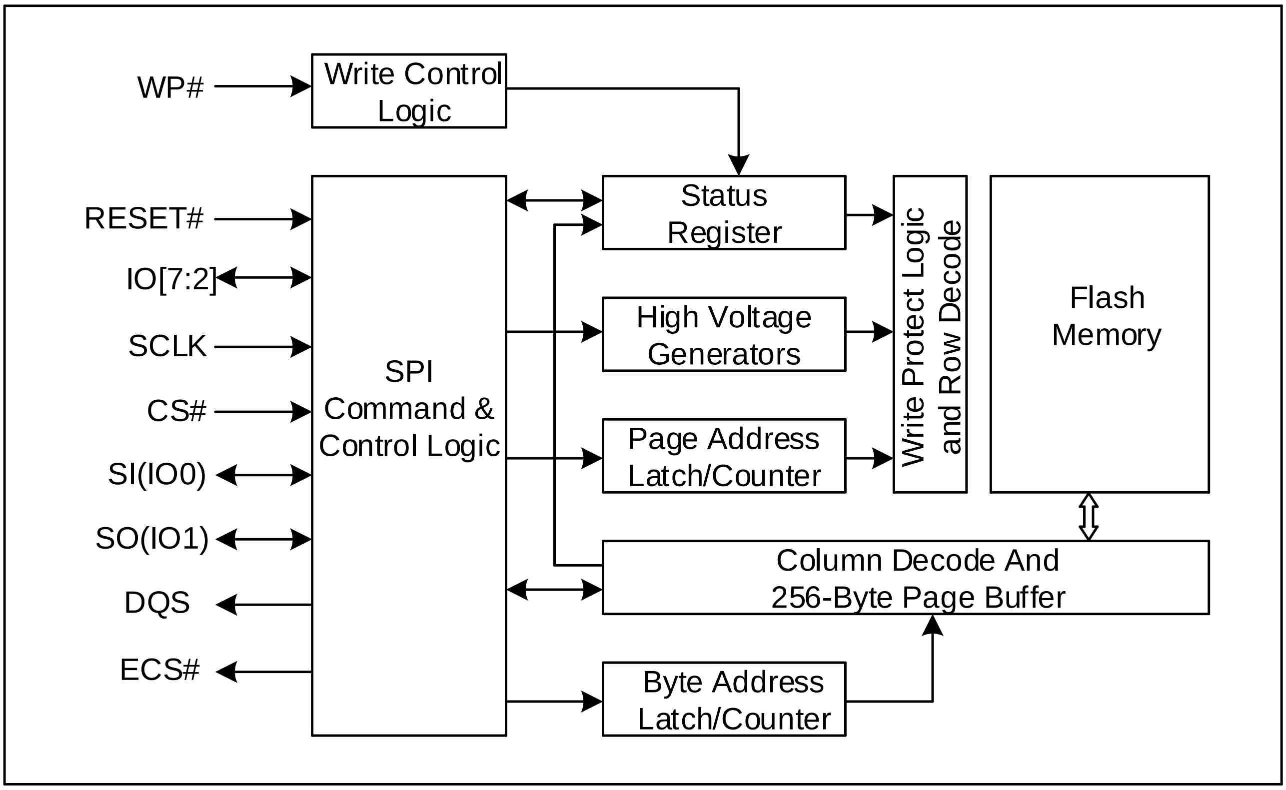
Pin No.	Pin Name	I/O	Description
A4	RESET#	I	Reset Input
A5	ECS#	O	ECC Correction Signal
B2	SCLK	I	Serial Clock Input
B3/C1/E5	VSS		Ground
B4/D1/E4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C3	DQS	O	Data Strobe Signal Output
C4	IO2	I/O	Data Input Output 2
C5	WP#	I	Write Protect Input

D2	SO (IO1)	I/O	Data Output (Data Input Output 1)
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)
D4	IO3	I/O	Data Input Output 3
D5	IO4	I/O	Data Input Output 4
E1	IO7	I/O	Data Input Output 7
E2	IO6	I/O	Data Input Output 6
E3	IO5	I/O	Data Input Output 5

Table 2. Pin Description for SOP16 300mil package

Pin No.	Pin Name	I/O	Description
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	RESET#	I	Reset Input
4	IO7	I/O	Data Input Output 7
5	IO5	I/O	Data Input Output 5
6	VSS		Ground
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	IO2	I/O	Data Input Output 2
10	VSS		Ground
11	VCC		Power Supply
12	IO6	I/O	Data Input Output 6
13	DQS	O	Data Strobe Signal Output
14	IO4	I/O	Data Input Output 4
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input

BLOCK DIAGRAM



3. MEMORY ORGANIZATION

GD25LX256E

Each device has	Each block has	Each sector has	Each page has	
32M	64/32K	4K	256	Bytes
128K	256/128	16	-	pages
8192	16/8	-	-	sectors
512/1024	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25LX256E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
511	8191	1FFF000h	1FFFFFFh
	……	……	……
	8176	1FF0000h	1FF0FFFh
510	8175	1FEF000h	1FEFFFFh
	……	……	……
	8160	1FE0000h	1FE0FFFh
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000h	02FFFFh
	……	……	……
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	……	……	……
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	……	……	……
	0	000000h	000FFFh

4. DEVICE OPERATION

4.1. SPI Mode

Standard SPI

The GD25LX256E features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Octal SPI

The GD25LX256E supports Octal SPI operation when using the “Octal Output Fast Read”, “Octal I/O Fast Read”, “Octal Input Page Program, Extended Octal Input Fast Program” (8BH/7CH, CBH/CCH, 82H/84H,C2H/8EH) commands. These commands allow data to be transferred to or from the device at eight times the rate of the standard SPI. When using the Octal SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Octal DTR SPI

The GD25LX256E supports Octal DTR SPI operation when using the “DTR Octal I/O Fast Read” (FDH) command. This command allows data to be transferred to or from the device at sixteen times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the Octal DTR SPI commands the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.2. OPI Mode

Standard OPI

The GD25LX256E supports Octal Peripheral Interface (OPI) operations only when the device is switched to OPI mode by setting byte<0> in Nonvolatile/Volatile Configuration Register. The OPI mode utilizes all 8 IO pins to input the command code. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK. Only one mode can be active at any given times. Upon power-up and after software reset using “Enable Reset (66H) and Reset (99H)” command, the state of the device is defined by the setting of byte<0> in Nonvolatile Configuration Register.

DTR OPI

The GD25LX256E supports DTR OPI operation when the device is switched to OPI mode by setting byte<0> in Nonvolatile/Volatile Configuration Register. The data input/output will be latched on both rising and falling edges of the serial clock. Only one mode can be active at any given times. Upon power-up and after software reset using “Enable Reset (66H) and Reset (99H)” command, the state of the device is defined by the setting of byte<0> in Nonvolatile Configuration Register.

4.3. RESET Function

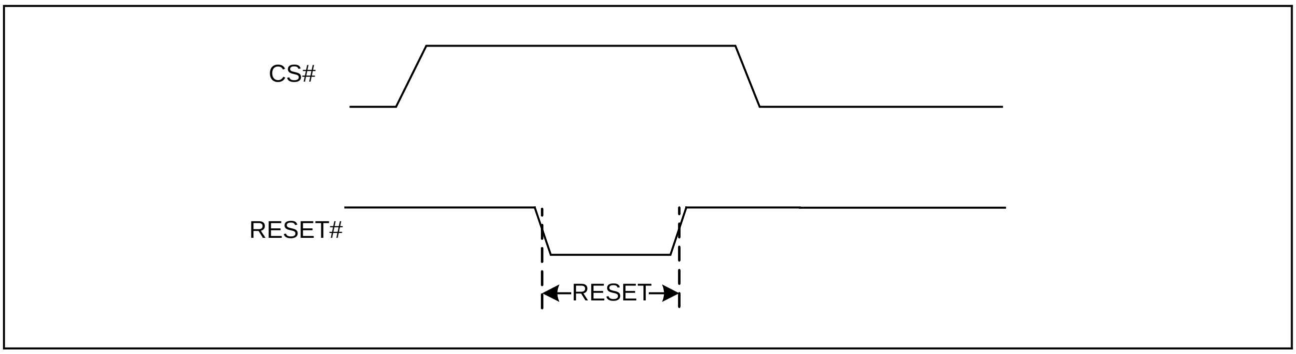
The RESET# pin allows the device to be reset by the control.

The RESET# pin goes low for a minimum period of tRLRH will reset the flash. After reset cycle, the flash is at the following states:

-Standby mode

-All the volatile bits will return to the default status as power on.

Figure 1 RESET Condition



4.4. ECC Function

The ECC Correction Signal (ECS#) pin is provided to the system hardware designers to determine the ECC status during any Read operation. The ECS# pin will be pulled low during any 8-Byte Read data output period in which an ECC event has occurred. ECS# pin can be used to represent SEC (Single Error Correction). ECC Correction Signal Output pin is an Open-Drain connection.

4.5. Data Strobe Function

DQS signal indicates output data valid for DTR modes and is required to support high speed data output. DQS pin is used for READ but not for WRITE operations, which is configured by nonvolatile and volatile configuration register byte <0>. DQS pin is not required in extended-SPI protocol except to achieve high frequency for specific DTR commands. When data strobe function is enabled, DQS signal is driven to ground once CS# goes LOW till the device is driving output data, in which case DQS toggles to synchronize data output. When data strobe function is not enabled, DQS signal is not driven.

5. DATA PROTECTION

The GD25LX256E provide the following data protection methods:

◆ Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:

-Power-Up/ Software reset (66H+99H)

-Write Disable (WRDI)

-Write Status Register (WRSR)

-Write Extended Address Register (WEAR)

-Write Nonvolatile Configuration Register (WNVCR)

-Write Volatile Configuration Register (WVCR)

-Page Program (PP)

-Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)

-Erase Security Registers / Program Security Registers

◆ Software Protection Mode:

-The Block Protect (BP3, BP2, BP1, and BP0) bits and Top Bottom (TB) bit define the section of the memory array that can be read but cannot be changed.

- Individual Block Protection bit provides the protection selection of each individual block and sectors in the top and bottom block.

◆ Hardware Protection Mode: WP# goes low to protect the BP0~BP3 bits, TB bit and SRP0 bit.

◆ Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and reset command (66H+99H).

Table 3. GD25LX256E Protected area size

Status Register Content					**Memory Content**			
TB	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h-01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h-01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h-01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h-01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 to 511	01F00000h-01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h-01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h-01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h-01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h-01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h-0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h-0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h-0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h-0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h-000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h-001FFFFFh	2MB	Lower 1/16

1	0	1	1	1	0 to 63	00000000h-003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h-007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h-00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	ALL	00000000h-01FFFFFFh	32MB	ALL
X	1	X	1	X	ALL	00000000h-01FFFFFFh	32MB	ALL

Table 4. GD25LX256E Individual Block Protection (WPS=0)

Block	Sector	Address range		Individual Block Lock Operation
511	8191	01FF F000h	01FF FFFFh	**512 Blocks** **Block Lock: 36H+Address** **Block Unlock: 39H+Address** **Read Block Lock: 3DH+Address** **Global Block Lock: 7EH** **Global Block Unlock: 98H**
	……	……	……	
	8176	01FF 0000h	01FF 0FFFh	
510	……	01FE 0000h	01FE FFFFh	
……	……	……	……	
……	……	……	……	
……	……	……	……	
1	……	0001 0000h	0001 FFFFh	
0	15	0000 F000h	0000 FFFFh	
	……	……	……	
	0	0000 0000h	0000 0FFFh	

Notes:

1. Protection configuration: This bit is used to select which Write Protect scheme should be used.
2. Volatile lock bits. Each volatile bit corresponds to and provides volatile protection for an individual memory sector, which is locked temporarily (protection is cleared when the device is reset or powered down).
3. The first and last sectors will have volatile protections at the 4KB sector level. Each 4KB sector in these sectors can be individually locked by volatile lock bits setting.

6. DATA INTEGRITY CHECK

The data storage and transmission errors will cause unexpected flash device variation that makes a harmful impact on overall system functions. To prevent these errors, GD25LX256E product provides advanced Data Integrity Check function. For the data storage and data transmission in the flash device, Data Integrity Check can check errors and correct them, allowing self-checking and preventing errors in advance.

The Data Integrity Check function includes two methods:

- **ECC (Error Checking and Correcting): to prevent the data storage errors**
- **Parity Check (Cyclic Redundancy Check): to prevent the data transmission errors**

The register data and software signals can also be used to associate the Data Integrity Check function to fully record the results of checking, and can also immediately feedback.

6.1. ECC (Error Checking and Correcting)

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device operation life and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In GD25LX256E, every aligned 8-Byte data (A[2:0] = 0, 0, 0) stored in the memory array will be checked by the internal ECC engine using SEC (Single Error Correction) Hsiao Codes algorithm. With 8-Byte ECC data granularity, ECC calculation latency time can be minimized and highest level of data integrity can be preserved.

The default value of all memory data is FFH (Erased) when the device is shipped from the factory. A “Page Program (02H/12H)” or an “Octal Page Program (82H/84H/8EH)” command can be used to program the user data into the memory array. When ECC is enabled (ECC=1 in Configuration Register), ECC calculation will be performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. It is necessary to program every page in aligned 8-Byte granularity so that ECC engine can store the correct ECC information. It is also required that every aligned 8-Byte data granularity can only be programmed once to avoid additional ECC calculation in the same granularity resulting incorrect ECC results. A technique previously known as “Incremental Byte/Bit Programming to the same Byte location” cannot be used for GD25LX256E when ECC is enabled.

During data read operations, the internal ECC engine will check the ECC results stored in the spare area and apply necessary error correction or error detection to the main array data being read out. It is necessary to check the ECC Status Bits (SEC) in the Status Register after every Read operation to see if the data read out contains one error or not. A Read operation can start from any Byte address and continue through the entire memory array, so it is not necessary to align the 8-Byte granularity boundary address to start a Read command.

Additional hardware monitoring of the ECC status can also be used to observe the ECC status in real time during any data output. When configured, the ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC event.

The ECC register bit can be reset through either of the following situations:

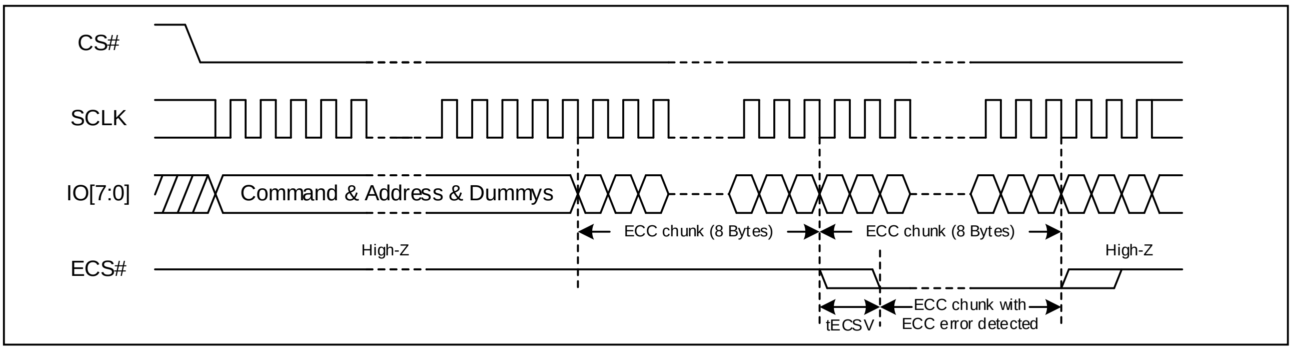
- Issuing Software Reset Command
- Hardware Reset
- Power-up cycle

6.2. ECS# (Error corrected Signal) Pin

The ECS# pin is a real time hardware signal to feedback the ECC correction status. The ECS# pin is designed as an open drain structure. In normal situation, the ECS# is kept on Hi-Z state. Once error correction begins, the ECS# pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing

The ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC (Single Error Correction) event.

Figure 2. ECS# Timing



6.3. Parity Check (CRC)

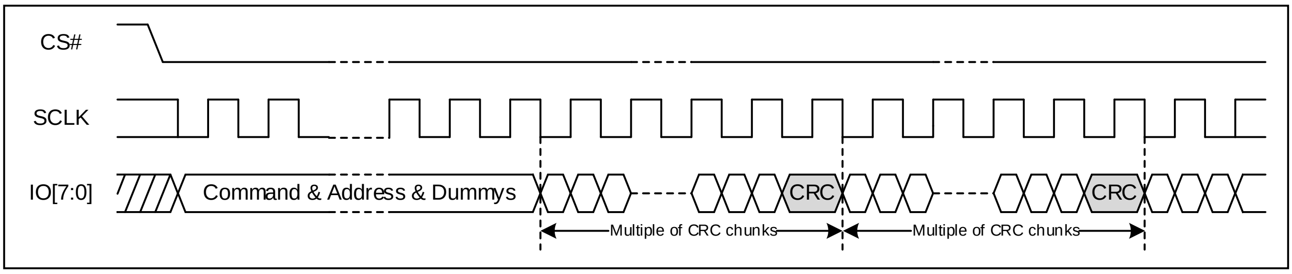
The parity check function can only be operated at DTR OPI read, it does not support STR read. The bit7~6 in Byte<4> of the Configuration Register can set the parity check function.

For read operation after the Parity check function is enabled, the data CRC bit should be output by each CRC chunk unit. Otherwise, read CRC code might be error.

The CRC Chunk size can be configured as 16-Byte, 32-Byte, or 64-Byte by the Configuration Register setting. However, when the device enters the "Read with Wrap" mode, while the CRC function is also enabled, the CRC Chunk size will be set to be identical with the Wrap Length (16, 32 or 64 Byte) by internal circuitry. Only when the device is not in the "Read with Wrap" mode, the original CRC Chunk size setting will be restored.

The data CRC bytes are calculated by bitwise exclusive-OR of all the data bytes in the CRC chunk.

Figure 3. CRC Timing



7. STATUS AND EXTENDED ADDRESS REGISTERS

7.1. Status Register

No.	Bit Name	Description	Note
S0	WIP	Erase/Write In Progress	Volatile, read only
S1	WEL	Write Enable Latch	Volatile, read only
S2	BP0	Block Protect Bits	Non-volatile writable
S3	BP1	Block Protect Bits	Non-volatile writable
S4	BP2	Block Protect Bits	Non-volatile writable
S5	BP3	Block Protect Bits	Non-volatile writable
S6	TB	Top/Bottom Protect Bit	Non-volatile writable
S7	SRP0	Status Register Protection	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register or configuration register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register or configuration register progress, when WIP bit sets 0, means the device is not in program/erase/write status register or configuration register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write, Program or Erase command is accepted.

TB bit

The Top Bottom (TB) bit is non-volatile. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bits (BP3, BP2, BP1, and BP0), starting from Top or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set to "1", the protect area will change to Bottom area of the memory device. This bit is written with the Write Status Register (WRSR) command.

BP3, BP2, BP1, BP0 bits

The Block Protect (BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, and BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed only if none sector or block is protected.

SRP0 bit

The Status Register Protect SRP0 bit are non-volatile Read/Write bits in the status register. The SRP0 bit in conjunction with SRP1 bit (Reference Configuration Register) control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	WP#	Status Register	Description
x	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	1	X	One Time Program(1)	Status Register is permanently protected and cannot be written to.

NOTE:

1. This feature is available on special order. Please contact GigaDevice for details.

7.2. Flag Status Register

No.	Bit Name	Description	Note
FS0	ADS	Current Address Mode	Volatile, read only
FS1	Protection	0:clear;1= failure or protection error	Volatile read only
FS2	SUS_P	Program Suspend	Volatile, read only
FS3	Reserved	Reserved	Reserved
FS4	PE	Program Error bit	Volatile, read only
FS5	EE	Erase Error bit	Volatile, read only
FS6	SUS_E	Erase Suspend	Volatile, read only
FS7	RY/BY#	Ready/Busy#	Volatile, read only

The status and control bits of the Flag Status Register are as follows:

ADS bit

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

Protection bit

The Protection bit is a read only bit that indicates a program or erase failure. Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

SUS_E, SUS_P bits

The SUS_E and SUS_P bits are read only bits in the Flag Status Register (FS6 and FS2) that are set to 1 after executing an Erase/Program Suspend (75H) command (The Erase Suspend will set the SUS_E to 1,and the Program Suspend will set the SUS_P to 1). The SUS_E and SUS_P bit are cleared to 0 by Erase/Program Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

PE bit

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space.
Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

EE bit

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space.
Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

RY/BY# bit

The RY/BY# bit is a read only bit that indicates Program or Erase Status bit. Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.

7.3. Extended Address Register

Table 5. Extended Address Register

No.	Name	Description	Note
EA0	A24	Address bit	Volatile writable
EA1	Reserved	Reserved	Reserved
EA2	Reserved	Reserved	Reserved
EA3	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA5	Reserved	Reserved	Reserved
EA6	Reserved	Reserved	Reserved
EA7	SEC	Error Correction bit	Volatile, read only

The extended address register is only used when the address mode is 3-Byte mode, as to set the higher address. A24=1 indicates the upper 128Mb memory address, A24=0 indicates the lower 128Mb. The default value of EA0 is “0”.
For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected top or bottom 128Mb, and it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.
The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase, block erase, program operation are limited in selected segment and will not cross the boundary.

A24 bit

The Extended Address Bit A24 is used only when the device is operating in the 3-Byte Address Mode (ADS=0), which is volatile writable by C5H command. The lower 128Mb memory array (00000000h – 00FFFFFFh) is selected when A24=0, and all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (01000000h – 01FFFFFFh) will be selected.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit A24 setting will be ignored.

SEC bits

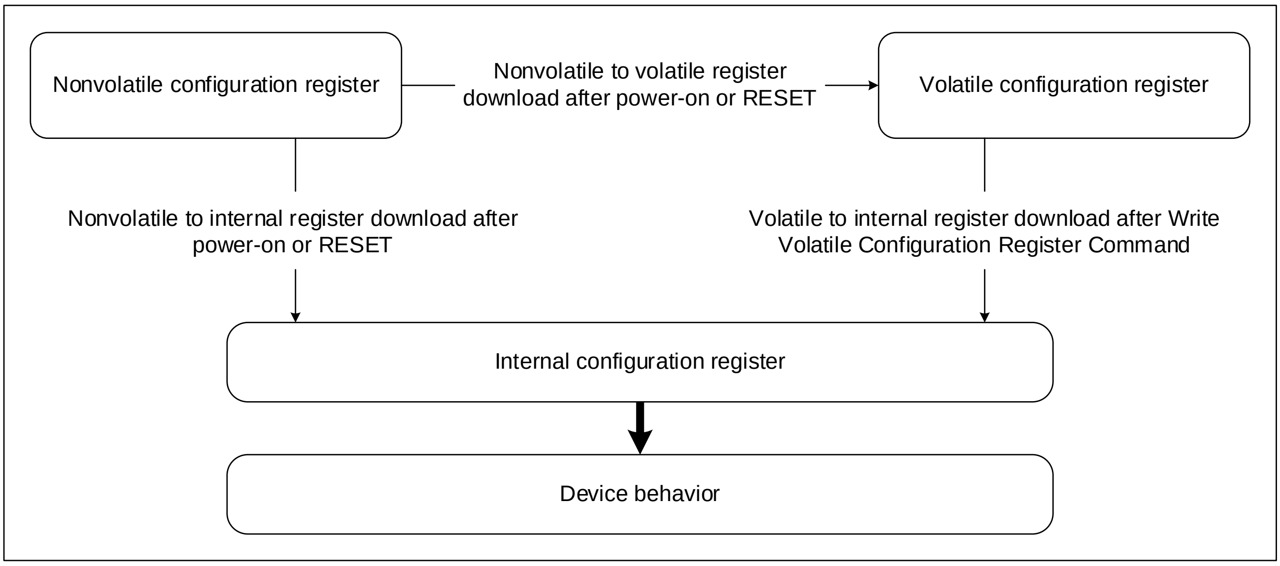
SEC (Single Error Correction) Status Bit are used to show the ECC results for the last Read operation. SEC bit will be cleared to 0 once the device accepts a new Read command.

SEC	Definitions
0	No ECC events in all aligned 8-Byte granularities
1	SEC events in single or multiple 8-Byte granularities, and the data is OK to use. (Unless it contains more than one odd bit errors in 8-Byte granularity)

8. Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users. The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.



8.1. Nonvolatile Configuration Register

Nonvolatile Configuration Register bits set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme, but only the LSB is used to access different register settings, thereby providing up to 256 bytes of registers (See the table below for the details). A READ command from a reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit isn't cleared.

Table 6. Nonvolatile Configuration Register

Addr	Settings	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
<0>	I/O mode	1	1	1	1	1	1	1	1	SPI with DQS (Default)
		1	1	0	1	1	1	1	1	SPI W/O DQS
		1	1	1	0	0	1	1	1	Octal DTR with DQS
		1	1	0	0	0	1	1	1	Octal DTR W/O DQS
		1	0	1	1	0	1	1	1	Octal with DQS
		1	0	0	1	0	1	1	1	Octal W/O DQS
		Others								The Same as Default Value (SPI with DQS)

<1>	Dummy cycle configuration[1-7]	0	0	0	0	0	0	0	0	default
		0	0	0	0	0	0	1	1	3 Dummy
		0	0	0	0	0	1	0	0	4 Dummy
		…								05~1D: 5~29 Dummy
		0	0	0	1	1	1	1	0	30 Dummy
		Others								Initiation Dummy According to Specific Command
<2>	OTP configuration	x	x	x	x	x	x	x	0	Security Registers Unlocked (Default)
		x	x	x	x	x	x	x	1	Security Registers Locked
		x	x	x	0	x	x	x	x	SRP1 Unlocked (Default)
		x	x	x	1	x	x	x	x	SRP1 Locked
<3>	Driver Strength configuration	1	1	1	1	1	1	1	1	50 Ohm (Default)
		1	1	1	1	1	1	1	0	35 Ohm
		1	1	1	1	1	1	0	1	25 Ohm
		1	1	1	1	1	1	0	0	18 Ohm
		Others								The Same as Default Value (50 Ohm)
<4>	CRC configuration	1	1	x	x	x	x	x	x	CRC Disabled (Default)
		1	0	x	x	x	x	x	x	16-Byte CRC
		0	1	x	x	x	x	x	x	32-Byte CRC
		0	0	x	x	x	x	x	x	64-Byte CRC
	On die termination	x	x	1	1	x	x	x	x	ODT Disabled (Default)
		x	x	1	0	x	x	x	x	150-Ohm ODT
		x	x	0	1	x	x	x	x	100-Ohm ODT
		x	x	0	1	x	x	x	x	50-Ohm ODT
	DLP configuration	x	x	x	x	1	x	x	x	DLP Disabled (Default)
		x	x	x	x	0	x	x	x	DLP Enabled
	Protection configuration	x	x	x	x	x	1	x	x	BP Protection (Default)
		x	x	x	x	x	0	x	x	WPS Protection[8]
	ECC configuration	x	x	x	x	x	x	x	1	ECC Enabled
		x	x	x	x	x	x	x	0	ECC Disabled (Default)
<5>	Beyond 128Mb addr configuration	1	1	1	1	1	1	1	1	3-Byte Address (Default)
		1	1	1	1	1	1	1	0	4-Byte Address
		Others								The Same as Default Value (3-Byte Address)
<6>	Continuous Read configuration[9]	1	1	1	1	1	1	1	1	XIP Disabled (Default)
		1	1	1	1	1	1	1	0	XIP Enabled
		Others								The Same as Default Value (XIP Disabled)
<7>	Wrap configuration[10]	1	1	1	1	1	1	1	1	Wrap Disabled (Default)
		1	1	1	1	1	1	1	0	64-Byte Wrap

		1	1	1	1	1	1	0	1	32-Byte Wrap
		1	1	1	1	1	1	0	0	16-Byte Wrap
		Others								The Same as Default Value (Wrap Disabled)

Notes:

1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
2. 03H/13H: SPI 0 dummy; OPI&DTR N/A
3. 05H/70H/9EH/9FH: SPI 0dummy; OPI&DTR 8 dummy.
4. 3DH: SPI 0dummy; OPI&DTR 8 dummy.
5. 4BH/5AH/B5H/85H: SPI&OPI&DTR 8 dummy.
6. 0BH/0CH/6BH/6CH/48H: SPI 8 dummy; OPI&DTR dummy follow CONFIGURATION REGISTER<2> (initiation = 16 dummy)
7. CBH/CCH/FDH: SPI&OPI&DTR dummy follow CONFIGURATION REGISTER<2> (initiation = 16 dummy)
8. When WPS protection is enabled, the entire memory array is being protected after Power-up or Reset.
9. Only Octal I/O Fast Read (CBH/CCH) and DTR Octal I/O Fast Read (FDH) support Continuous Read.
10. Only Octal I/O Fast Read (CBH/CCH) and DTR Octal I/O Fast Read (FDH) support Wrap read.

8.2. Volatile Configuration Register

Volatile Configuration Register bits temporarily set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme; however, only the LSB is used to access different register settings to provide up to 256 bytes of registers (See the table below for the details). A READ command from a reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit isn't cleared.

Table 7. Volatile Configuration Register

Addr	Settings	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
<0>	I/O mode	1	1	1	1	1	1	1	1	SPI with DQS (Default)
		1	1	0	1	1	1	1	1	SPI W/O DQS
		1	1	1	0	0	1	1	1	Octal DTR with DQS
		1	1	0	0	0	1	1	1	Octal DTR W/O DQS
		1	0	1	1	0	1	1	1	Octal with DQS
		1	0	0	1	0	1	1	1	Octal W/O DQS
		Others								The Same as Default Value (SPI with DQS)
<1>	Dummy cycle configuration(1-7)	0	0	0	0	0	0	0	0	default
		0	0	0	0	0	0	1	1	3 Dummy
		0	0	0	0	0	1	0	0	4 Dummy
		…								05~1D: 5~29 Dummy
		0	0	0	1	1	1	1	0	30 Dummy

		Others								Initiation Dummy According to Specific Command
<2>	Reserved	x	x	x	x	x	x	x	0	Reserved
<3>	Driver Strength configuration	1	1	1	1	1	1	1	1	50 Ohm (Default)
		1	1	1	1	1	1	1	0	35 Ohm
		1	1	1	1	1	1	0	1	25 Ohm
		1	1	1	1	1	1	0	0	18 Ohm
		Others								The Same as Default Value (50 Ohm)
<4>	CRC configuration	1	1	x	x	x	x	x	x	CRC Disabled (Default)
		1	0	x	x	x	x	x	x	16-Byte CRC
		0	1	x	x	x	x	x	x	32-Byte CRC
		0	0	x	x	x	x	x	x	64-Byte CRC
	On die termination	x	x	1	1	x	x	x	x	ODT Disabled (Default)
		x	x	1	0	x	x	x	x	150-Ohm ODT
		x	x	0	1	x	x	x	x	100-Ohm ODT
		x	x	0	1	x	x	x	x	50-Ohm ODT
	DLP configuration	x	x	x	x	1	x	x	x	DLP Disabled (Default)
		x	x	x	x	0	x	x	x	DLP Enabled
	Protection configuration	x	x	x	x	x	1	x	x	BP Protection (Default)
		x	x	x	x	x	0	x	x	WPS Protection(8)
	ECC configuration	x	x	x	x	x	x	x	1	ECC Enabled
		x	x	x	x	x	x	x	0	ECC Disabled (Default)
<5>	Beyond 128Mb addr configuration	1	1	1	1	1	1	1	1	3-Byte Address (Default)
		1	1	1	1	1	1	1	0	4-Byte Address
		Others								The Same as Default Value (3-Byte Address)
<6>	Continuous Read configuration(9)	1	1	1	1	1	1	1	1	XIP Disabled (Default)
		1	1	1	1	1	1	1	0	XIP Enabled
		Others								The Same as Default Value (XIP Disabled)
<7>	Wrap configuration(10)	1	1	1	1	1	1	1	1	Wrap Disabled (Default)
		1	1	1	1	1	1	1	0	64-Byte Wrap
		1	1	1	1	1	1	0	1	32-Byte Wrap
		1	1	1	1	1	1	0	0	16-Byte Wrap
		Others								The Same as Default Value (Wrap Disabled)

Notes:

1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
2. 03H/13H: SPI 0 dummy; OPI&DTR N/A
3. 05H/70H/9EH/9FH: SPI 0dummy; OPI&DTR 8 dummy.

4. 3DH: SPI 0dummy; OPI&DTR 8 dummy.

5. 4BH/5AH/B5H/85H: SPI&OPI&DTR 8 dummy.

6. 0BH/0CH/6BH/6CH/48H: SPI 8 dummy; OPI&DTR dummy follow CONFIGURATION REGISTER<2> (initiation = 16 dummy)

7. CBH/CCH/FDH: SPI&OPI&DTR dummy follow CONFIGURATION REGISTER<2> (initiation = 16 dummy)

8. When WPS protection is enabled, the entire memory array is being protected after Power-up or Reset.

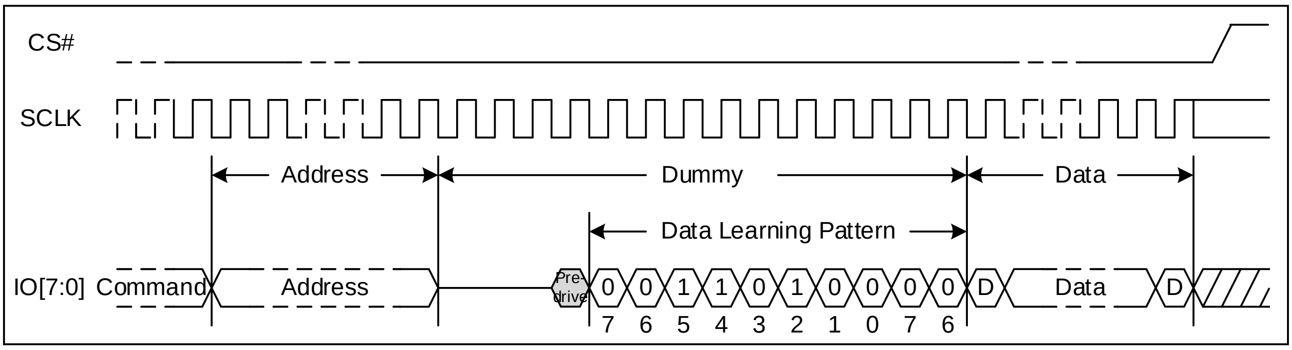
9. Only Octal I/O Fast Read (CBH/CCH) and DTR Octal I/O Fast Read (FDH) support Continuous Read.

10. Only Octal I/O Fast Read (CBH/CCH) and DTR Octal I/O Fast Read (FDH) support Wrap read.

DLP bit

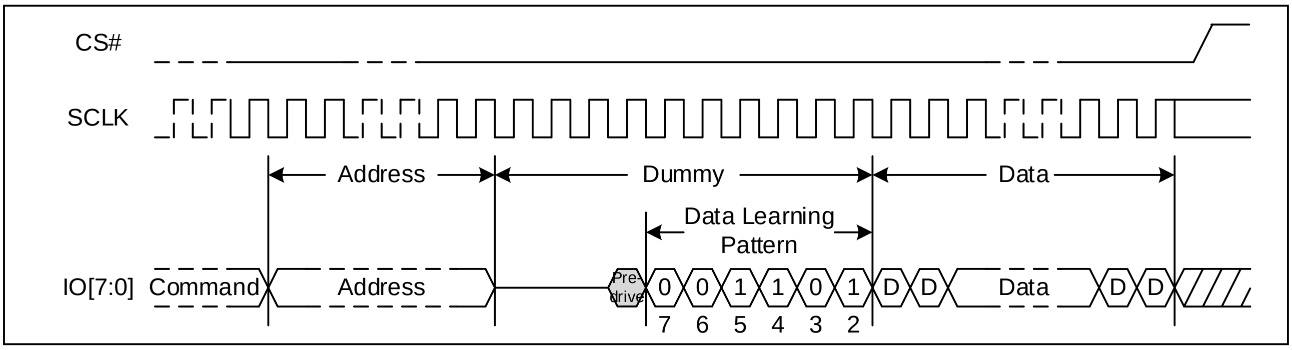
The DLP bit is Data Learning Pattern Enable bit, which is writable by B1/81H command. For Octal output, Octal I/O and Octal I/O DTR Fast Read commands, a pre-defined "Data Learning Pattern" can be used by the flash memory controller to determine the flash data output timing on 8 I/O pins. When DLP=1, from the failing edge of the fourth dummy clock, the flash will output "00110100" Data Learning Pattern sequence on each of the I/O or 8 I/O pins until data output. If the dummy clock is not enough for the output of the whole Data Learning Pattern, the last several bit of the Data Learning Pattern would be cut-off. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

Figure 4. Data Learning Pattern Sequence Diagram (STR, Dummy Clock ≥ 12)



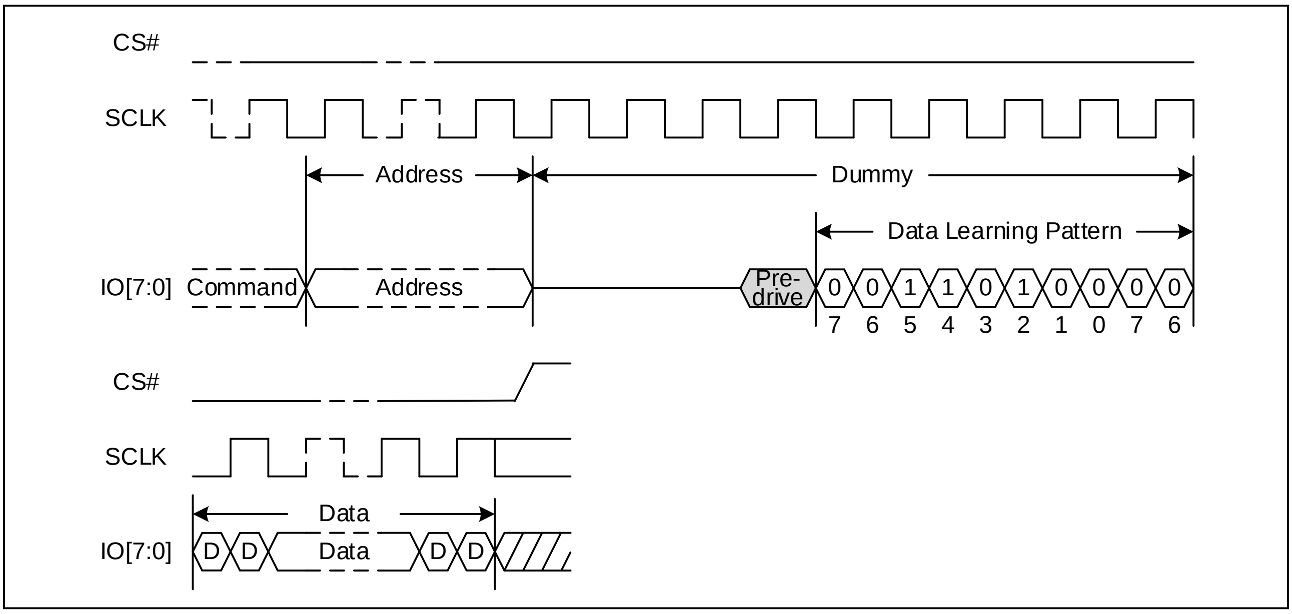
Note: 14 dummy cycle example

Figure 5. Data Learning Pattern Sequence Diagram (STR, Dummy Clock < 12)



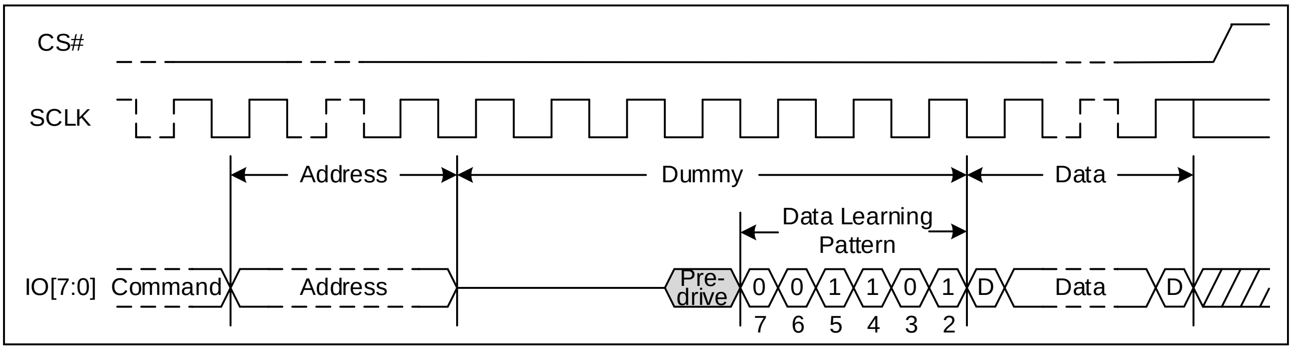
Note: 10 dummy cycle example

Figure 6. Data Learning Pattern Sequence Diagram (DTR, Dummy Clock ≥ 8)



Note: 9 dummy cycle example

Figure 7. Data Learning Pattern Sequence Diagram (DTR, Dummy Clock < 8)



Note: 7 dummy cycle example

8.3. Supported Clock Frequencies

Table 2. Clock Frequencies of TFBGA-24 (5x5 Ball Array)

Number of Dummy Clock Cycle	Octal I/O FAST READ		OPI DTR
	SDR	DTR	
3	20	20	20
4	40	40	40
5	60	60	60
6	84	84	84
7	84	84	84
8	104	104	104
9	104	104	104
10	133	133	133
11	133	133	133
12	152	152	152
13	152	152	152
14	166	166	166
15	166	166	166
16 and above	166	200	200

Note:

1. Values are guaranteed by characterization and not 100% tested in production

Table 3. Clock Frequencies of SOP16 (300mil)

Number of Dummy Clock Cycle	Octal I/O FAST READ		OPI DTR
	SDR	DTR	
3	20	20	20
4	40	40	40
5	60	60	60
6	84	84	84
7	84	84	84
8	104	104	104
9	104	104	104
10	133	133	133
11	133	133	133
12	152	152	152
13	152	152	152
14 and above	166	166	166

Note:

1. Values are guaranteed by characterization and not 100% tested in production

8.4. Data Sequence Wraps by Density

Table 4 Sequence of Bytes during Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- . . . -15-0-1- . .	0-1-2- . . . -31-0-1- . .	0-1-2- . . . -63-0-1- . .
1	1-2- . . . -15-0-1-2- . .	1-2- . . . -31-0-1-2- . .	1-2- . . . -63-0-1-2- . .
….	….	….	….
15	15-0-1-2-3- . . . -15-0-1- . .	15-16-17- . . . -31-0-1- . .	15-16-17- . . . -63-0-1- . .
….	….	….	
31	-	31-0-1-2-3- . . . -31-0-1- . .	31-32-33- . . . -63-0-1- . .
…	….	….	….
63	-	-	63-0-1- . . . -63-0-1- . .

9. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 10 Commands (Extended/Octal SPI)

Command name	Code	Extended SPI		Octal SPI			Addr. Bytes	Data Bytes
		CMD-Addr-Data	Dummy Clock Cycles	CMD- Addr-Data (S-D-D)	CMD- Addr-Data (S-S-S)	Dummy Clock Cycles		
Software Reset Operations								
Reset Enable	66h	1-0-0	0	8-0-0	8-0-0	0	0	0
Reset Memory	99h	1-0-0	0	8-0-0	8-0-0	0	0	0
Read ID Operations								
Read ID	9E/9Fh	1-0-(1)	0	8-0-(8)	8-0-(8)	8	0	1 to 4
Read Serial Flash Discovery Parameter	5Ah	1-1-(1)	8	8-8-(8)	8-8-(8)	8	3 (STR) 4 (DTR)	1 to ∞
Read Unique ID	4Bh	1-1-(1)	8	8-8-(8)	8-8-(8)	8	3(4)	1 to ∞
Read Memory Operations								
Read	03h	1-1-(1)	0	—	—	—	3(4)	1 to ∞
Fast Read	0Bh	1-1-(1)	8	8-8-(8)	8-8-(8)	16	3(4)	1 to ∞
Octal Output Fast Read	8Bh	1-1-(8)	8	8-8-(8)	8-8-(8)	16	3(4)	1 to ∞
Octal I/O Fast Read	CBh	1-8-(8)	16	8-8-(8)	8-8-(8)	16	3(4)	1 to ∞
Read Memory Operations with 4-Byte Address								
4-Byte Read	13h	1-1-(1)	0	—	—	—	4	1 to ∞
4-Byte Fast Read	0Ch	1-1-(1)	8	8-8-(8)	8-8-(8)	16	4	1 to ∞
4-Byte Octal Output Fast Read	7Ch	1-1-(8)	8	8-8-(8)	8-8-(8)	16	4	1 to ∞

4-Byte Octal I/O Fast Read	CCh	1-8-(8)	16	8-8-(8)	8-8-(8)	16	4	1 to ∞
4-Byte DTR Octal I/O Fast Read	FDh	1-8-(8)	16	8-8-(8)	8-8-(8)	16	4	1 to ∞
Write Operations								
Write Enable	06h	1-0-0	0	8-0-0	8-0-0	0	0	0
Write Disable	04h	1-0-0	0	8-0-0	8-0-0	0	0	0
Read Register Operations								
Read Status Register	05h	1-0-(1)	0	8-0-(8)	8-0-(8)	8	0	1 to ∞
Read Flag Status Register	70h	1-0-(1)	0	8-0-(8)	8-0-(8)	8	0	1 to ∞
Read Extended Addr. Register	C8h	1-0-(1)	0	8-0-(8)	8-0-(8)	8	0	1
Read Nonvolatile Configuration Register	B5h	1-1-(1)	8	8-8-(8)	8-8-(8)	8	3(4)	1
Read Volatile Configuration Register	85h	1-1-(1)	8	8-8-(8)	8-8-(8)	8	3(4)	1
Write Register Operations								
Write Status Register	01h	1-0-1	0	8-0-8	8-0-8	0	0	1
Write Extended Addr. Register	C5h	1-0-1	0	8-0-8	8-0-8	0	0	1
Volatile SR Write Enable	50h	1-0-0	0	8-0-0	8-0-0	0	0	0
Write Nonvolatile Configuration Register	B1h	1-1-1	0	8-8-8	8-8-8	0	3(4)	1
Write Volatile Configuration Register	81h	1-1-1	0	8-8-8	8-8-8	0	3(4)	1
Clear Flag Status Register Operation								
Clear Flag Status Register	30h	1-0-0	0	8-0-0	8-0-0	0	0	0
Program Operations								
Page Program	02h	1-1-1	0	8-8-8	8-8-8	0	3(4)	1 to 256
Octal Input Fast Program	82h	1-1-8	0	8-8-8	8-8-8	0	3(4)	1 to 256

Extended Octal Input Fast Program	C2h	1-8-8	0	8-8-8	8-8-8	0	3(4)	1 to 256
Program Operations with 4-Byte Address								
4-Byte Page Program	12h	1-1-1	0	8-8-8	8-8-8	0	4	1 to 256
4-Byte Octal Input Fast Program	84h	1-1-8	0	8-8-8	8-8-8	0	4	1 to 256
4-Byte Octal Input Extended Fast Program	8Eh	1-8-8	0	8-8-8	8-8-8	0	4	1 to 256
Erase Operations								
4KB Sector Erase	20h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
32KB Block Erase	52h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
64KB Block Erase	D8h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
Chip Erase	C7h/60h	1-0-0	0	8-0-0	8-0-0	0	0	0
Erase Operations with 4-Byte Address								
4-Byte 4KB Sector Erase	21h	1-1-0	0	8-8-8	8-8-0	0	4	0
4-Byte 32KB Block Erase	5Ch	1-1-0	0	8-8-8	8-8-0	0	4	0
4-Byte 64KB Block Erase	DCh	1-1-0	0	8-8-0	8-8-0	0	4	0
Suspend/Resume Operations								
Program/Erase Suspend	75h	1-0-0	0	8-0-0	8-0-0	0	0	0
Program/Erase Resume	7Ah	1-0-0	0	8-0-0	8-0-0	0	0	0
One-Time Programmable(OTP) Operations								
Read OTP Array	48h	1-1-(1)	8	8-8-(8)	8-8-(8)	16	3(4)	1 to ∞
Program OTP Array	42h	1-1-1	0	8-8-8	8-8-8	0	3(4)	1 to 256
Erase OTP Array	44h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
4-ByteAddress Mode Operations								
Enter 4-Byte Address Mode	B7h	1-0-0	0	8-0-0	8-0-0	0	0	0
Exit 4-Byte Address Mode	E9h	1-0-0	0	8-0-0	8-0-0	0	0	0
Deep Power-Down Operations								
Enter Deep Power Down	B9h	1-0-0	0	8-0-0	8-0-0	0	0	0

Release From Deep Power Down	ABh	1-0-0	0	8-0-0	8-0-0	0	0	0
Advanced Sector Protection Operations								
Individual sector lock	36h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
Individual sector unlock	39h	1-1-0	0	8-8-0	8-8-0	0	3(4)	0
Read sector lock	3Dh	1-1-(1)	0	8-8-(8)	8-8-(8)	8	3(4)	1
Global sector lock	7Eh	1-0-0	0	8-0-0	8-0-0	0	0	0
Global sector unlock	98h	1-0-0	0	8-0-0	8-0-0	0	0	0

Table of ID Definitions
GD25LX256E

Operation Code	M7-M0	ID23-ID16	ID15-ID8	ID7-ID0
9E/9FH	C8	68	19	FF

9.1. Enable 4-byte Mode (B7H)

The Enable 4-byte Mode command enables accessing the address length of 32-bit for the memory area of the higher density (larger than 128Mb). The GD25LX256E default is in 24-bit address mode. After sending the Enable 4-byte Mode command, the ADS bit (FS0) will be set to 1 to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24 bit. The Disable 4-byte mode or Reset or Power-off will disable 4-byte mode.

Figure 8. Enable 4-byte Mode Sequence Diagram (SPI)

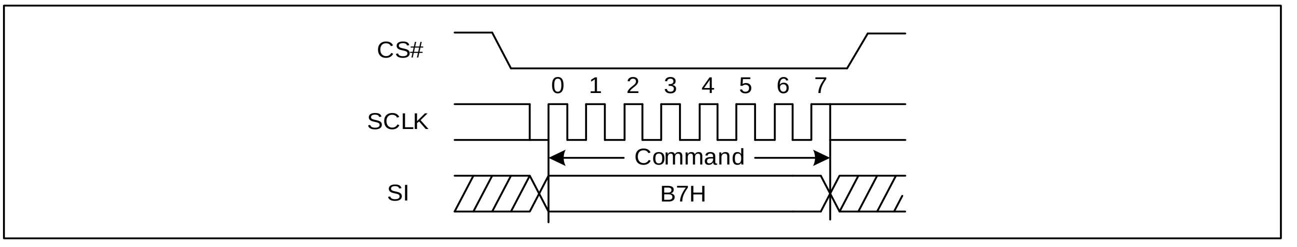
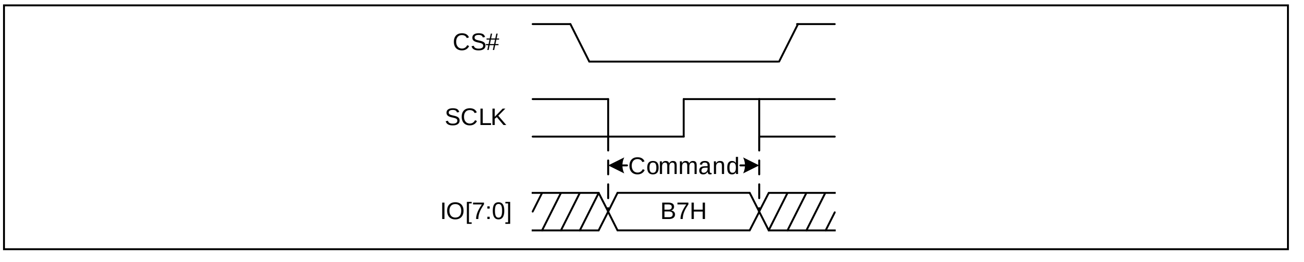


Figure 9. Enable 4-byte Mode Sequence Diagram (OPI)



9.2. Disable 4-byte Mode (E9H)

The Disable 4-byte Mode command is executed to exit the 4-byte address mode and return to the default 3-byte address mode. After sending the Disable 4-byte Mode command, the ADS bit (FS0) will be clear to be 0 to indicate the 4-byte address mode has been disabled, and then the address length will return to 24-bit.

Figure 10. Disable 4-byte Mode Sequence Diagram (SPI)

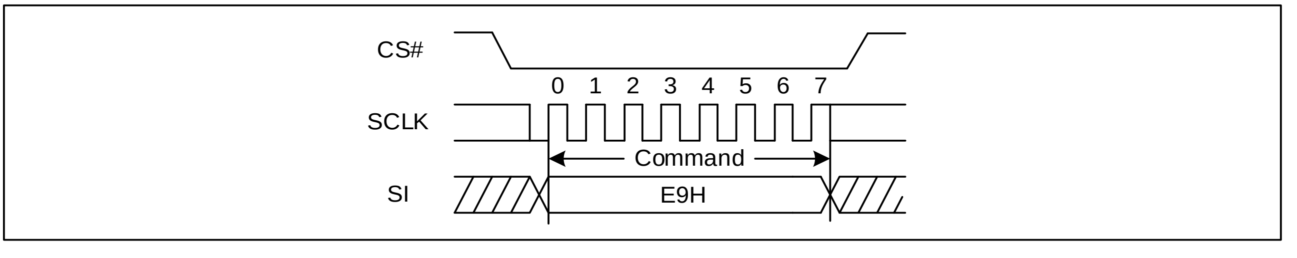
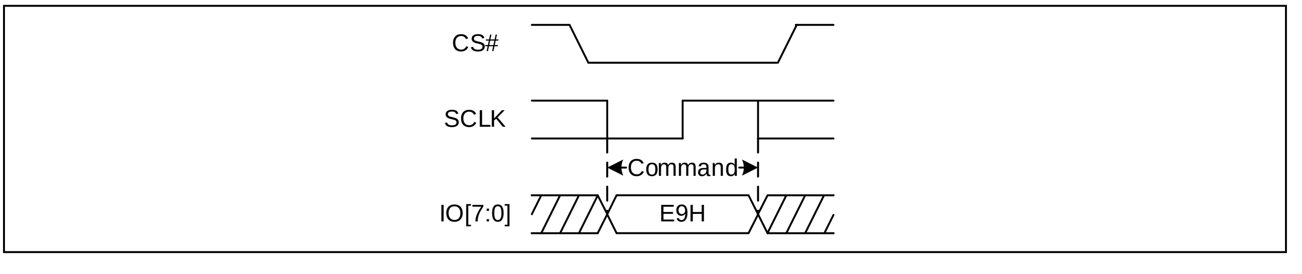


Figure 11. Disable 4-byte Mode Sequence Diagram (OPI)



9.3. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Extended Address Register (WEAR), Write Nonvolatile/Volatile configure register and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 12. Write Enable Sequence Diagram (SPI)

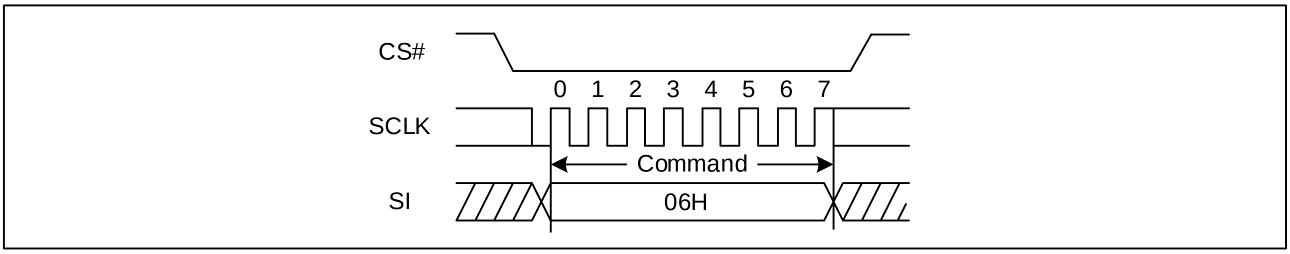
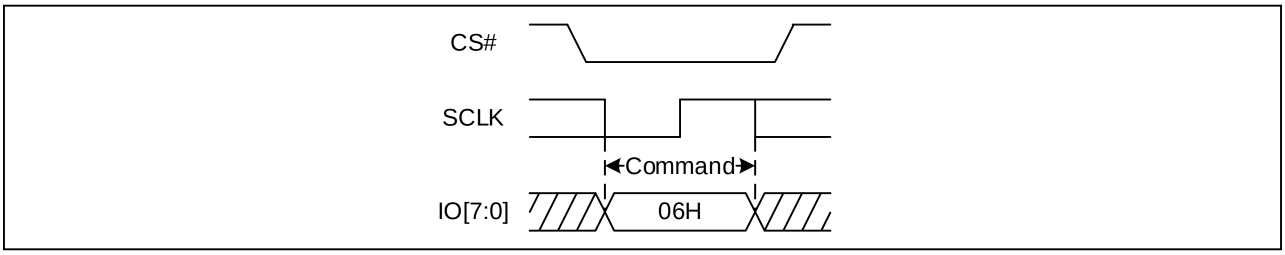


Figure 13. Write Enable Sequence Diagram (OPI)



9.4. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Write Extended Address Register (WEAR), Write Nonvolatile/Volatile configure register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Registers and Reset commands.

Figure 14. Write Disable Sequence Diagram (SPI)

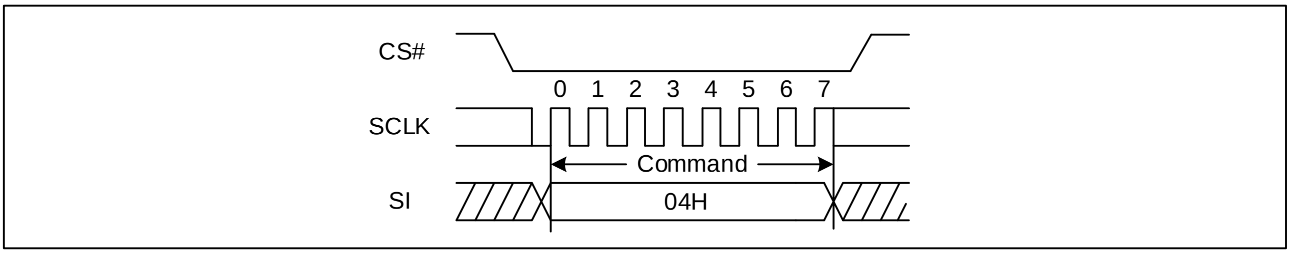
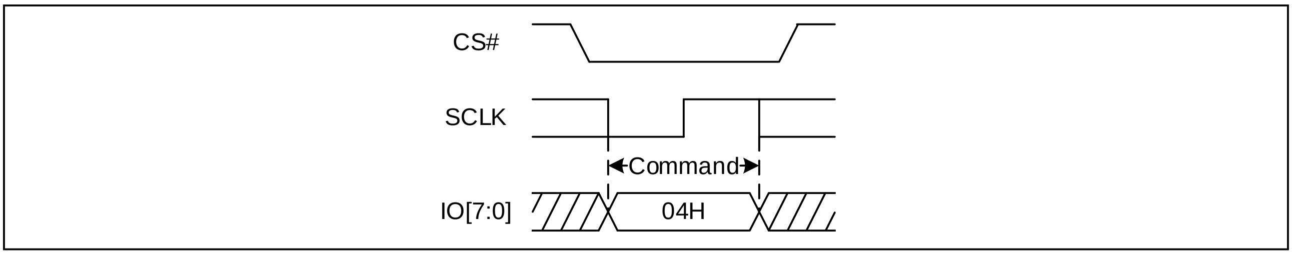


Figure 15. Write Disable Sequence Diagram (OPI)



9.5. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command, and any other commands cannot be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 16. Write Enable for Volatile Status Register Sequence Diagram (SPI)

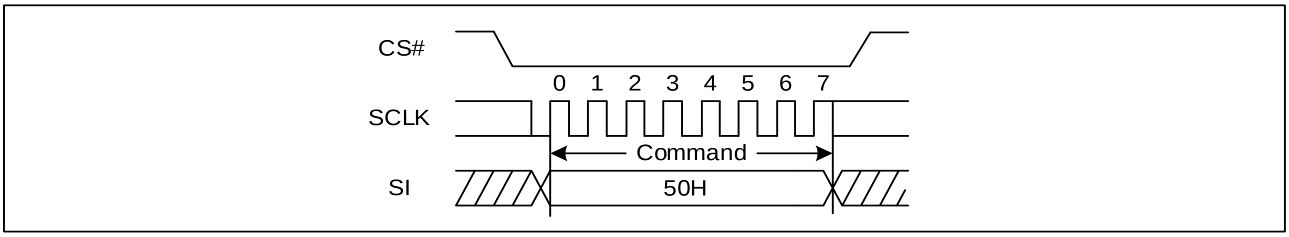
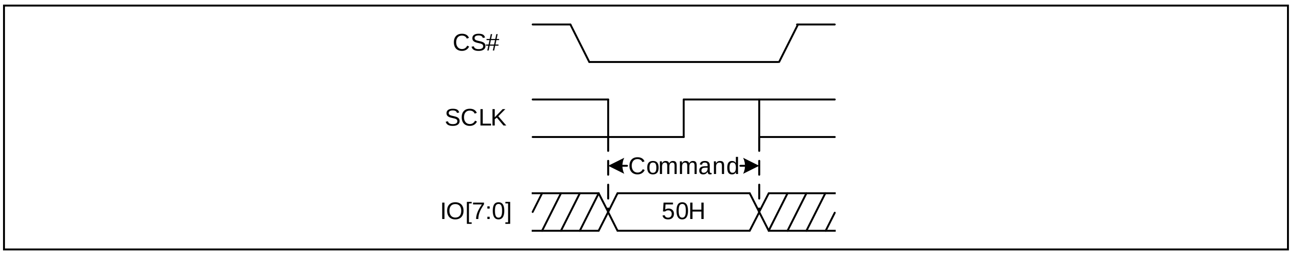


Figure 17. Write Enable for Volatile Status Register Sequence Diagram (OPI)



9.6. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on Byte2 of the Status Register. CS# must be driven high after the eighth of the data Byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (TB, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP0) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 18. Write Status Register Sequence Diagram (SPI)

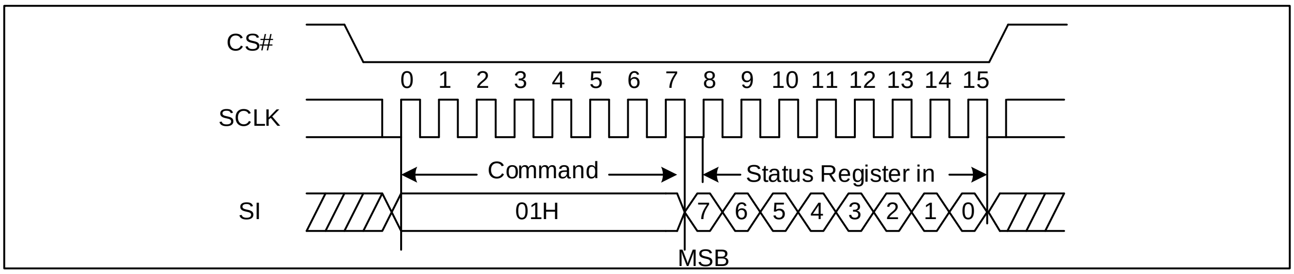
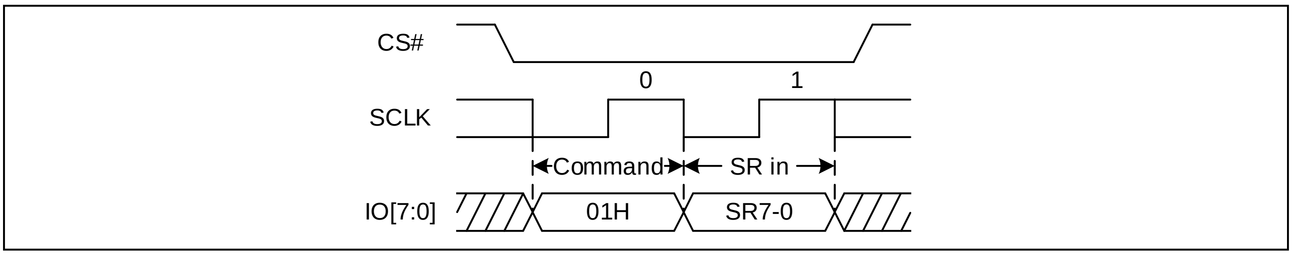


Figure 19. Write Status Register Sequence Diagram (OPI)



9.7. Write Extended Register (C5H)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06H) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “C5H”, and then writing the Extended Address Register data byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 20. Write Extended Register Sequence Diagram (SPI)

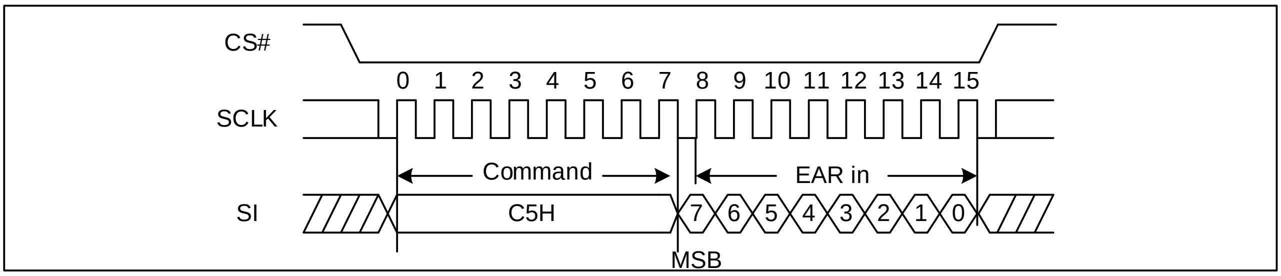
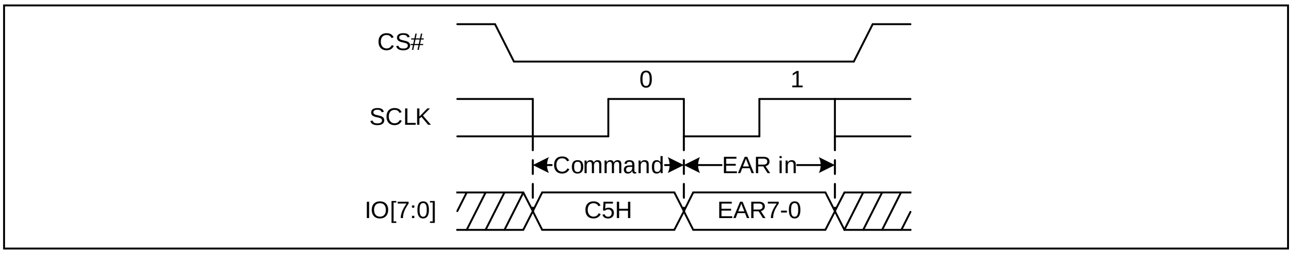


Figure 21. Write Extended Register Sequence Diagram (OPI)

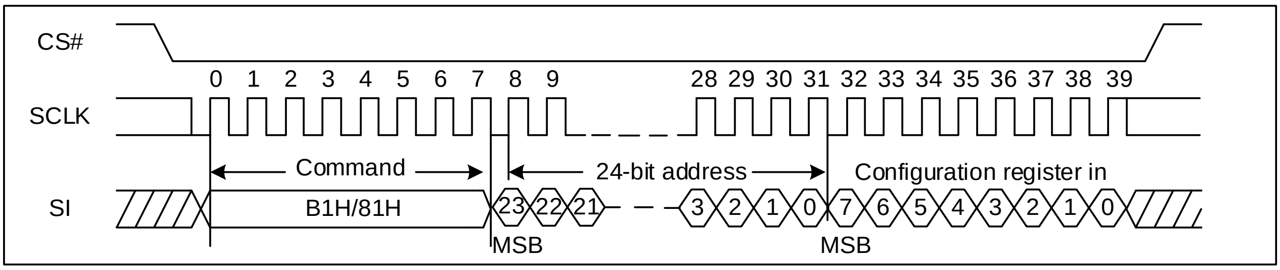


9.8. Write Nonvolatile/Volatile Configuration Register (WRCR) (B1H/81H)

The Write Nonvolatile/Volatile Configuration Register (WRCR) command allows new values to be written to the Nonvolatile/Volatile Configuration Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

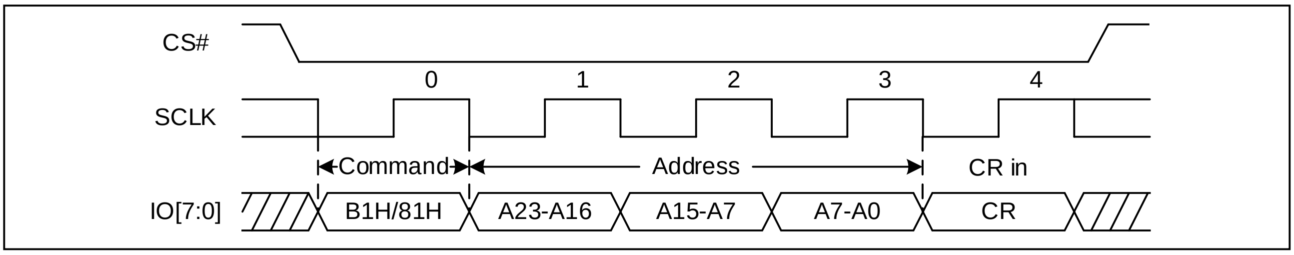
CS# must be driven high after the data Byte has been latched in. If not, the Write Configuration Register (WRCR) command is not executed. As soon as CS# is driven high, the self-timed Write Configuration Register cycle is initiated. While the Write Configuration Register cycle is in progress, the Configuration Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Configuration Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 22. Write Nonvolatile/Volatile Configuration Register Sequence Diagram (SPI)



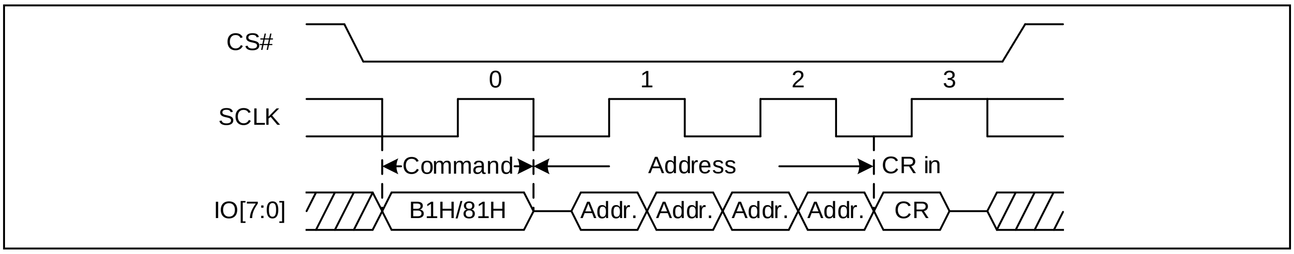
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 23. Write Nonvolatile/Volatile Configuration Register Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 24. Write Nonvolatile/Volatile Configuration Register Sequence Diagram (DTR OPI)



9.9. Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. The SO will output Status Register bits S7~S0.

Figure 25. Read Status Register Sequence Diagram (SPI)

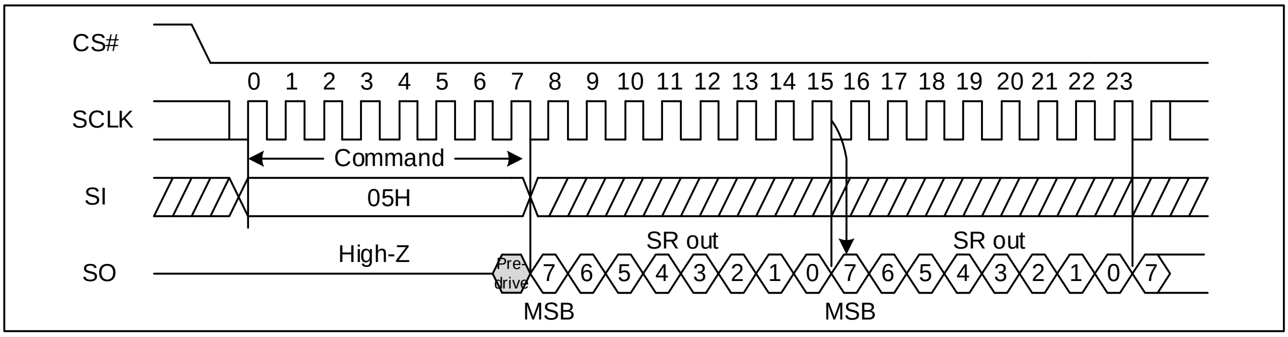


Figure 26. Read Status Register (RDSR) Sequence (STR OPI)

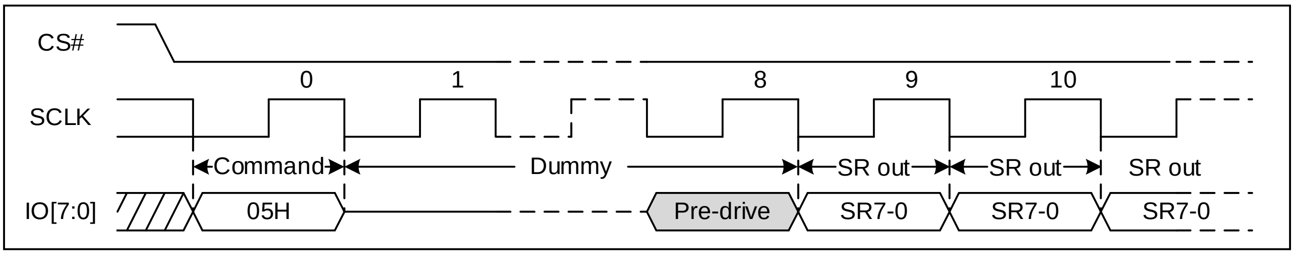
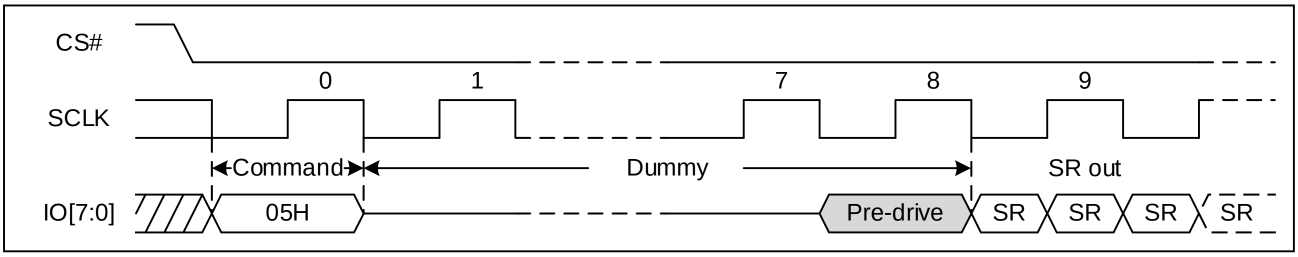


Figure 27. Read Status Register (RDSR) Sequence (DTR OPI)



9.10. Read Flag Status Register (RDSR) (70H)

The Read Flag Status Register command is for reading the Flag Status Register. The Flag Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Flag Status Register continuously. The SO will output Status Register bits FS7~FS0.

Figure 28. Read Status Register Sequence Diagram (SPI)

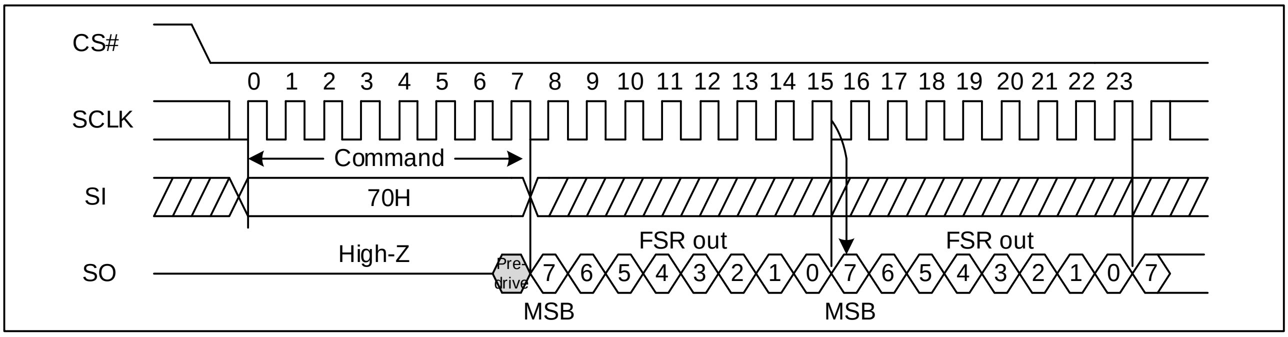


Figure 29. Read Status Register (RDSR) Sequence (STR OPI)

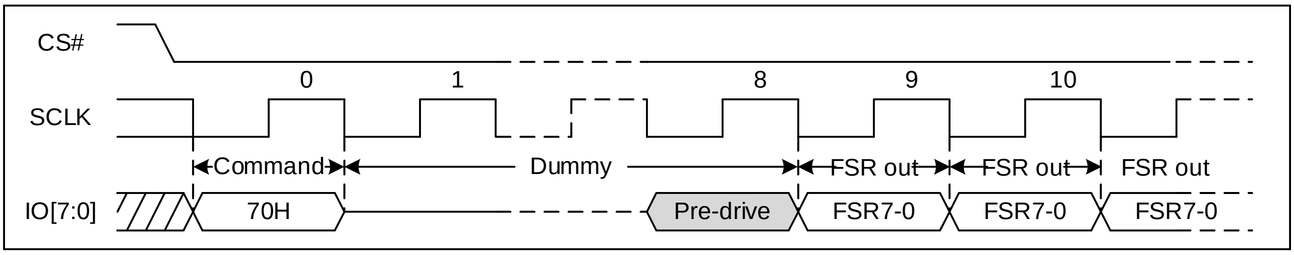
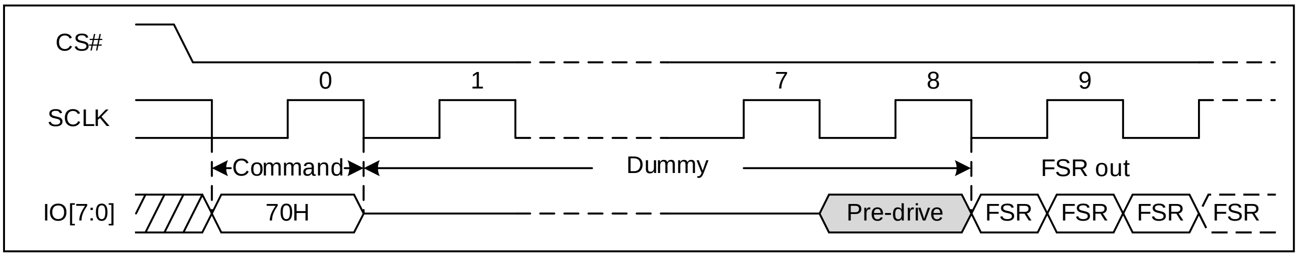


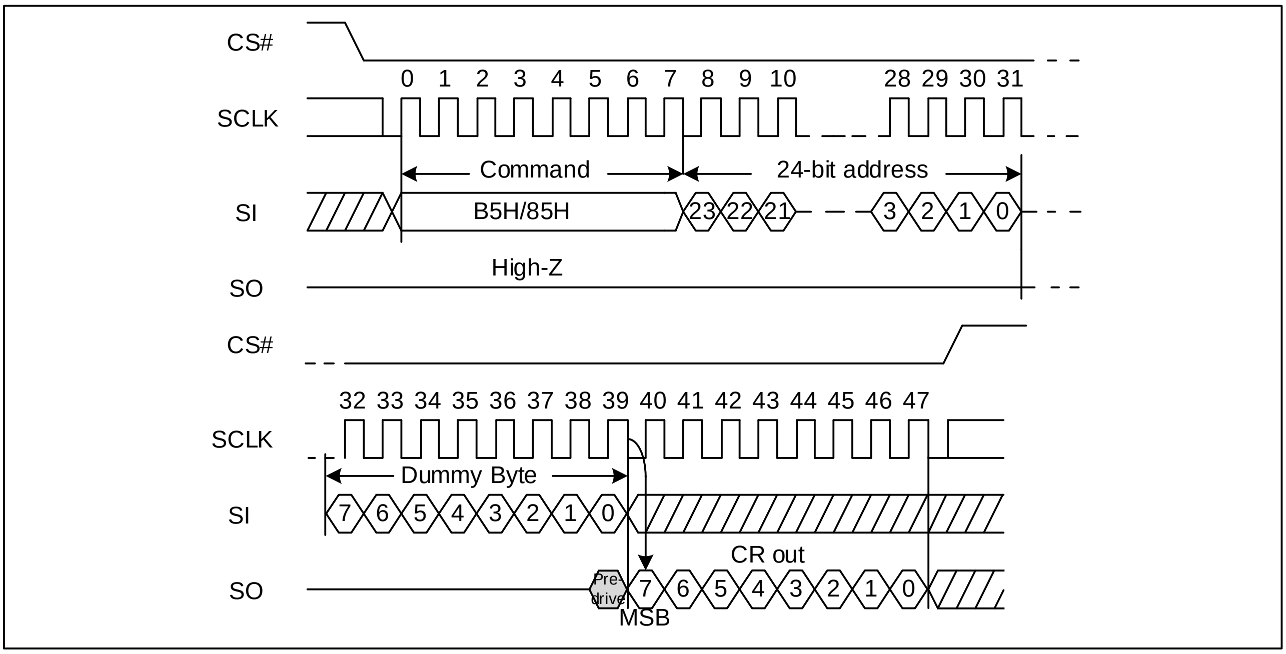
Figure 30. Read Status Register (RDSR) Sequence (DTR OPI)



9.11. Read Nonvolatile/Volatile Configuration Register (B5H/85H)

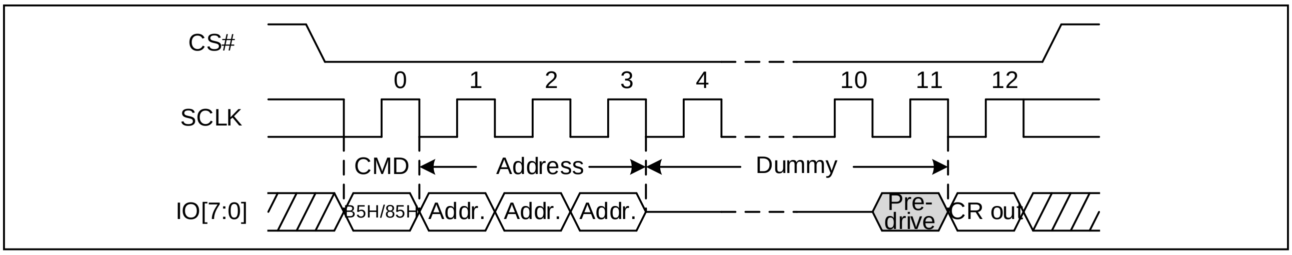
The Nonvolatile/Volatile Configuration Register command is for reading the Nonvolatile/Volatile Configuration Registers. It is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the Configuration Register, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of SCLK. Read Nonvolatile/Volatile Configuration Register command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 31. Read Configuration Registers Sequence Diagram (SPI)



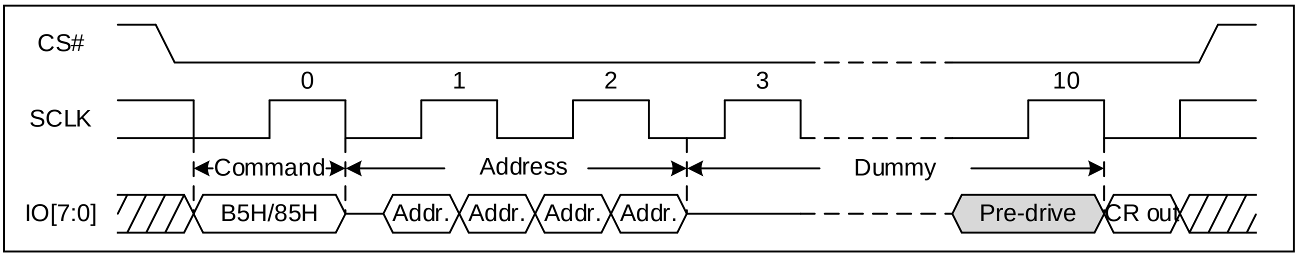
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 32. Read Configuration Registers Sequence (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 33. Read Configuration Registers Sequence (DTR OPI)



9.12. Read Extended Register (C8H)

Extended Register contains ECC Status Bit and Address Bit A24. The Read Extended Register instruction is entered by driving CS# low and shifting the instruction code “C8H” into the SI pin on the rising edge of SCLK. The Extended Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first.

When the device is in the 4-Byte Address Mode, the value of A24 bit is ignored.

Figure 34. Read Extended Register Sequence Diagram (SPI)

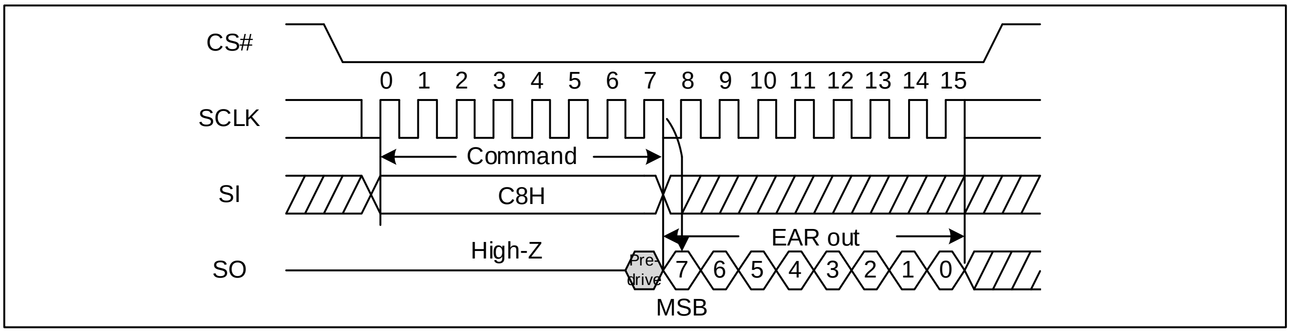


Figure 35. Read Extended Register Sequence Diagram (STR OPI)

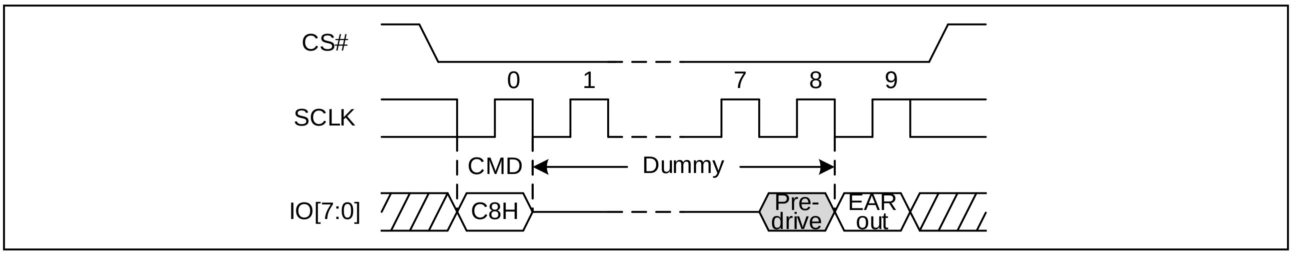
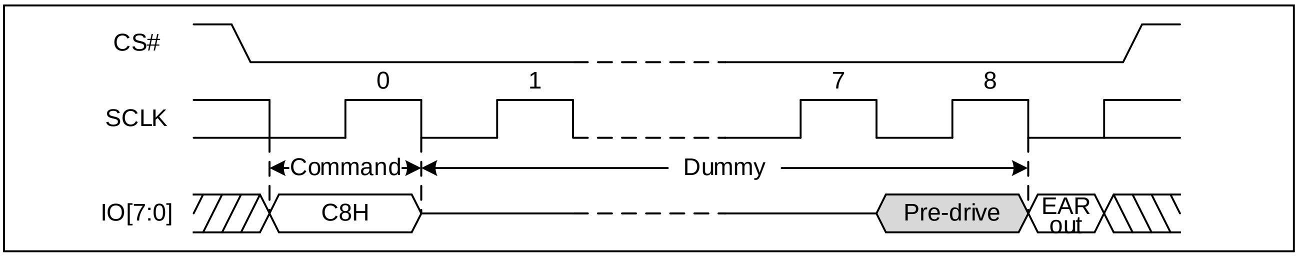


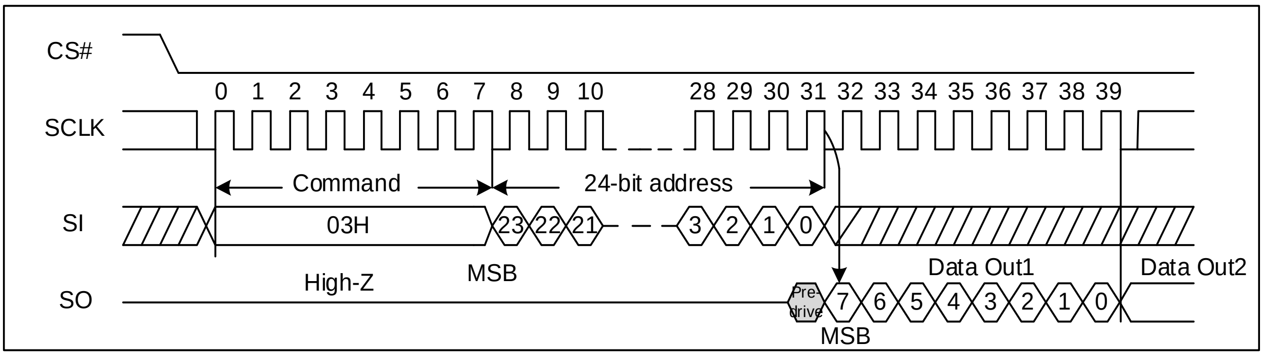
Figure 36. Read Extended Register Sequence Diagram (DTR OPI)



9.13. Read Data Bytes (READ) (03H/13H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fR, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 37. Read Data Bytes Sequence Diagram



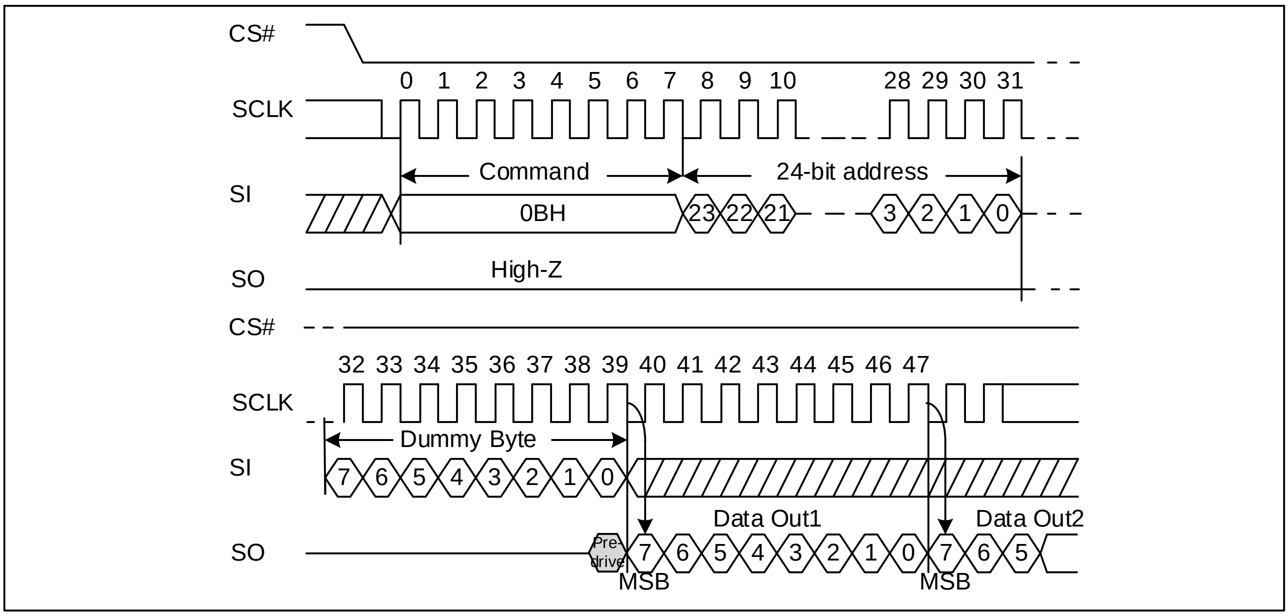
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

9.14. Read Data Bytes at Higher Speed (Fast Read) (0BH/0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) or a 4-byte address (A31-A0) and dummy clocks, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

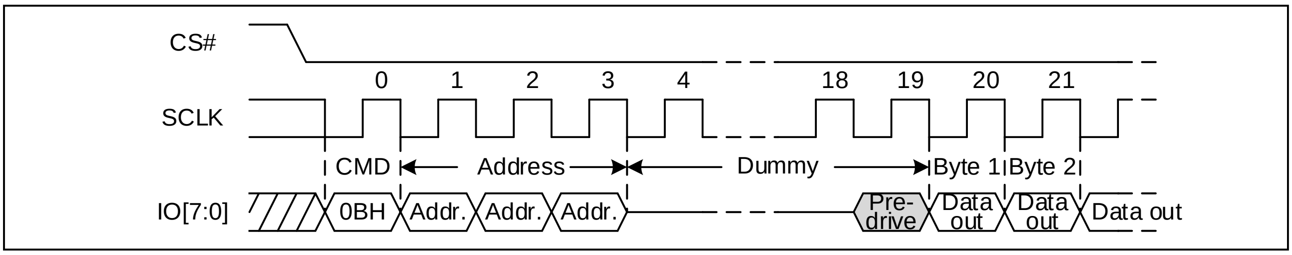
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 38. Read Data Bytes at Higher Speed Sequence Diagram (SPI)



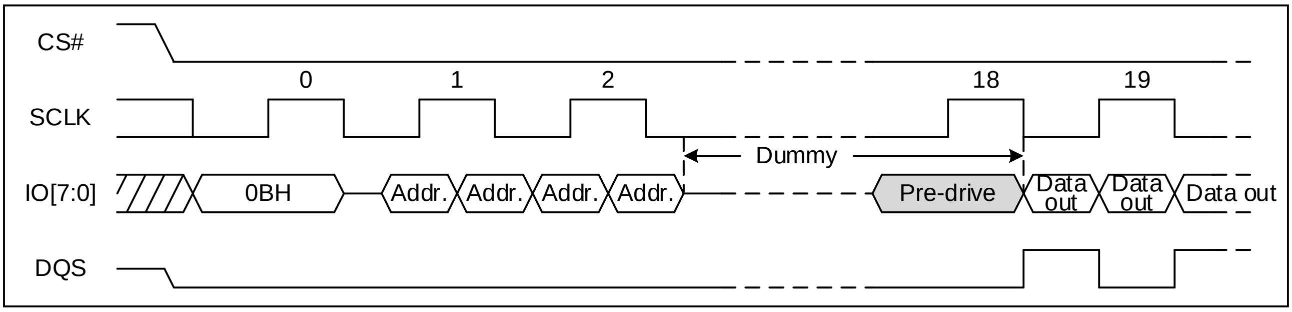
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 39. Read Data Bytes at Higher Speed Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 40. Read Data Bytes at Higher Speed Sequence Diagram (DTR OPI)

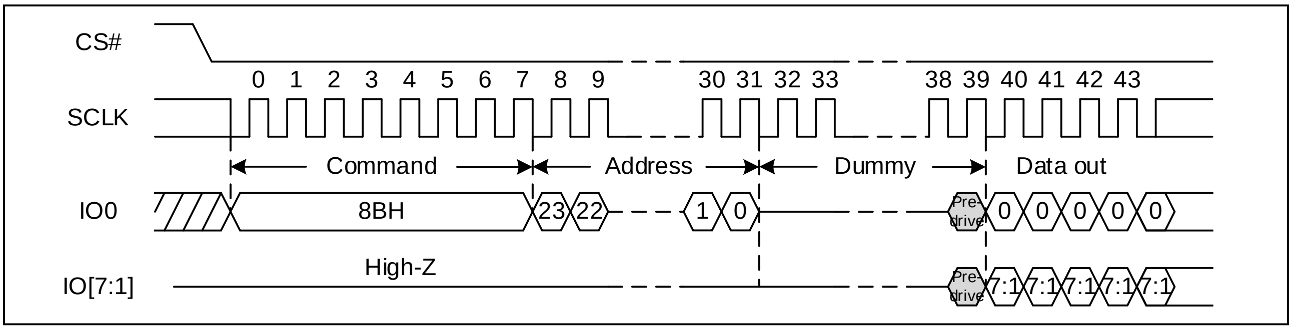


9.15. Octal Output Fast Read (8BH/7CH)

The Octal Output Fast Read command is followed by 3-byte address (A23-A0) or a 4-byte address (A31-A0) and dummy clocks, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 8-bit per clock cycle from IO7, IO6, IO5, IO4, IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

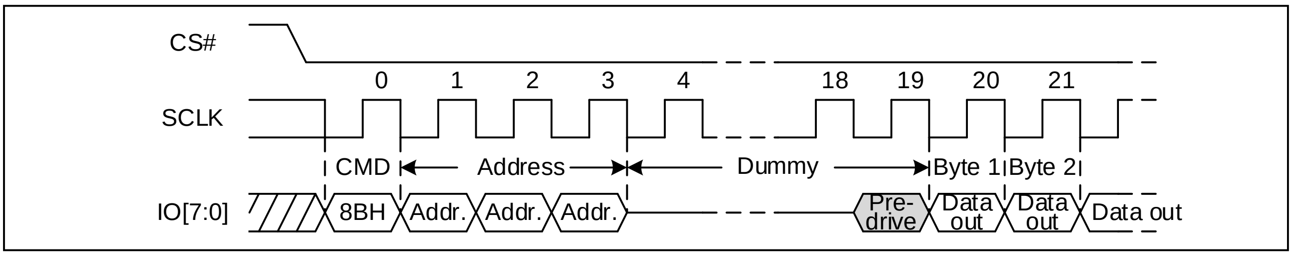
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 41. Octal Output Fast Read Sequence Diagram (SPI)



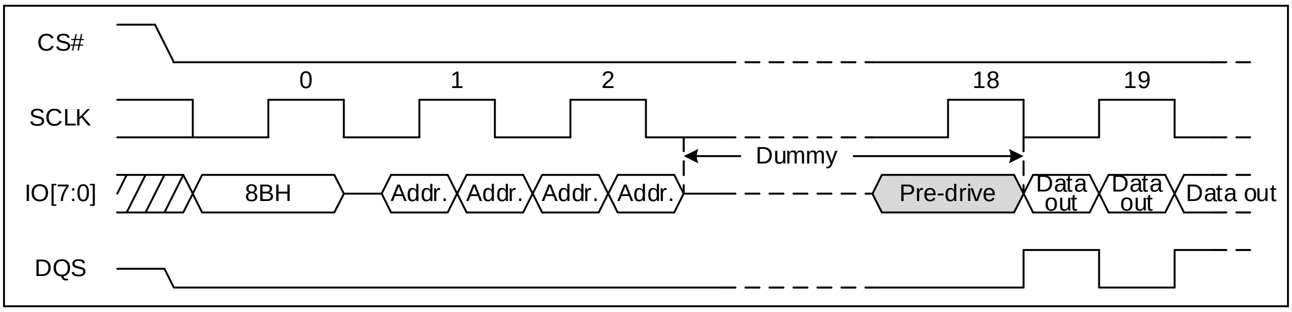
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 42. Octal Output Fast Read Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 43. Octal Output Fast Read Sequence Diagram (DTR OPI)

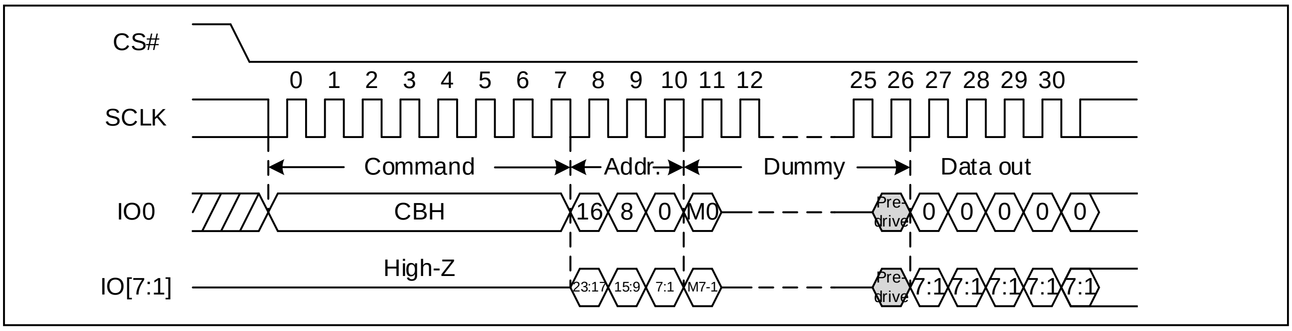


9.16. Octal I/O Fast Read (CBH/CCH)

The Octal I/O Fast Read command is similar to the Octal Output Fast Read command but with the capability to input the 3-byte address (A23-0) or a 4-byte address (A31-A0) and a “Continuous Read Mode” byte and dummy clocks. 8-bit per clock is transferred by IO[7:0] and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO[7:0]. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

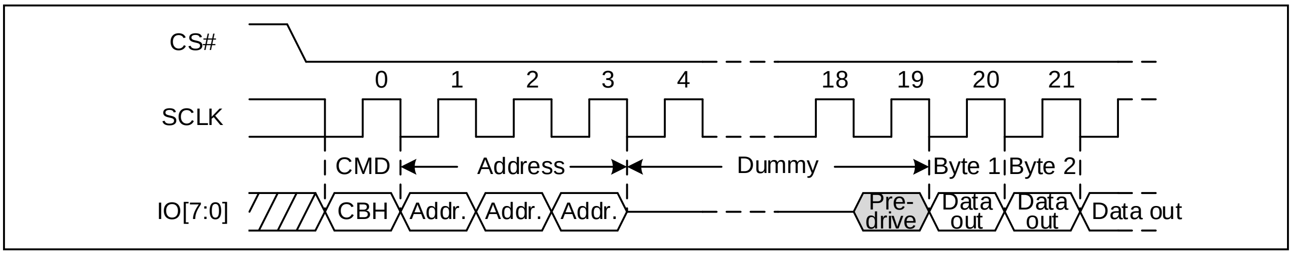
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 44. Octal I/O Fast Read Sequence Diagram (SPI, M5-4 ≠ (1, 0))



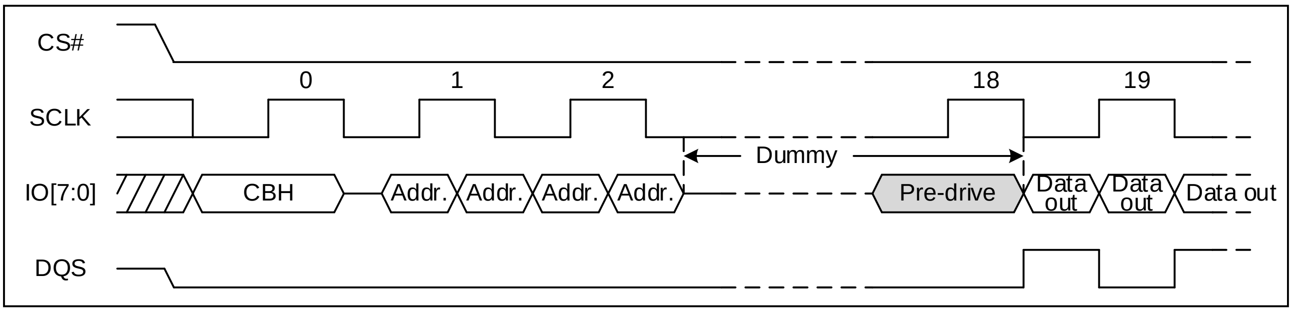
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 45. Octal I/O Fast Read Sequence Diagram (STR OPI, M5-4 ≠ (1, 0))



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

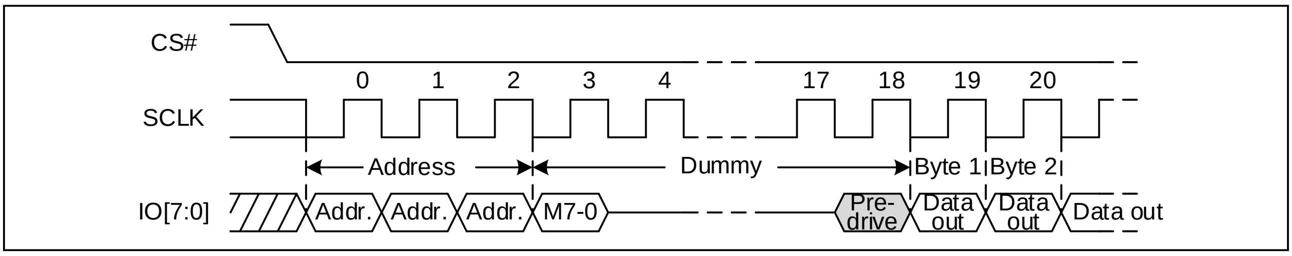
Figure 46. Octal Output Fast Read Sequence Diagram (DTR OPI, M5-4 ≠ (1, 0))



Octal I/O Fast Read with "Continuous Read Mode"

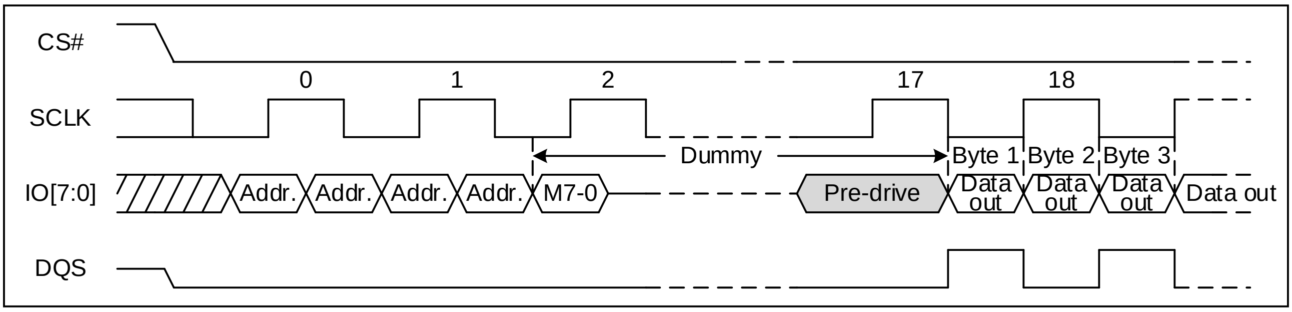
The Octal I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0) or a 4-byte address (A31-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Octal I/O Fast Read command (after CS# is raised and then lowered) does not require the CBH/CCH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first CBH/CCH command code, thus returning to normal operation.

Figure 47. Octal I/O Fast Read Sequence Diagram (STR, M5-4 = (1, 0))



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 48. Octal Output Fast Read Sequence Diagram (DTR OPI, M5-4 = (1, 0))



Octal I/O Fast Read with "16/32/64-Byte Wrap Around"

The Octal I/O Fast Read command can be used to access a specific portion within a page by issuing Wrap configuration register byte prior to CBH/CCH. The data being accessed can be limited to either a 16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-byte) of data without issuing multiple read commands.

9.17. Octal I/O DTR Read (FDH)

The Octal I/O DTR Read command enables Double Transfer Rate throughput on Octal I/O of Serial Flash in read mode. The address (interleave on 8 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 8 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock edge, and 8-bit data can be read out at one clock edge, which means 8 bits at rising edge of clock, the other 8 bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single Octal I/O DTR Read command. The address counter rolls over to 0 when the highest address has been reached. Once writing Octal I/O DTR Read command, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DTROIO instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 49. DTR Octal I/O Fast Read Sequence Diagram (SPI)

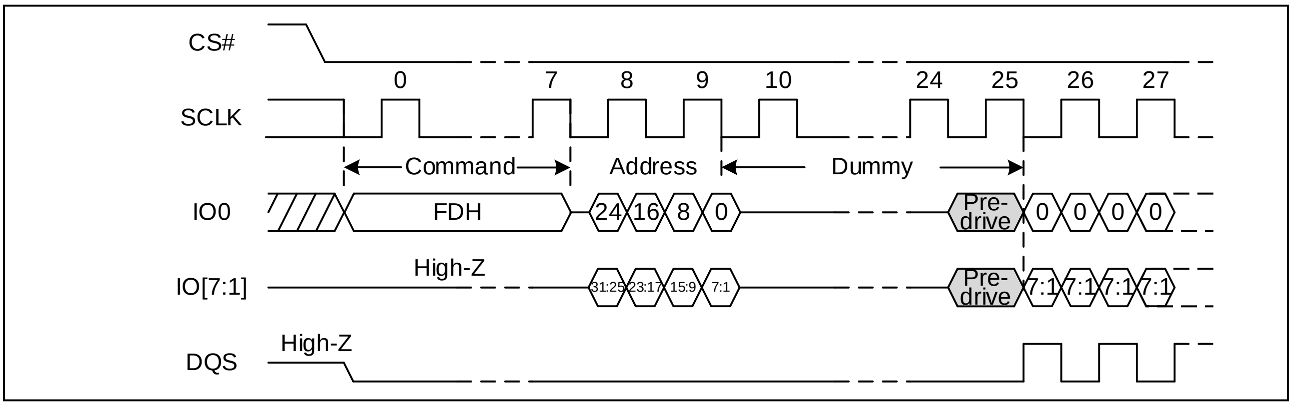
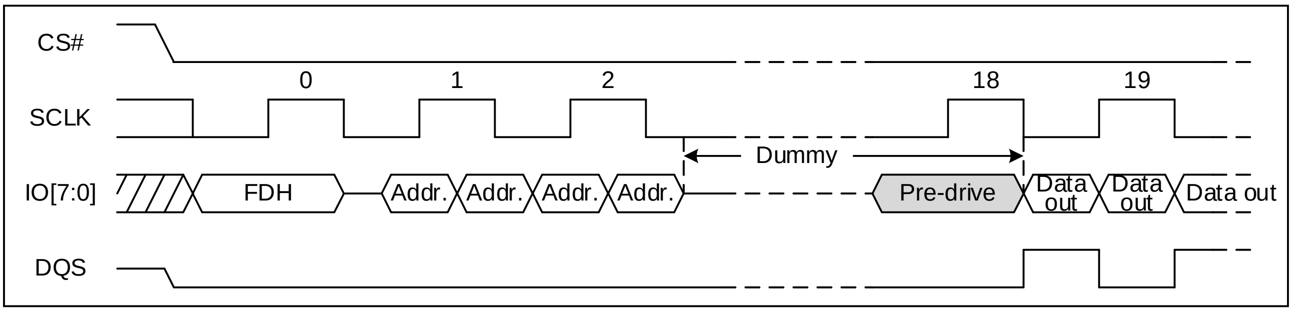


Figure 50. Octal Output Fast Read Sequence Diagram (OPI)



9.18. Page Program (PP) (02H/12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

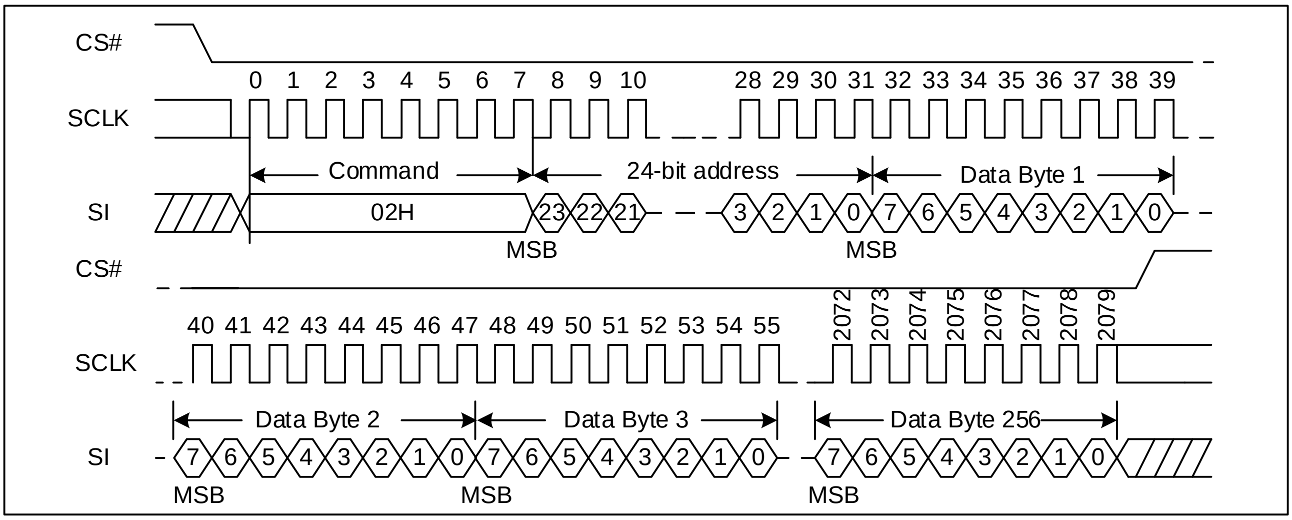
The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address or 4-byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

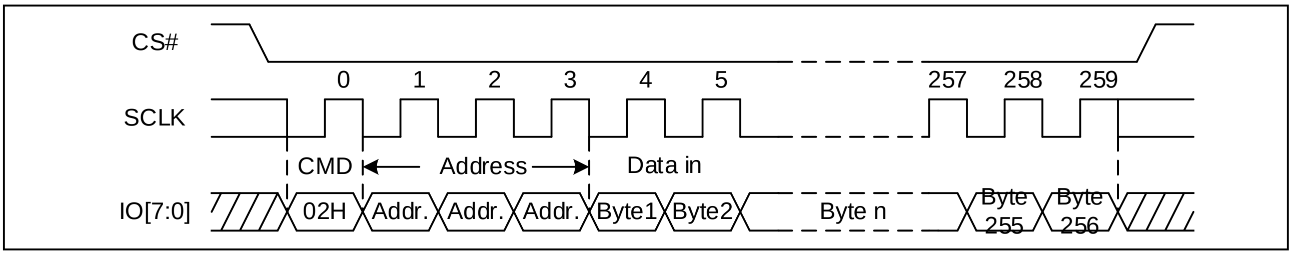
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 51. Page Program Sequence Diagram (SPI)



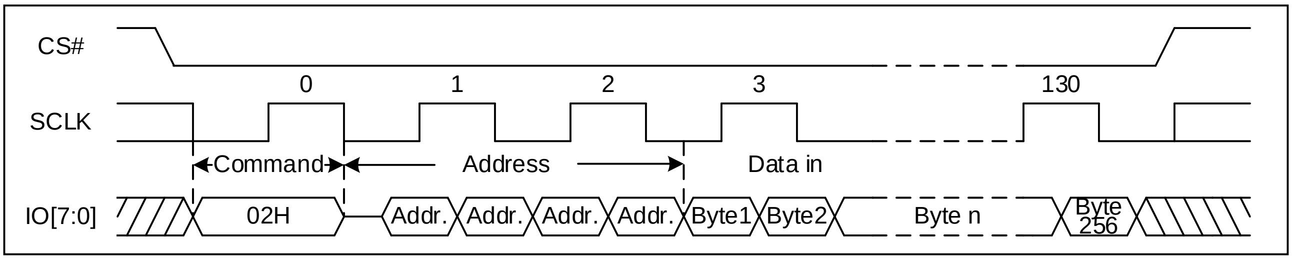
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 52. Page Program Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 53. Page Program Sequence Diagram (DTR OPI)



9.19. Octal Page Program (82H/84H)

The Octal Page Program command is for programming the memory using four pins: IO0, IO1, IO2, IO3, IO4, IO5, IO6 and IO7. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Octal Page Program command is entered by driving CS# Low, followed by the command code (82H/84H), three or four address bytes and at least one data byte on IO pins.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Octal Page Program (PP) command is not executed.

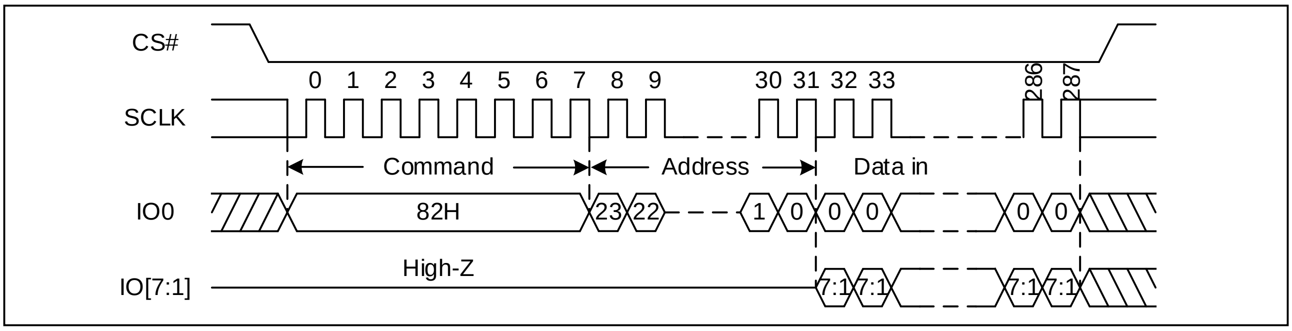
As soon as CS# is driven high, the self-timed Octal Page Program cycle (whose duration is t_{PP}) is initiated. While the Octal Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit.

The Write in Progress (WIP) bit is 1 during the self-timed Octal Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Octal Page Program command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

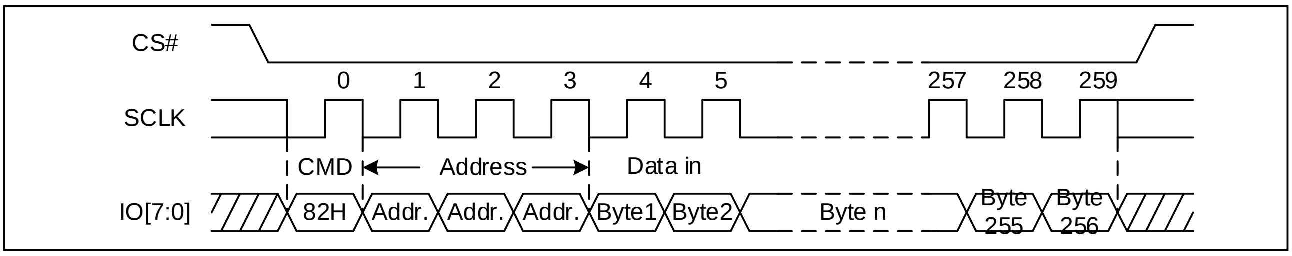
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even

Figure 54. Octal Page Program Sequence Diagram (SPI)



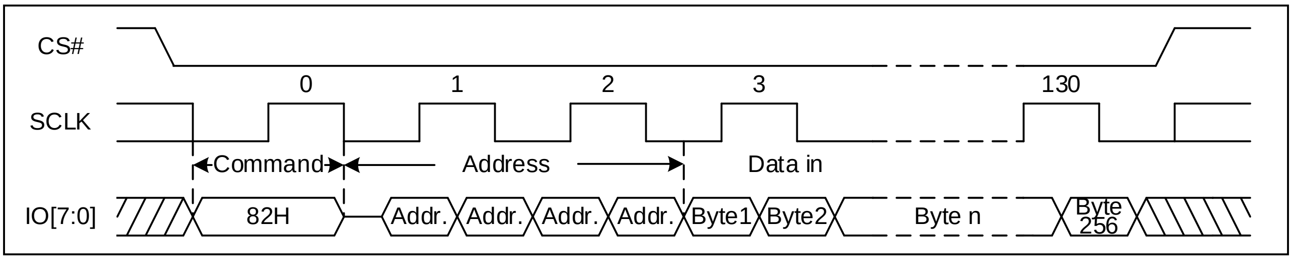
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 55. Page Program Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 56. Page Program Sequence Diagram (DTR OPI)



9.20. Extend Octal Page Program (C2H/8EH)

The Extend Octal Page Program command is for programming the memory using eight pins: IO0, IO1, IO2, IO3, IO4, IO5, IO6 and IO7. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend Octal Page Program command is entered by driving CS# Low, followed by the command code (C2H/8EH), three or four address bytes and at least one data byte on IO pins.

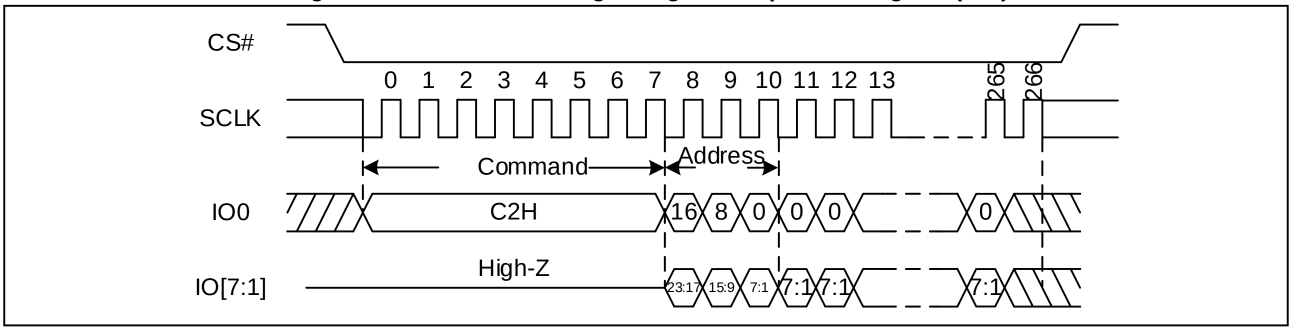
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Extend Octal Page Program (EPP) command is not executed.

As soon as CS# is driven high, the self-timed Extend Octal Page Program cycle (whose duration is tPP) is initiated. While the Extend Octal Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Octal Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

An Extend Octal Page Program command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

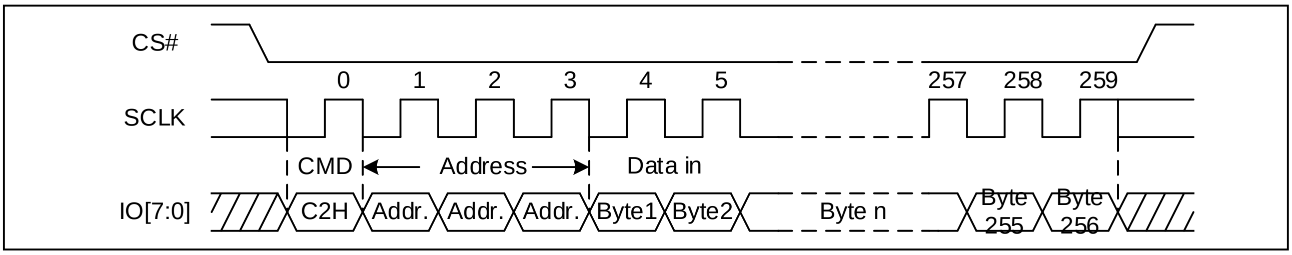
In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

Figure 57. Extend Octal Page Program Sequence Diagram (SPI)



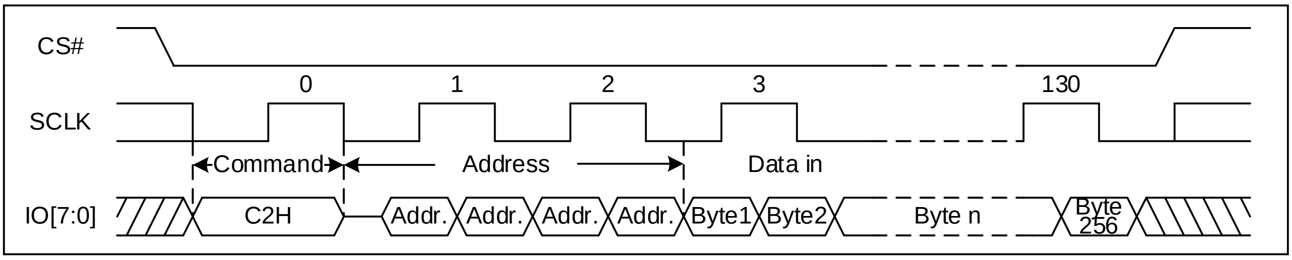
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 58. Page Program Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

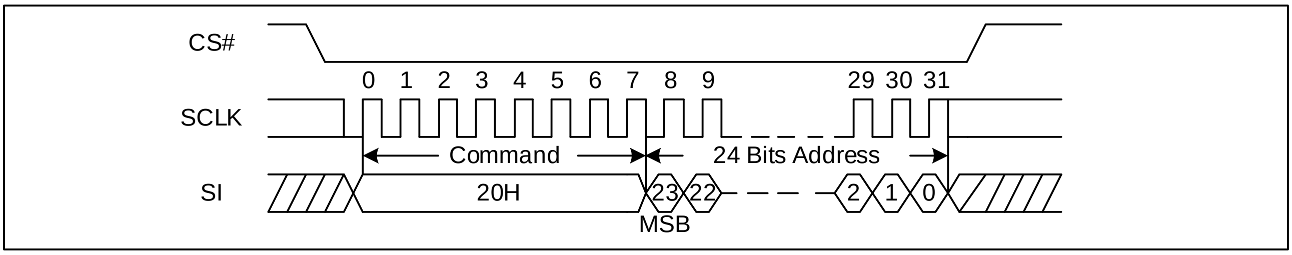
Figure 59. Page Program Sequence Diagram (DTR OPI)



9.21. Sector Erase (SE) (20H/21H)

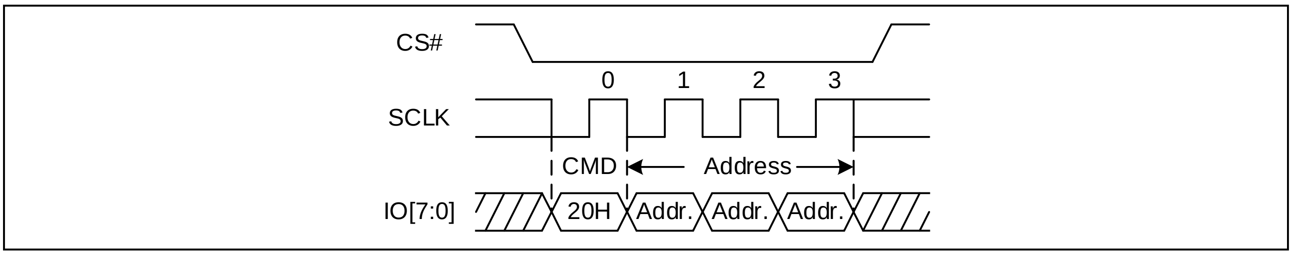
The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3- byte address or 4-byte address on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence. The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address or 4-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 60. Sector Erase Sequence Diagram (SPI)



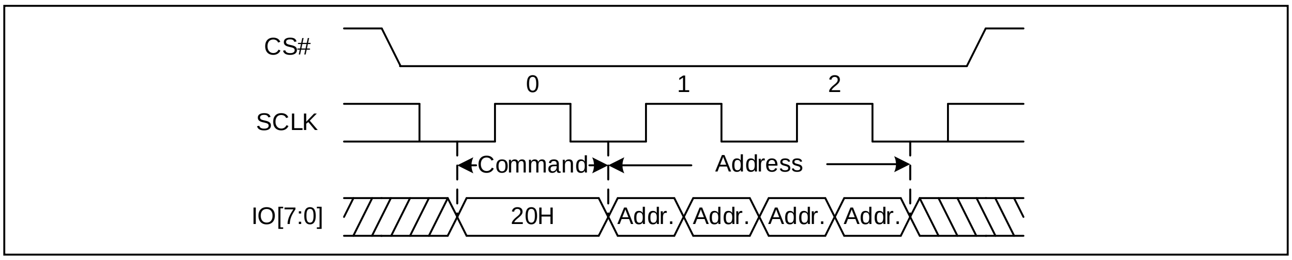
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 61. Sector Erase Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 62. Sector Erase Sequence Diagram (DTR OPI)

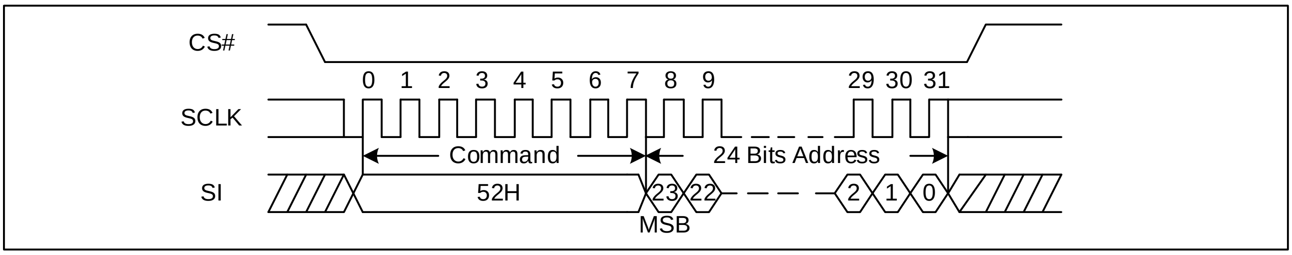


9.22. 32KB Block Erase (BE) (52H/5CH)

The 32KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and 3-byte address or 4-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

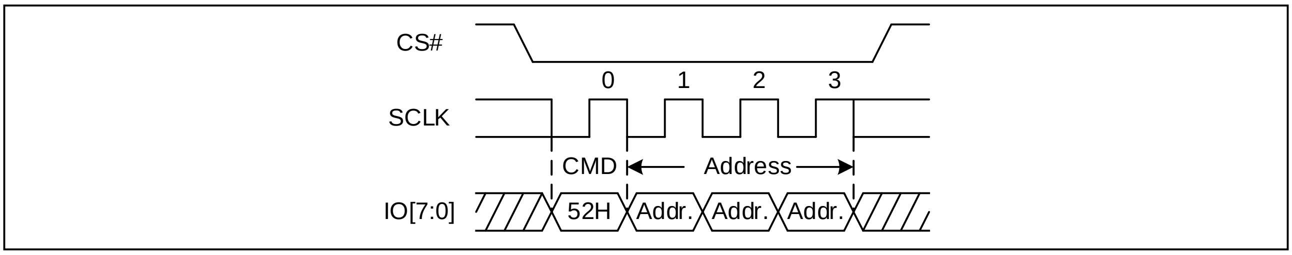
The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address or 4-byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 63. 32KB Block Erase Sequence Diagram (SPI)



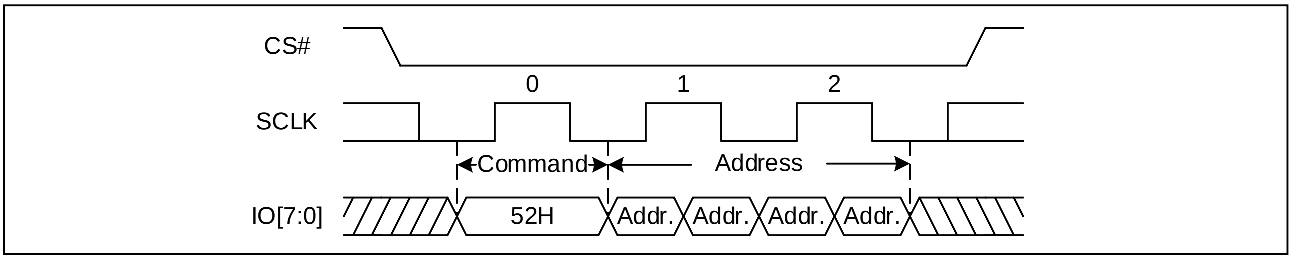
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 64. 32KB Block Erase Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 65. 32KB Block Erase Sequence Diagram (DTR OPI)

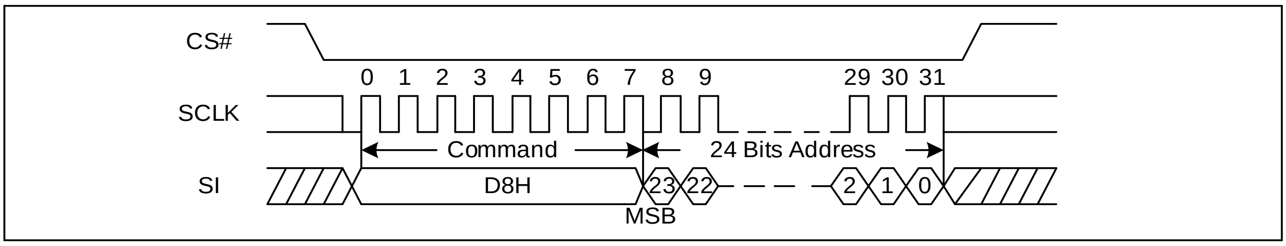


9.23. 64KB Block Erase (BE) (D8H/DCH)

The 64KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and 3-byte address or 4-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

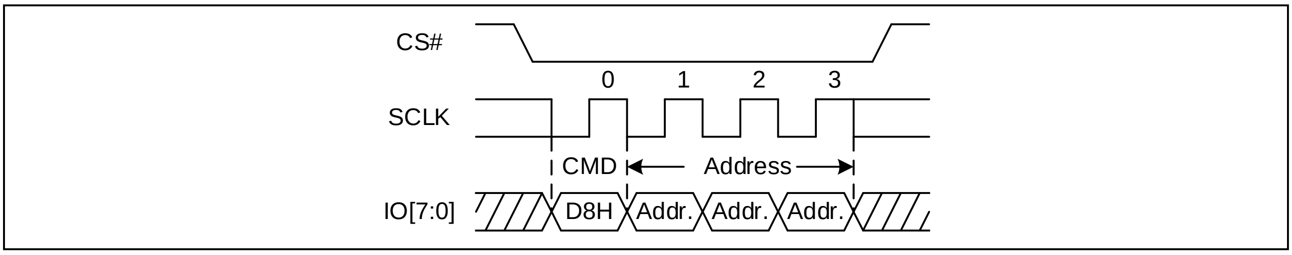
The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address or 4-byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 66. 64KB Block Erase Sequence Diagram (SPI)



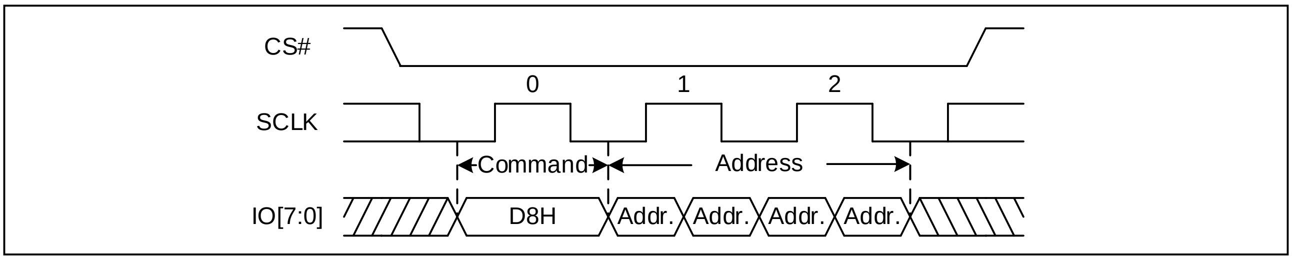
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 67. 64KB Block Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 68. 64KB Block Sequence Diagram (DTR OPI)



9.24. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence. The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, and BP0) bits are 0 The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 69. Chip Erase Sequence Diagram (SPI)

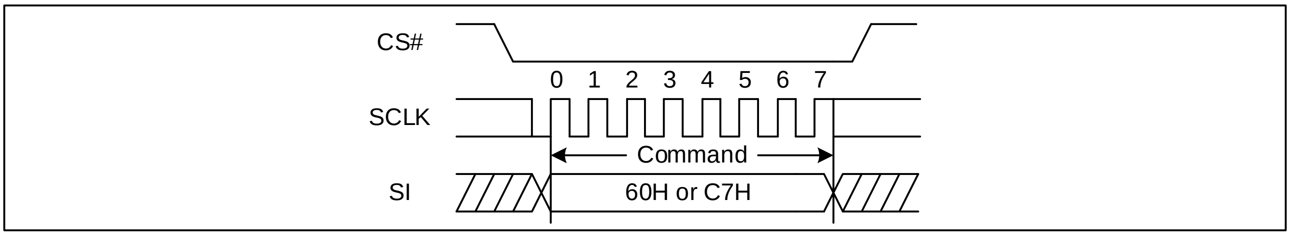
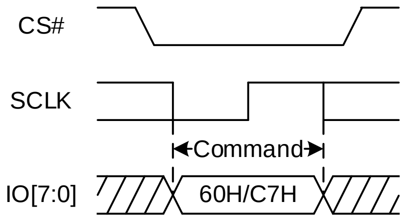


Figure 70. Chip Erase Sequence Diagram (OPI)



9.25. Clear SR Flags (30H)

The Clear Status Register Flags command resets bit FS1 (Protection), FS4 (Program Error bit) and FS5 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be not accepted even when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

Figure 71.Clear Status Register Flags Sequence Diagram (SPI)

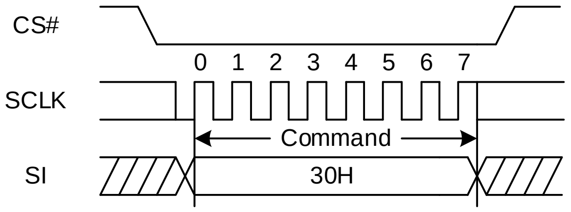
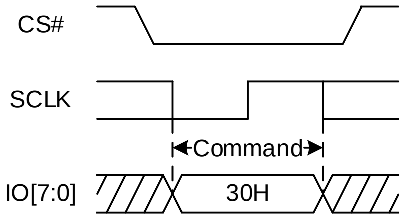


Figure 72. Clear Status Register Flags Sequence Diagram (OPI)



9.26. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABH) or Enable Reset (66H) and Reset (99H) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or

Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 73. Deep Power-Down Sequence Diagram (SPI)

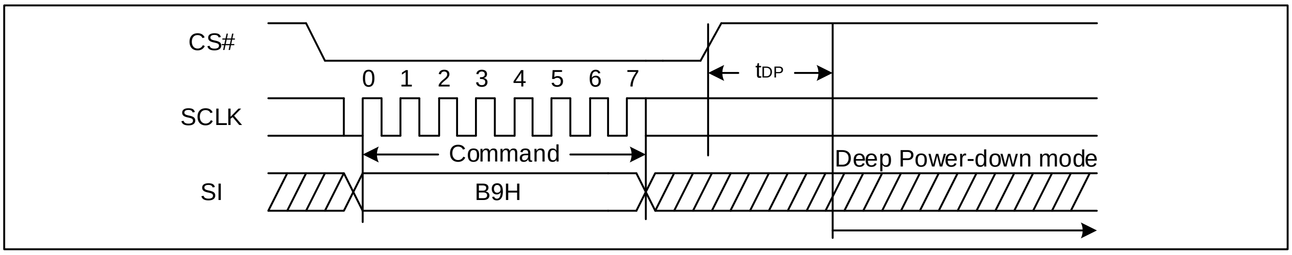
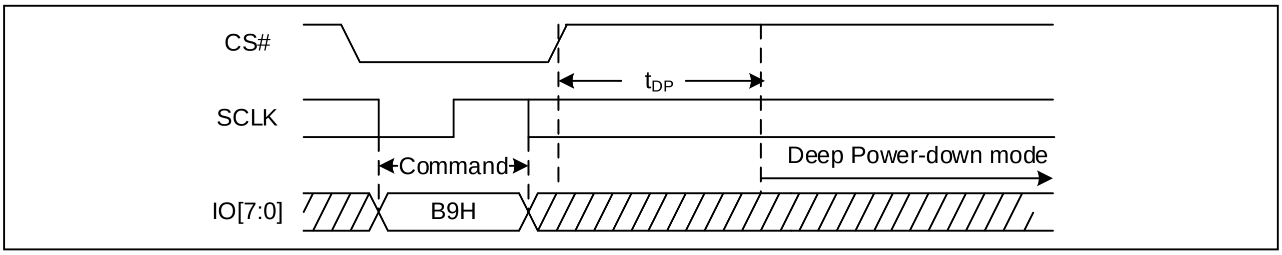


Figure 74. Deep Power-Down Sequence Diagram (OPI)



9.27. Release from Deep Power-Down (ABH)

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used to release the device from the Power-Down state, the command is the same as previously described, After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 75. Release Power-Down Sequence Diagram (SPI)

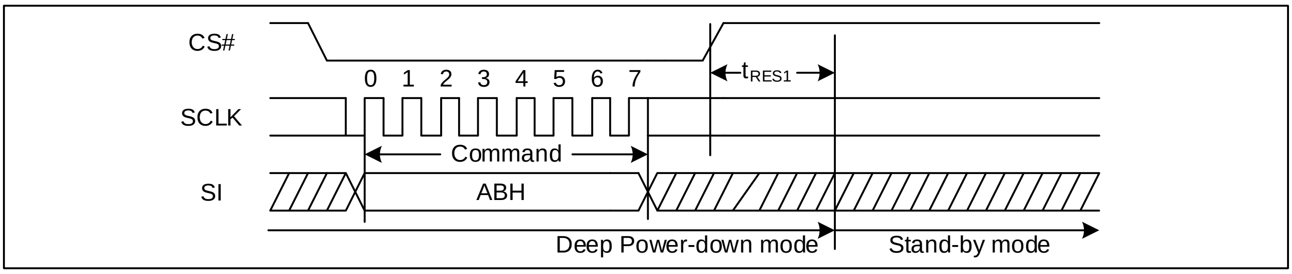
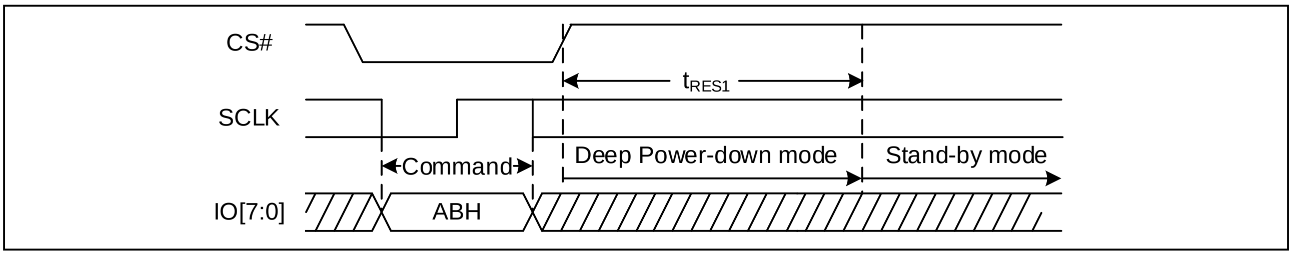


Figure 76. Release Power-Down Sequence Diagram (OPI)

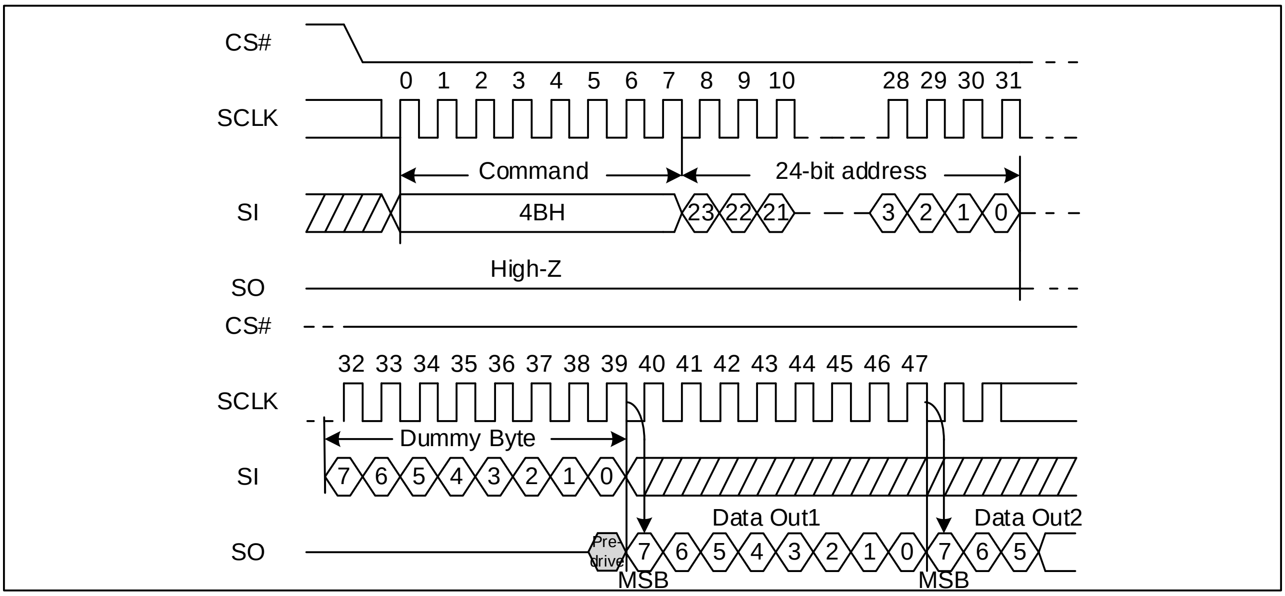


9.28. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

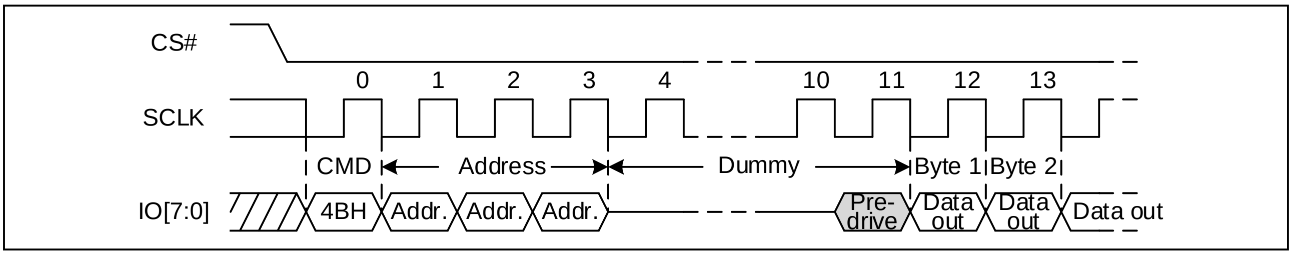
The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-byte address (000000H) or 4-byte address (00000000H) on SI →1 Byte Dummy →128bit Unique ID Out →CS# goes high.

Figure 77. Read Unique ID Sequence Diagram (SPI)



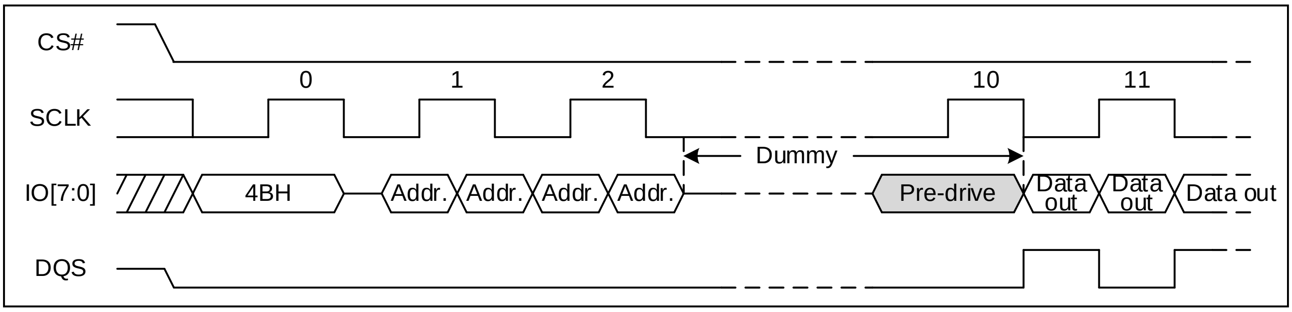
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 78. Read Unique ID Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 79. Read Unique ID Sequence Diagram (DTR OPI)



9.29. Read Identification (RDID) (9FH/9EH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by 3-bytes of device identification. The ID will cycle 4 times. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The command sequence is shown below. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 80. Read Identification ID Sequence Diagram (SPI)

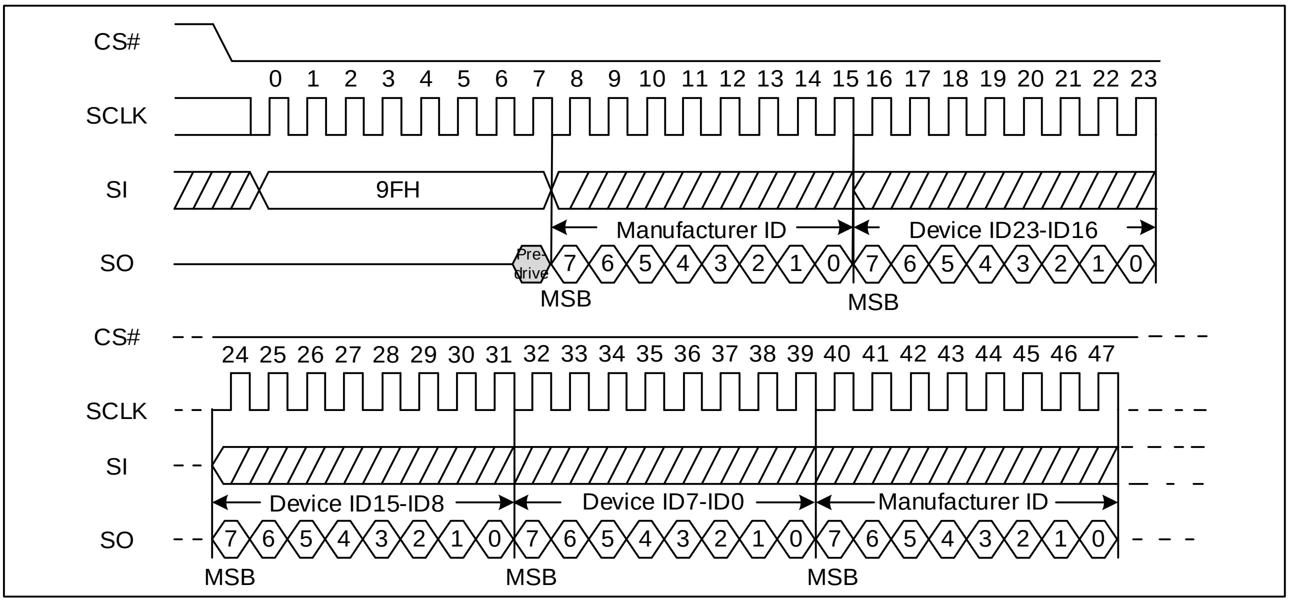


Figure 81. Read Identification ID Sequence Diagram (STR, OPI)

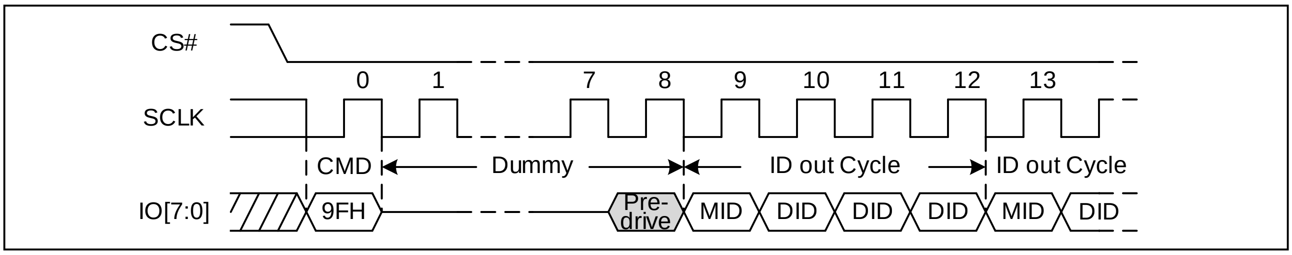
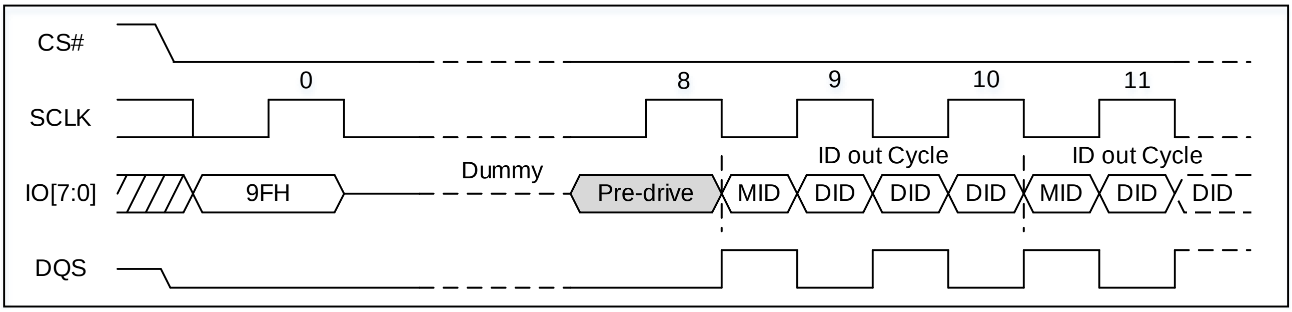


Figure 82. Read Identification ID Sequence Diagram (DTR, OPI)



9.30. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command "75H", allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Register command (01H, B1H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H/21H, 52H/5CH, D8H/DCH, C7H, 60H) and Page Program command (02H/12H, 82H/84H, C2H/8EH) are not allowed during Program suspend. The Write Register command (01H, B1H) and Erase Security Registers command (44H) and Erase commands (20H/21H, 52H/5CH, D8H/DCH, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation. The Program/Erase Suspend command will be accepted by the device only if the SUS_E/SUS_P bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS_E/SUS_P bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS_E/SUS_P bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

Figure 83. Program/Erase Suspend Sequence Diagram (SPI)

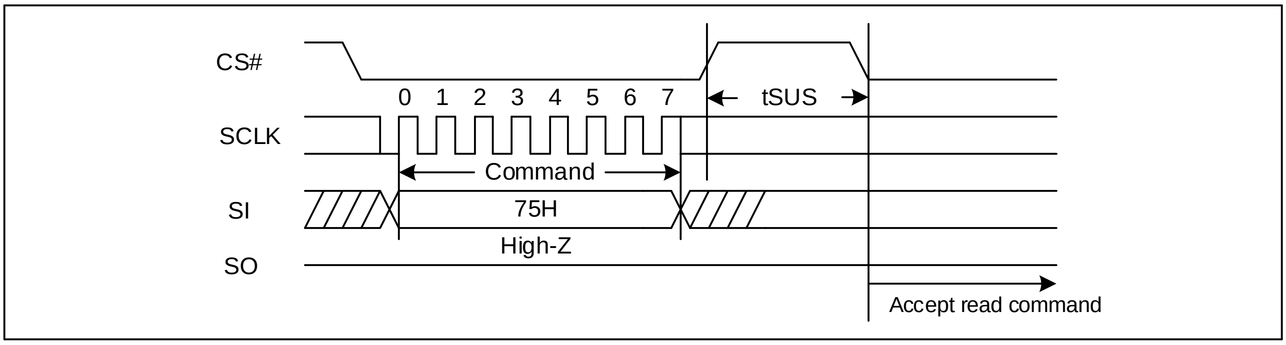
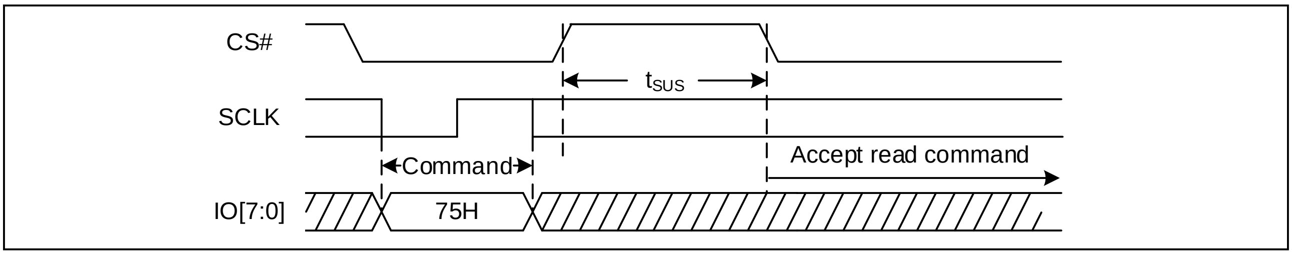


Figure 84. Program/Erase Suspend Sequence Diagram (OPI)



9.31. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS_E/SUS_P bit equal to 1 and the WIP bit equal to 0. After issued the SUS_E/SUS_P bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 85. Program/Erase Resume Sequence Diagram (SPI)

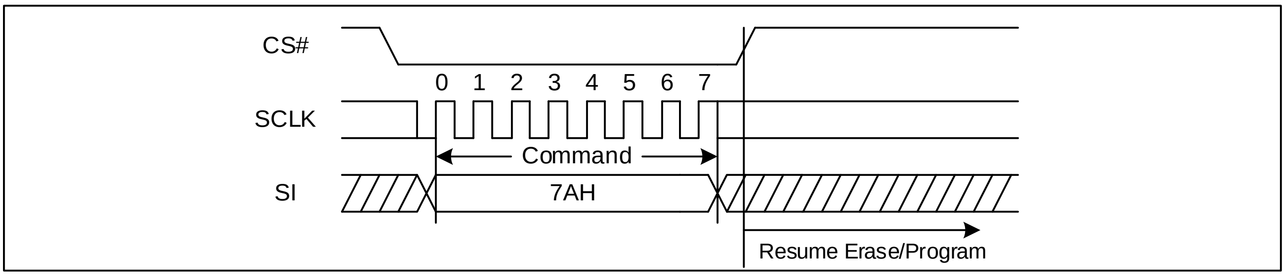
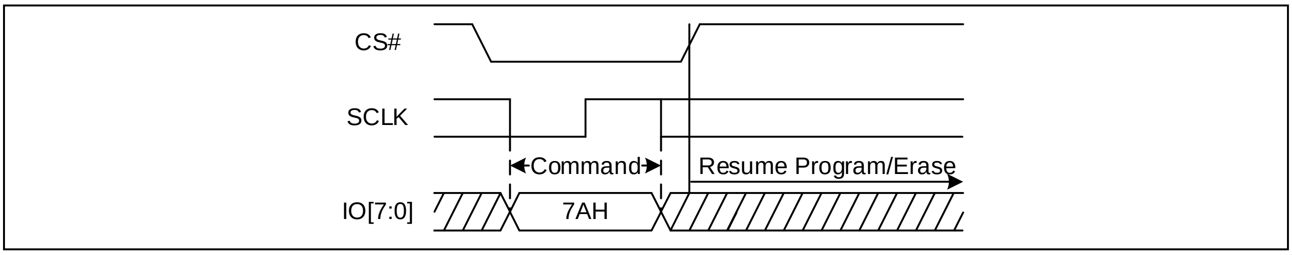


Figure 86. Program/Erase Resume Sequence Diagram (OPI)



9.32. Erase Security Registers (44H)

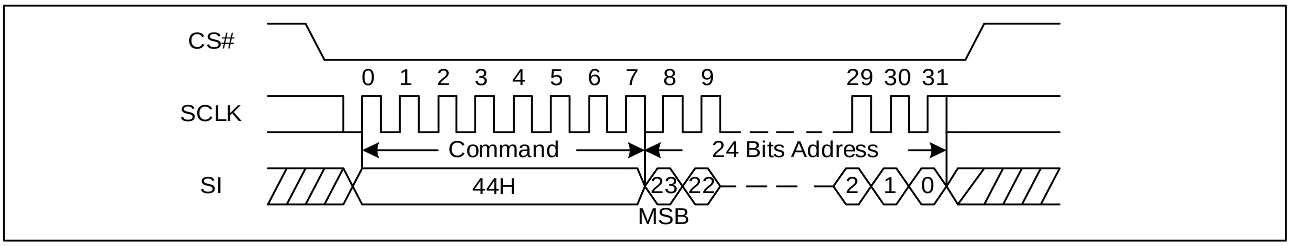
The GD25LX256E provides 4K-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit in the Configuration Register can be used to OTP protect the security registers. Once the bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

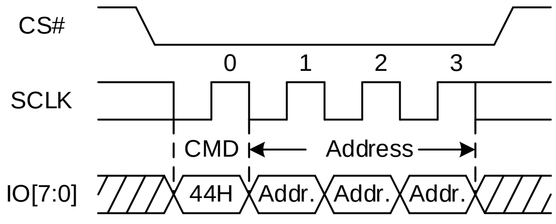
Address	A23-16	A15-12	A11-8	A7-0
Security Register	00H	0 0 0 0	Page Address	Byte Address

Figure 87. Erase Security Registers command Sequence Diagram (SPI)



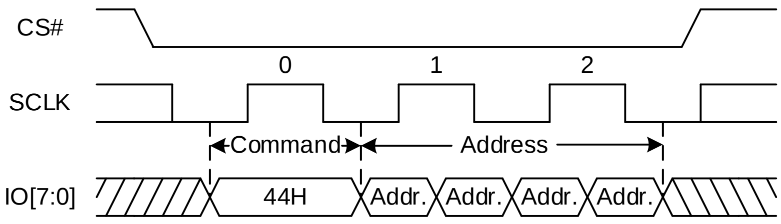
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 88. Erase Security Registers command Sequence Diagram (STR, OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 89. Erase Security Registers command Sequence Diagram (DTR, OPI)



9.33. Program Security Registers (42H)

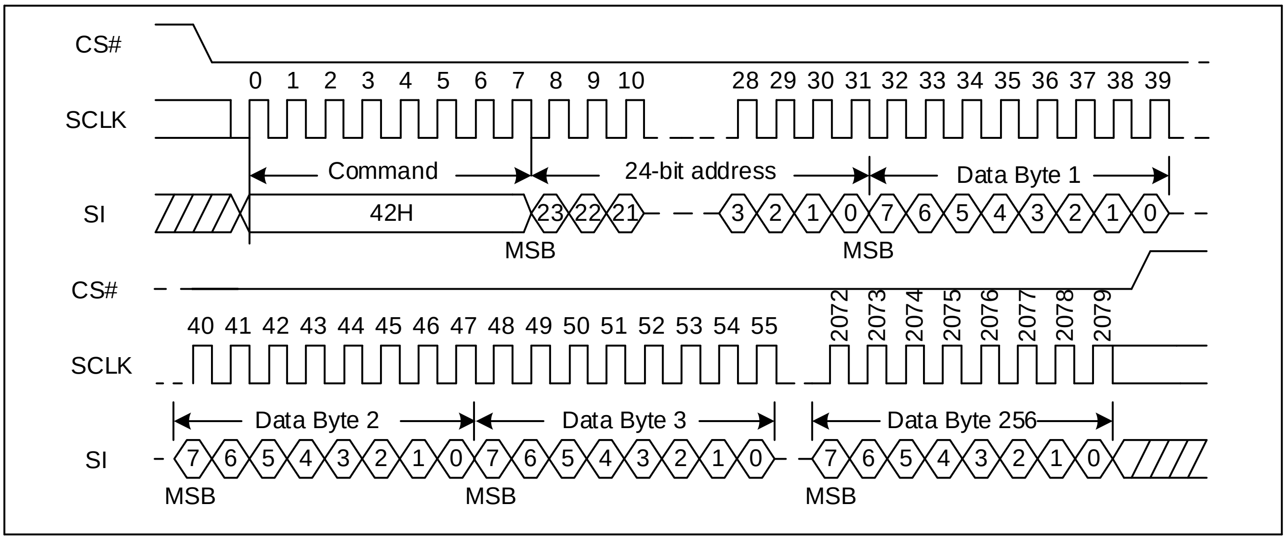
The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

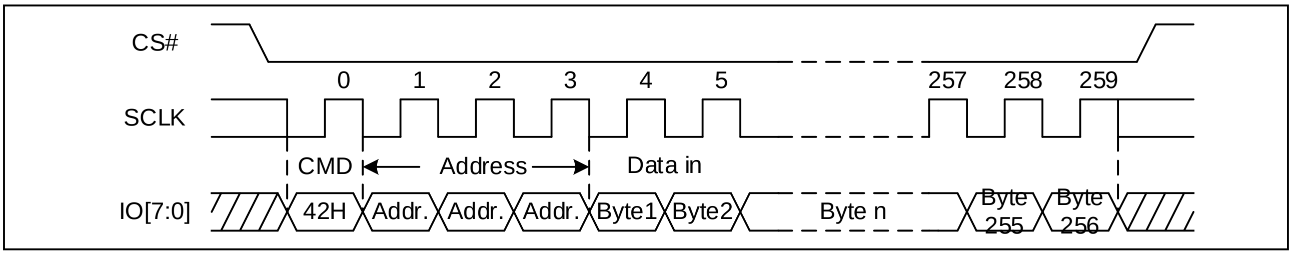
Address	A23-16	A15-12	A11-8	A7-0
Security Register	00H	0 0 0 0	Page Address	Byte Address

Figure 90. Program Security Registers command Sequence Diagram (SPI)



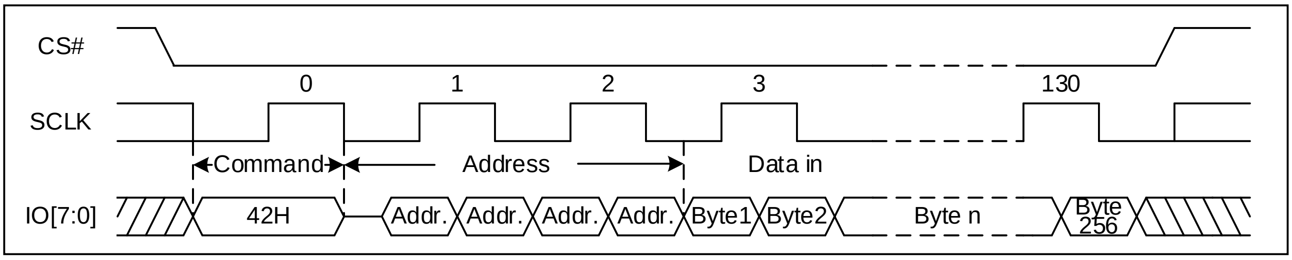
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 91. Program Security Registers command Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 92. Program Security Registers command Sequence Diagram (DTR OPI)



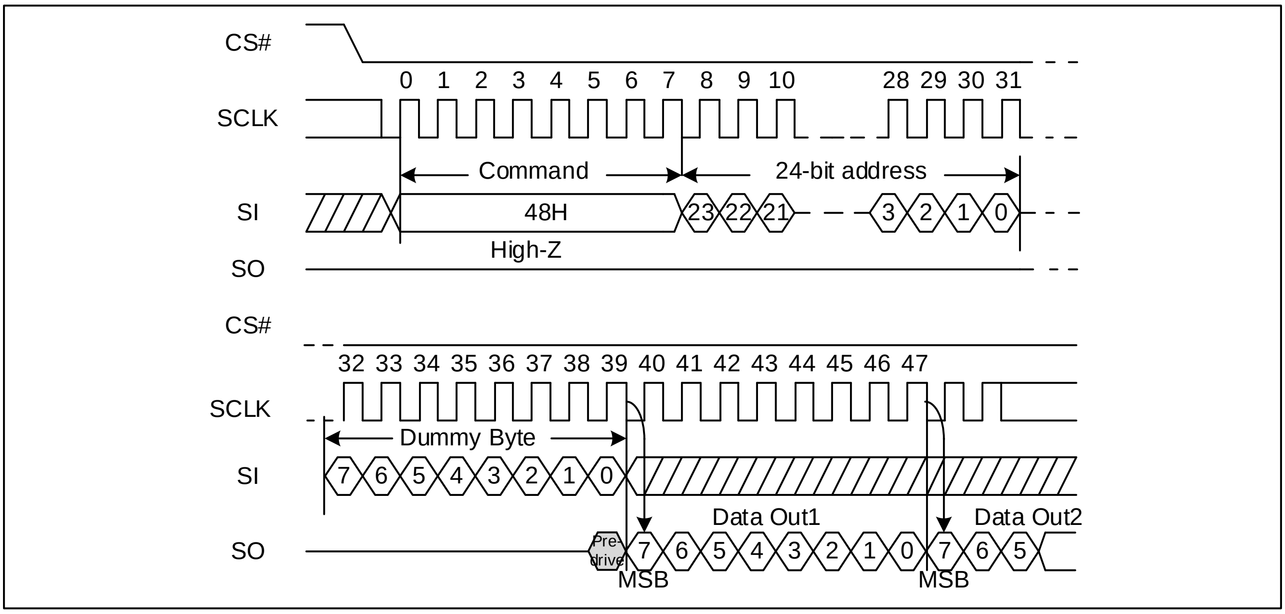
9.34. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A11-A0 address reaches the last byte of the register (Byte FFFH), it will reset to 000H, the command is completed by driving CS# high.

In DTR mode, the starting address given must be even (A0=0) and data byte number must be even.

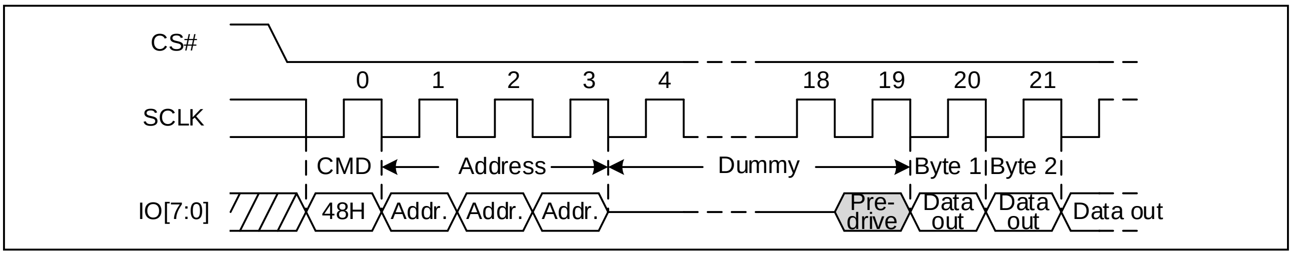
Address	A23-16	A15-12	A11-8	A7-0
Security Register	00H	0 0 0 0	Page Address	Byte Address

Figure 93. Read Security Registers command Sequence Diagram (SPI)



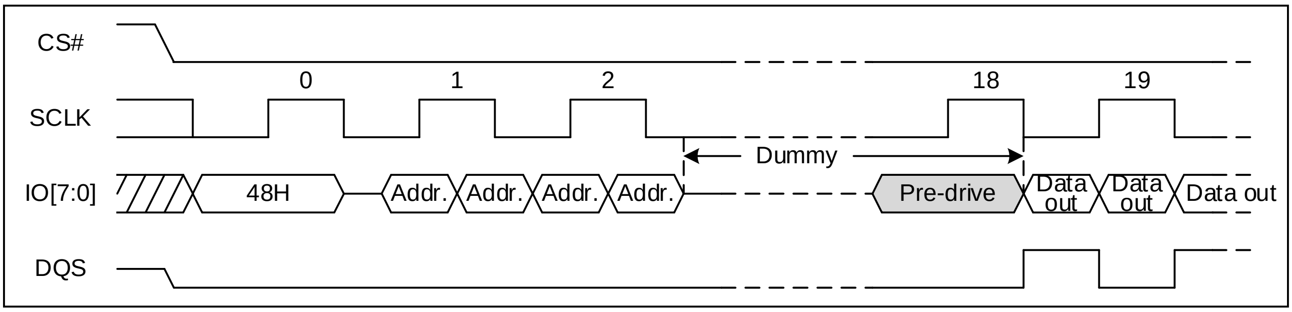
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 94. Read Security Registers command Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 95. Read Security Registers command Sequence Diagram (DTR OPI)



9.35. Individual Block/Sector Lock (36H)/Unlock (39H)/Read (3DH)

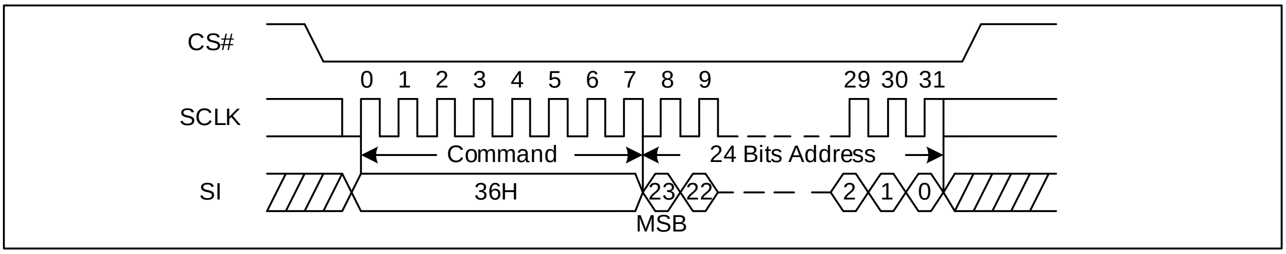
The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Configuration Register bit 2 at address 04h must be set to 0. If WPS=1, the write protection will be determined by the combination of TB, BP (3:0) bits in the Status Register.

The individual Block/Sector Lock command (36H) sequence: CS# goes low →SI: Sending individual Block/Sector Lock command→ SI: Sending 24bits/32bits individual Block/Sector Lock Address → CS# goes high.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low →SI: Sending individual Block/Sector Unlock command→ SI: Sending 24bits/32bits individual Block/Sector Lock Address → CS# goes high.

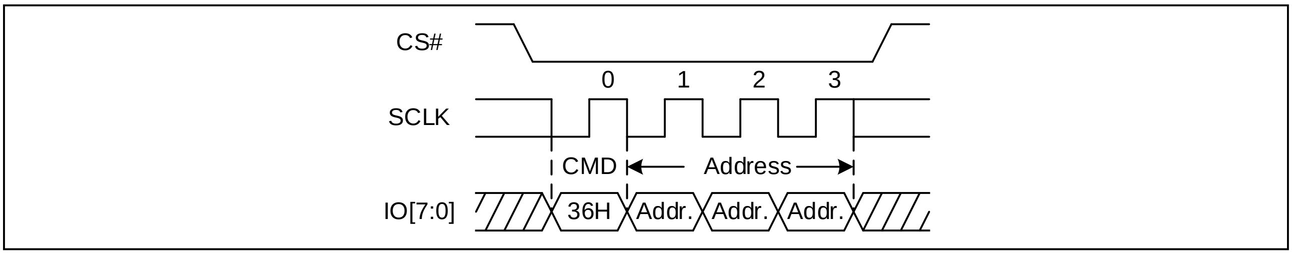
The Read individual Block/Sector lock command (3DH) sequence: CS# goes low → SI: Sending Read individual Block/Sector Lock command→ SI: Sending 24bits/32bits individual Block/Sector Lock Address → SO: The Block/Sector Lock Bit will out →CS# goes high. If the least significant bit (LSB) is1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

Figure 96. Individual Block/Sector Lock command Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 97. Individual Block/Sector Lock command Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 98. Individual Block/Sector Lock command Sequence Diagram (DTR OPI)

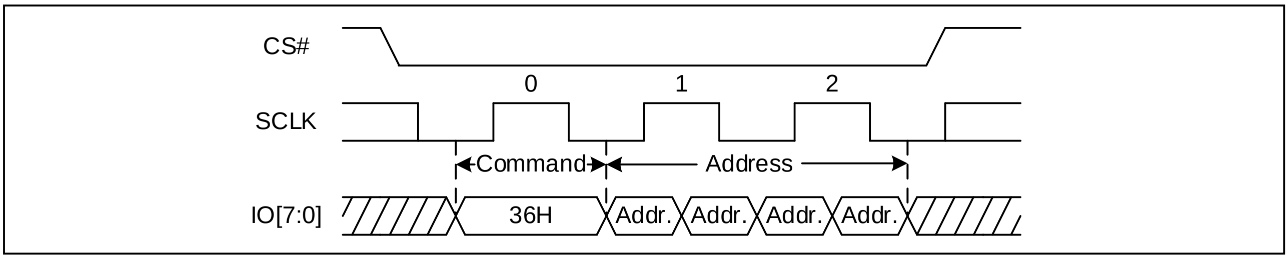
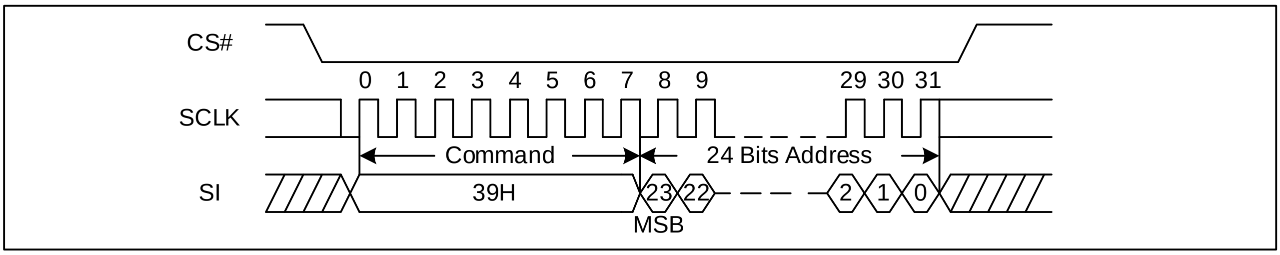
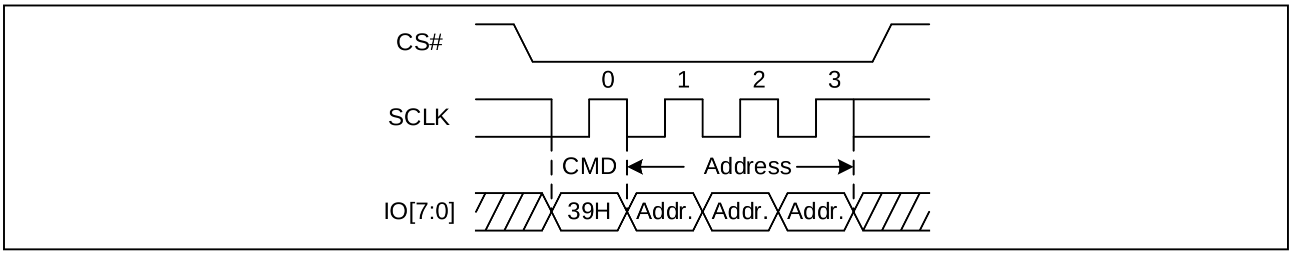


Figure 99. Individual Block/Sector Unlock command Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 100. Individual Block/Sector Unlock command Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 101. Individual Block/Sector Unlock command Sequence Diagram (DTR OPI)

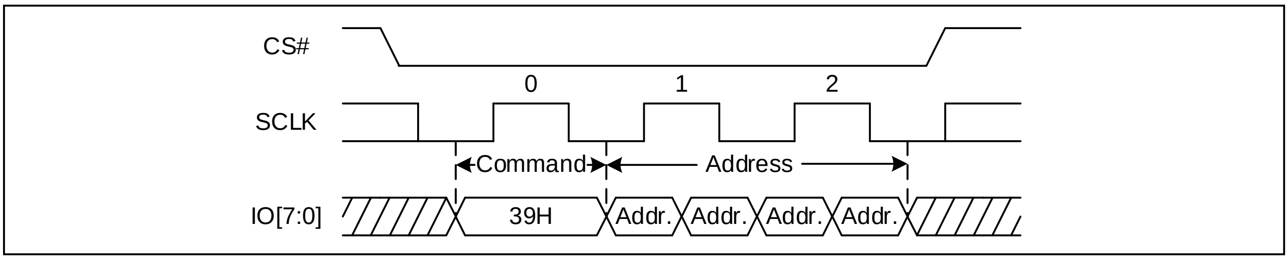
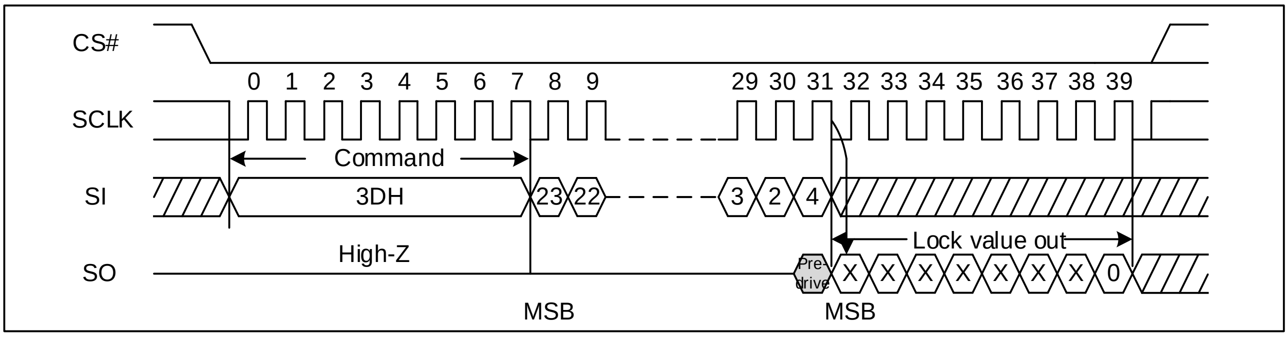
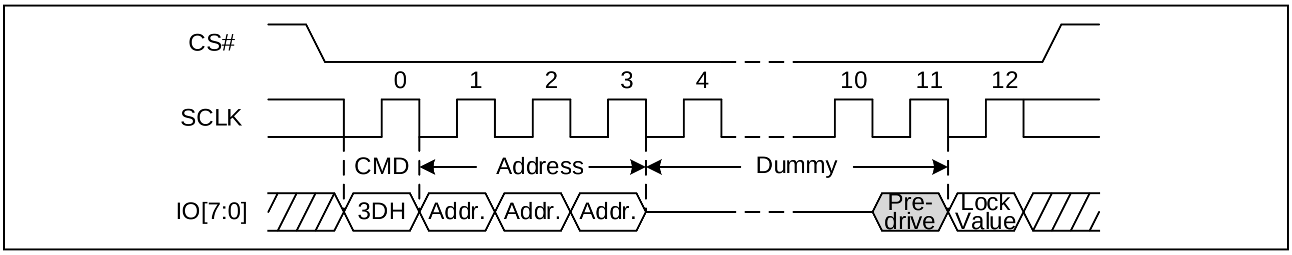


Figure 102. Read Individual Block/Sector lock command Sequence Diagram (SPI)



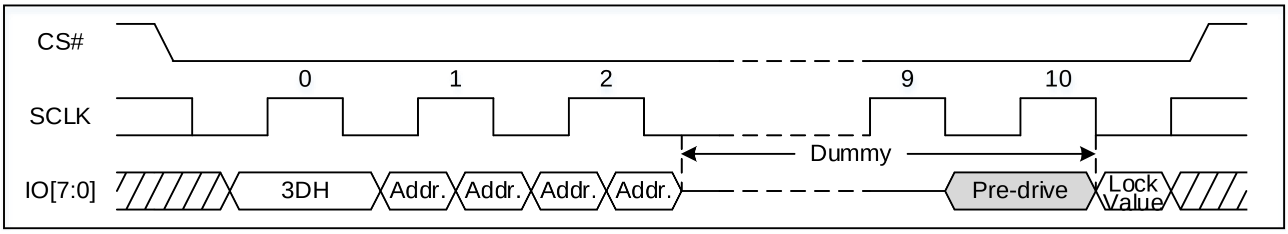
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 103. Read Individual Block/Sector lock command Sequence Diagram (STR OPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 104. Read Individual Block/Sector lock command Sequence Diagram (DTR OPI)



9.36. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low →SI: Sending Global Block/Sector Lock command→ CS# goes high.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low →SI: Sending Global Block/Sector Unlock command→ CS# goes high.

Figure 105. The Global Block/Sector Lock Sequence Diagram (SPI)

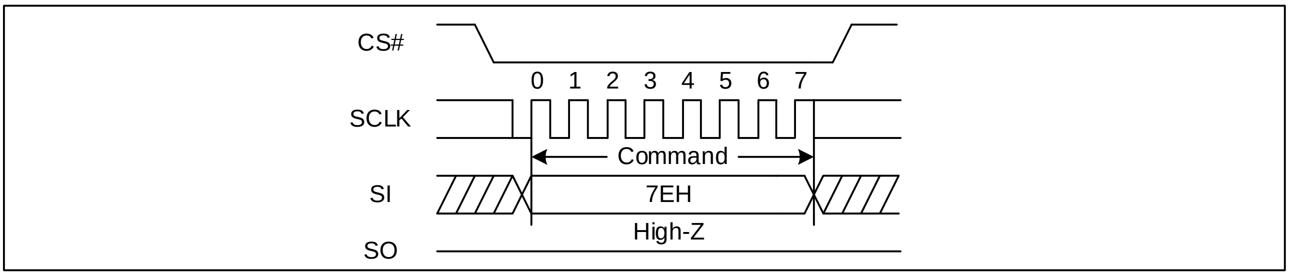


Figure 106. The Global Block/Sector Lock Sequence Diagram (OPI)

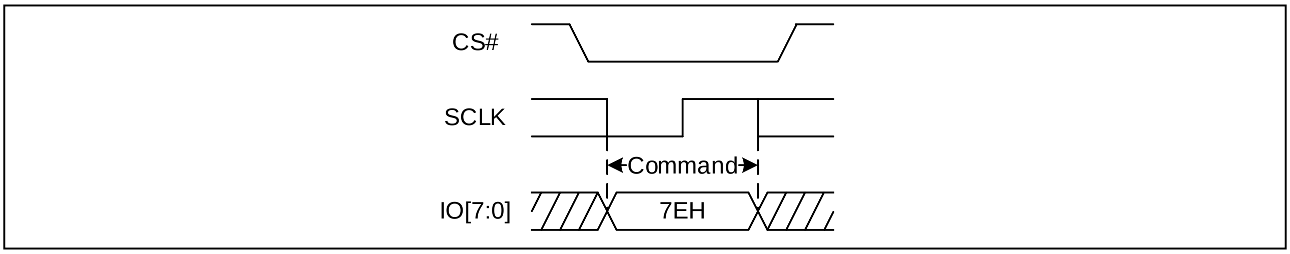


Figure 107. The Global Block/Sector Unlock Sequence Diagram (SPI)

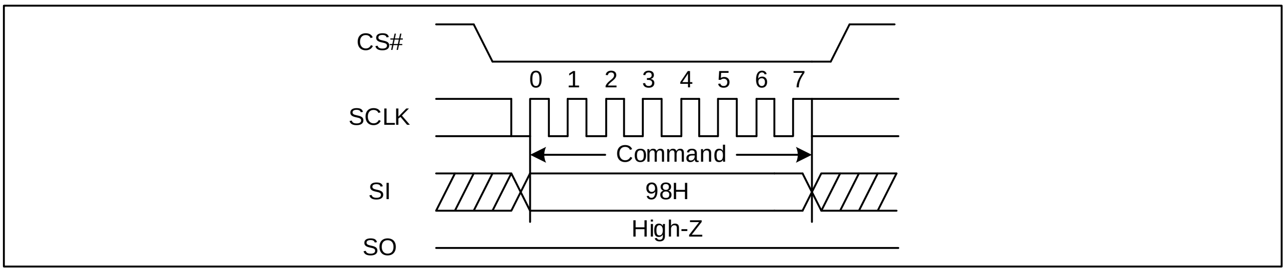
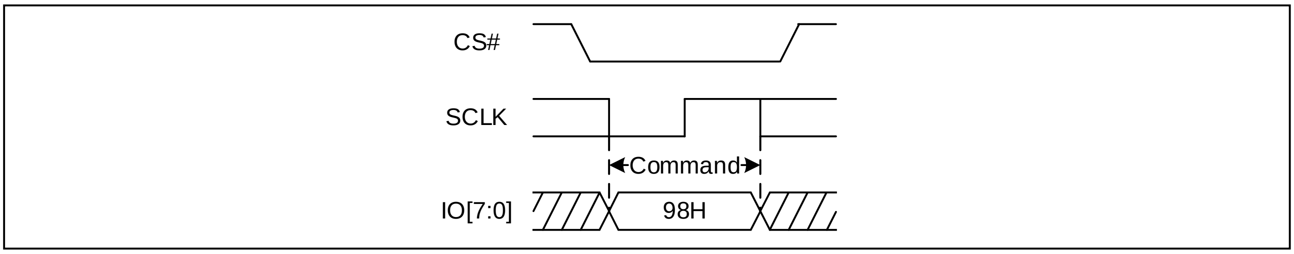


Figure 108. The Global Block/Sector Unlock Sequence Diagram (OPI)



9.37. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) .

When Flash is in OPI Mode, DTR Mode or Continuous Read Mode (XIP), 66H&99H cannot reset Flash to power-on state. Therefore, it is recommended to send the following sequence to reset Flash in these modes:

1. 8CLK with IO<7:0>=all "H" or all "L": ensure Flash quit XIP mode
2. OPI format 66H/99H: ensure Flash in OPI mode and DTR mode can be reset
3. SPI format 66H/99H: ensure Flash in SPI mode can be reset

The "Enable Reset (66H)" and the "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST / tRST_E to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 109. Enable Reset and Reset command Sequence Diagram (SPI)

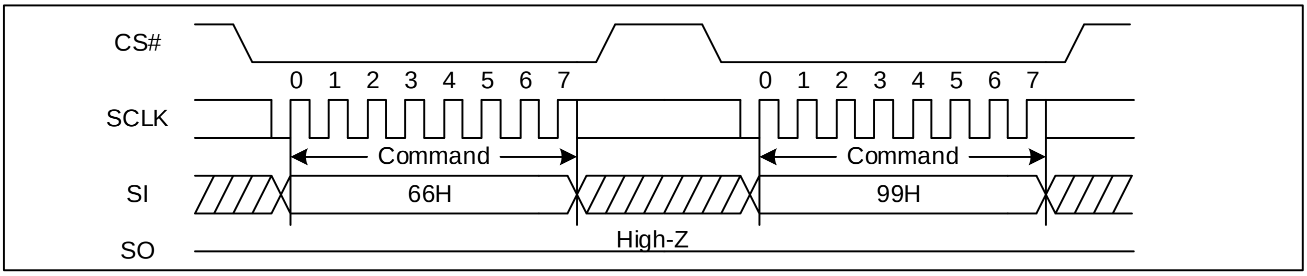
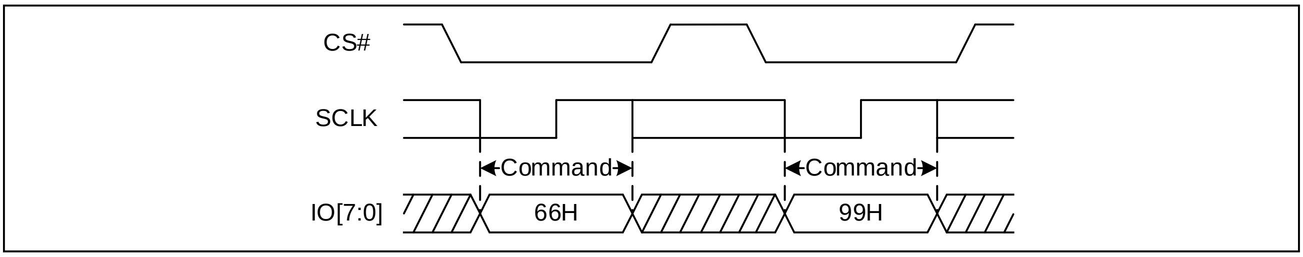


Figure 110. Enable Reset and Reset command Sequence Diagram (OPI)



9.38. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216C.

Figure 111. Read Serial Flash Discoverable Parameter command Sequence Diagram (SPI)

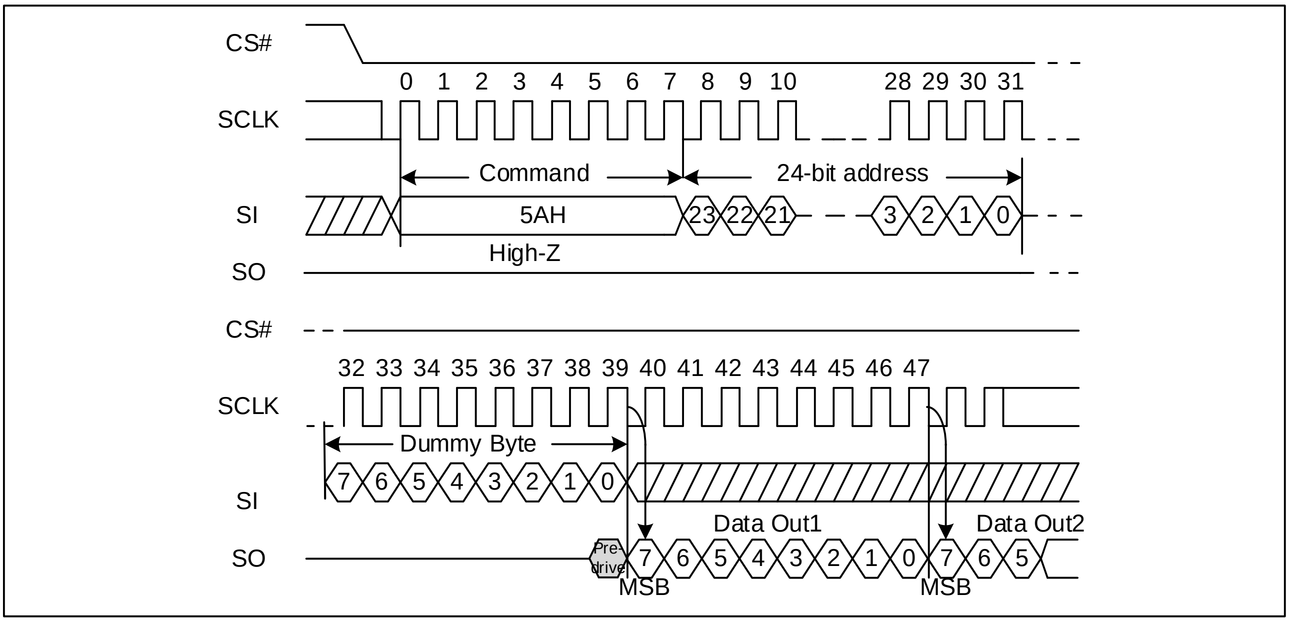


Figure 112. Read Serial Flash Discoverable Parameter command Sequence Diagram (STR OPI)

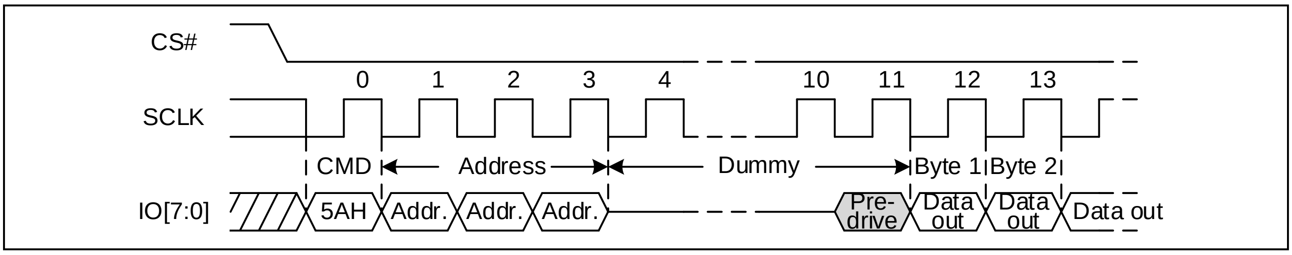


Figure 113. Read Serial Flash Discoverable Parameter command Sequence Diagram (DTR OPI)

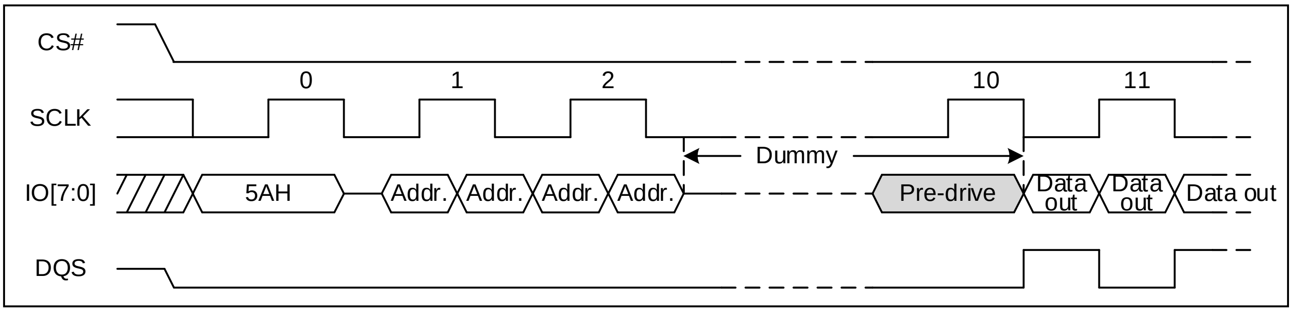


Table 5 Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)

10. ELECTRICAL CHARACTERISTICS

10.1. Power-On Timing

Figure 114. Power-on Timing

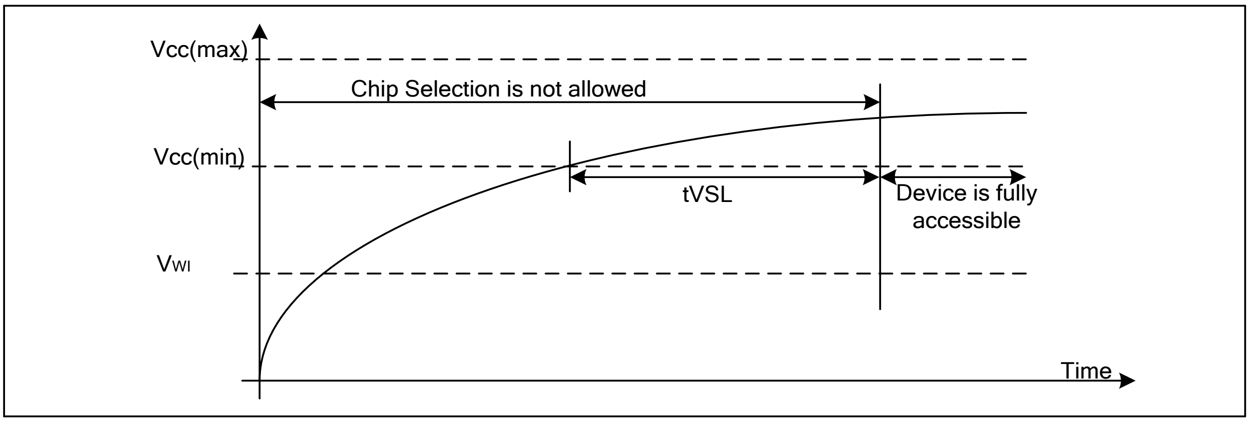


Table 16. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2.5		ms
VWI	Write Inhibit Voltage	1	1.4	V

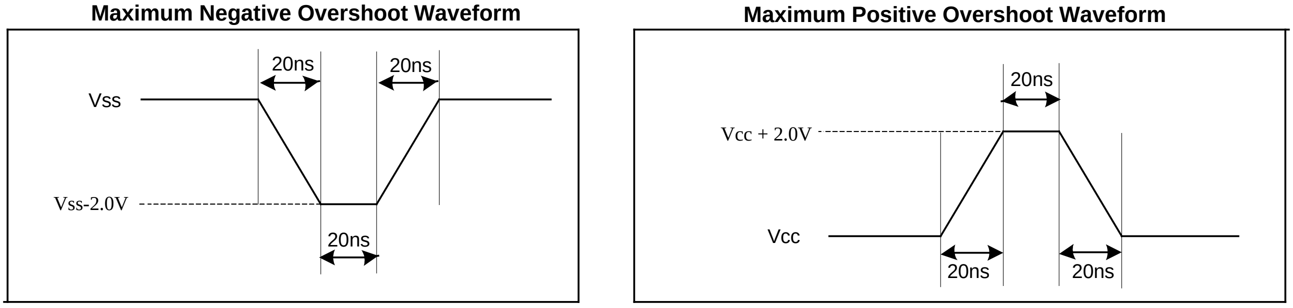
10.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

10.3. Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 2.5	V

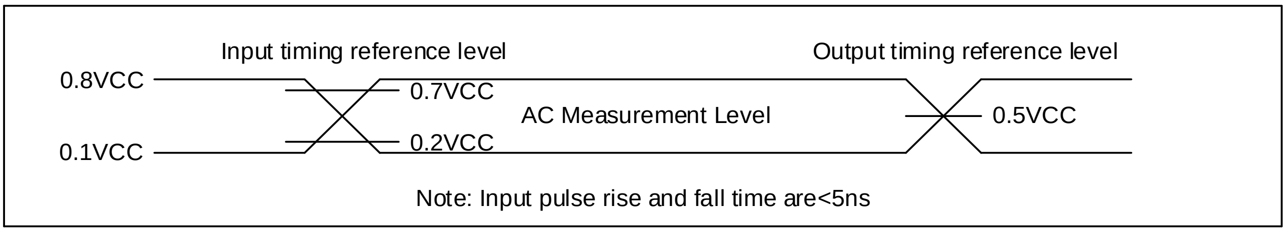
Figure 115. Input Test Waveform and Measurement Level



10.4. Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance	12			pF	
	Input Rise And Fall time			5	ns	
	Input Pause Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 116. Input Test Waveform and Measurement Level



10.5. DC Characteristics

(T= -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		25	150	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		5	50	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 200MHz (DTR), Q=Open(*1,*8 I/O)		50	70	mA
		CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(*1,*8 I/O)		30	50	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		20	40	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC		20	40	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		20	40	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		20	40	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		20	40	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =100uA			0.2	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note:

1. Typical value tested at T = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

10.6. AC Characteristics

(T= -40℃~85℃, VCC=1.65~2.0V, C_L=30pf)

Symbol	Parameter		Min.	Typ.	Max.	Unit
f_{C1}	Serial Clock Frequency for all instructions except Read in STR mode				166	MHz
f_{C2}	Serial Clock Frequency for Fast Read in DTR mode (0BH, 0CH, 8BH, 7CH, CBH, CCH, FDH in DTR mode)				200	MHz
f_R	Serial Clock Frequency For: Read (03H, 13H)				60	MHz
t_{CLH}	Serial Clock High Time		45% (1/fc)			ns
t_{CLL}	Serial Clock Low Time		45% (1/fc)			ns
t_{CLCH} t_{CHCL}	Serial Clock Rise Time (Slew Rate)/Serial Clock Fall Time (Slew Rate)	fSCLK≤ 100MHz	0.6			V/ns
		fSCLK≤ 133MHz	0.8			V/ns
		fSCLK≤ 166MHz	1			V/ns
		fSCLK≥ 166MHz	1.2			V/ns
t_{SLCH}	CS# Active Setup Time		4			ns
t_{CHSH}	CS# Active Hold Time		3			ns
t_{CLSH}	CS# Active Hold Time (DTR)		3			ns
t_{SHCH}	CS# Not Active Setup Time		3			ns
t_{CHSL}	CS# Not Active Hold Time		5			ns
t_{SHSL}	CS# High Time (Read/Write)	From Read to next Read	20			ns
		From Write/Erase/Program to Read Statue Register	40			ns
t_{CLQX} t_{CHQX}	Output Hold Time		1			ns
t_{DVCH}	Data In Setup Time (STR)	fSCLK ≤ 133MHz	2			ns
		fSCLK ＞133MHz	1			ns
t_{DVCH} t_{DVCL}	Data In Setup Time (DTR)	fSCLK ≤ 100MHz	1			ns
		fSCLK ≤ 133MHz	0.8			ns
		fSCLK ≤ 166MHz	0.6			ns
		fSCLK ＞166MHz	0.5			ns
t_{CHDX}	Data In Hold Time (STR)	fSCLK ≤ 133MHz	2			ns
		fSCLK ＞133MHz	1			ns
t_{CHDX} t_{CLDX}	Data In Hold Time (DTR)	fSCLK ≤ 100MHz	1			ns
		fSCLK ≤ 133MHz	0.8			ns
		fSCLK ≤ 166MHz	0.6			ns
		fSCLK ＞166MHz	0.5			ns
t_{SHQZ}	Output Disable Time				8	ns
t_{QSV}	Clock transient to DQS valid time			Align to 30pF tCLQV		ns
t_{DQSQ}	SIO valid skew related to DQS (12pF)				0.4	ns
t_{QHS}	SIO hold skew factor (12pF)				0.4	ns

t_{CLQV}	Clock Transient To Output Valid (30pF)			8	ns
t_{CHQV}	Clock Transient To Output Valid (12pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode			30	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RST}	CS# High To Next Command After Reset (except from erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (from erase)			30	ms
t_W	Write Status Register Cycle Time Write Non-Volatile Configuration Register Cycle Time		4	40	ms
t_{BP1}	Byte Program Time (First Byte)		30	50	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	5	μs
t_{PP}	Page Programming Time		0.4	1.2	ms
t_{SE}	Sector Erase Time		30	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.1	0.8	s
t_{BE2}	Block Erase Time (64K Bytes)		0.2	2	s
t_{CE}	Chip Erase Time (GD25LX256E)		50	200	s

Note:

1. Typical value tested at T = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Time of CS# High To Next Command After Reset from 01H/B1H command would be tW + tRST

Figure 117. Serial Input Timing

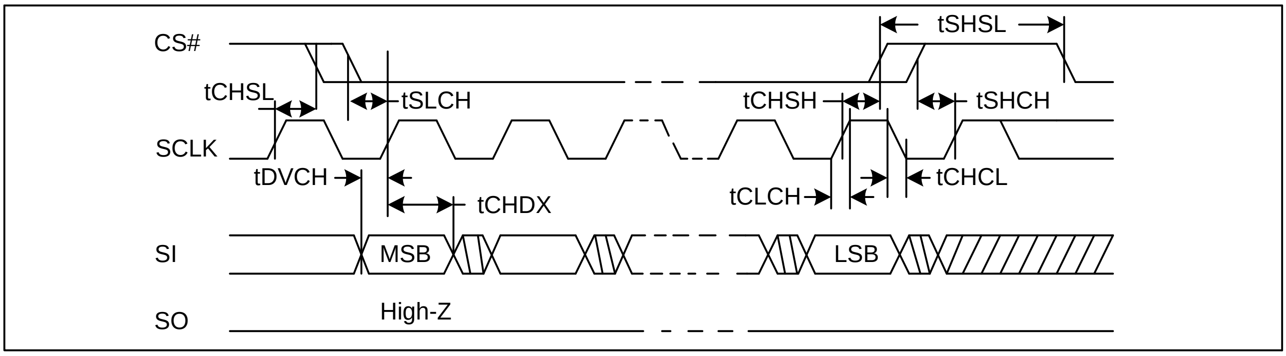


Figure 118. Output Timing

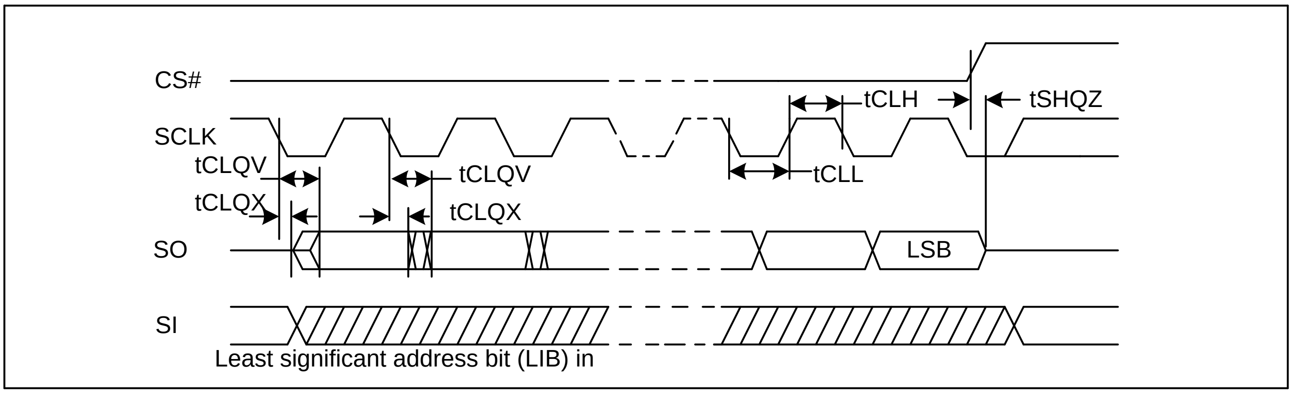


Figure 119. Serial Input Timing (DTR)

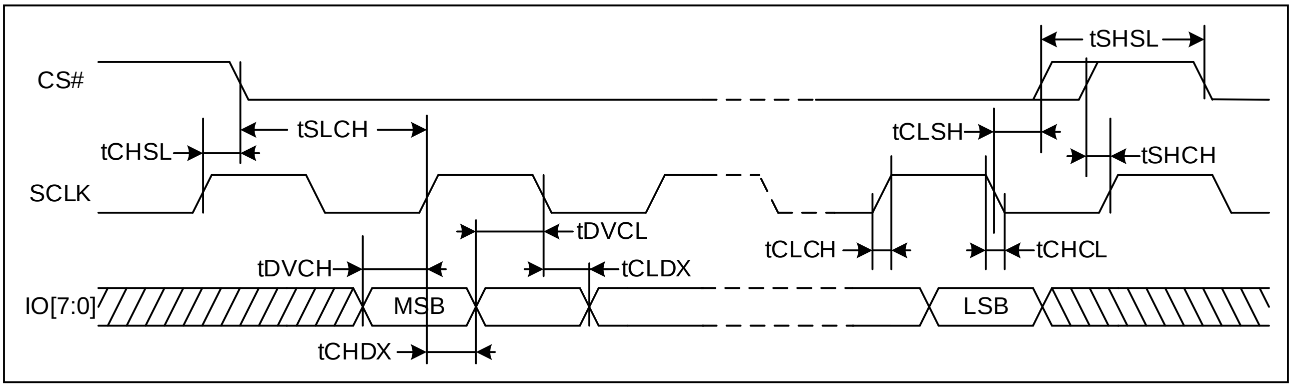


Figure 120. Serial Output Timing (DTR)

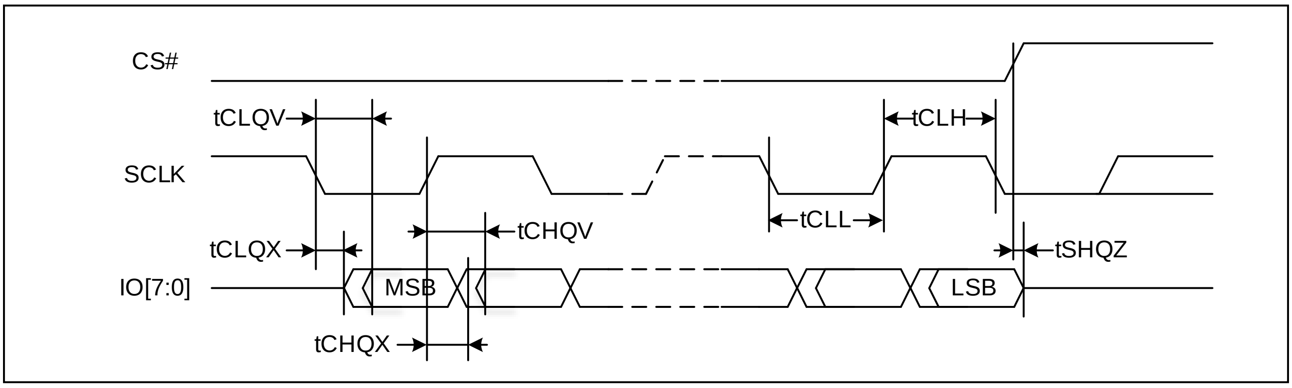


Figure 121. DQS Output Timing (DTR)

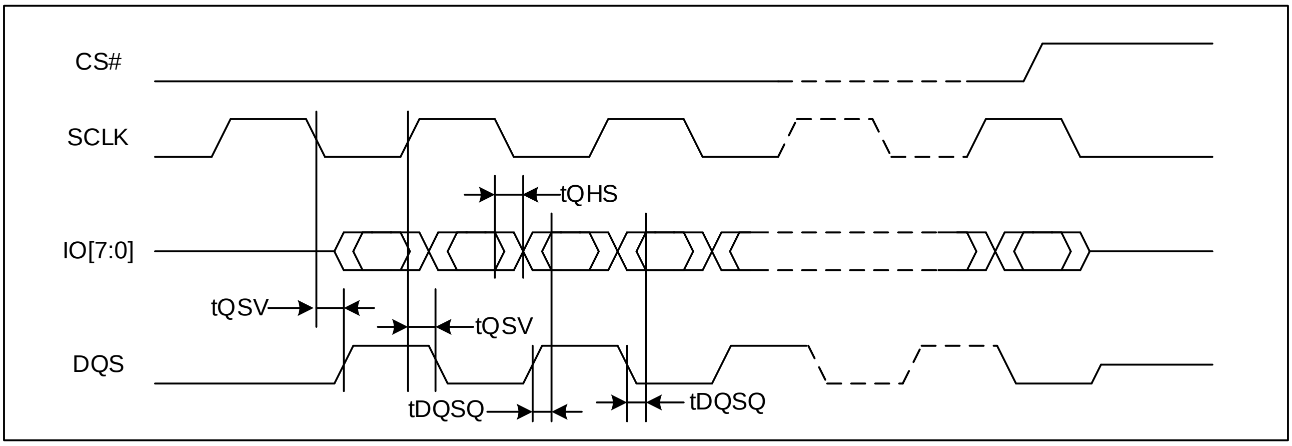


Figure 122. RESET Timing

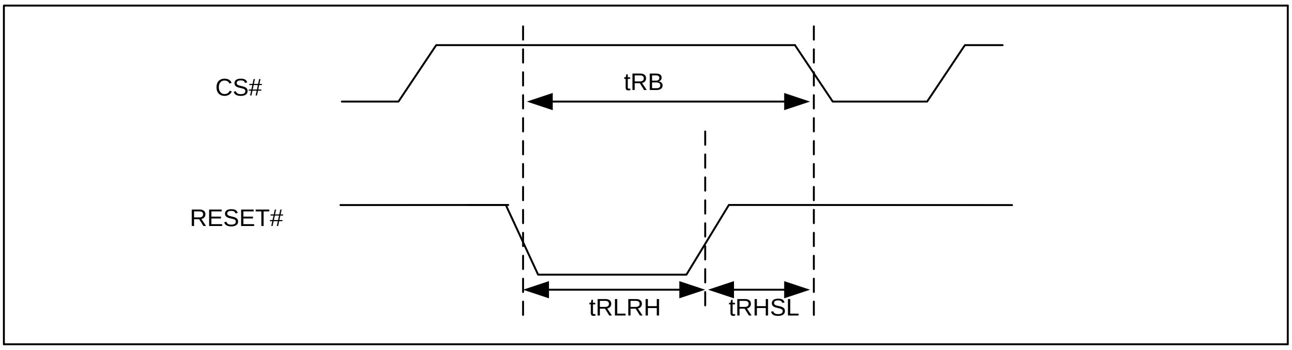


Table 17. Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
t_{RLRH}	Reset Pulse Width	1			μs
t_{RHSL}	Reset High Time Before Read	50			ns
t_{RB}	Reset Recovery Time (From Read or Program)			30	μs
	Reset Recovery Time (From Erase)			30	ms

Note:

1. Time of Reset Recovery Time from 01H/B1H command would be tW + tRB

11. ORDERING INFORMATION

GD XX XX XX X X X X X

Packing
T or no mark: Tube
Y: Tray
R: Tape and Reel

Green Code
G: Pb Free + Halogen Free Green Package
R: Pb Free + Halogen Free Green Package + RESET# Pin

Temperature Range
I: Industrial (-40℃ to +85℃)
J: Industrial (-40℃ to +105℃)*
E: Industrial (-40℃ to +125℃)*
F: Industrial+ (-40℃ to +85℃)
3: Automotive (-40℃ to +85℃)*
2: Automotive (-40℃ to +105℃)*
A: Automotive (-40℃ to +125℃)*

Package Type
F: SOP16 300mil
B: TFBGA-24ball (5x5 Ball Array)
4: WLCSP

Generation
E: E Version

Density
256: 256M bit

Series
LX: 1.8V, 4KB Uniform Sector

Product Family
25: SPI NOR Flash

***This datasheet applies to temperature range I: Industrial (-40℃ to +85℃) and F: Industrial+ (-40℃ to +85℃) only. Please contact GigaDevice sales for extended temperature industrial products and automotive products.**

11.1. Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

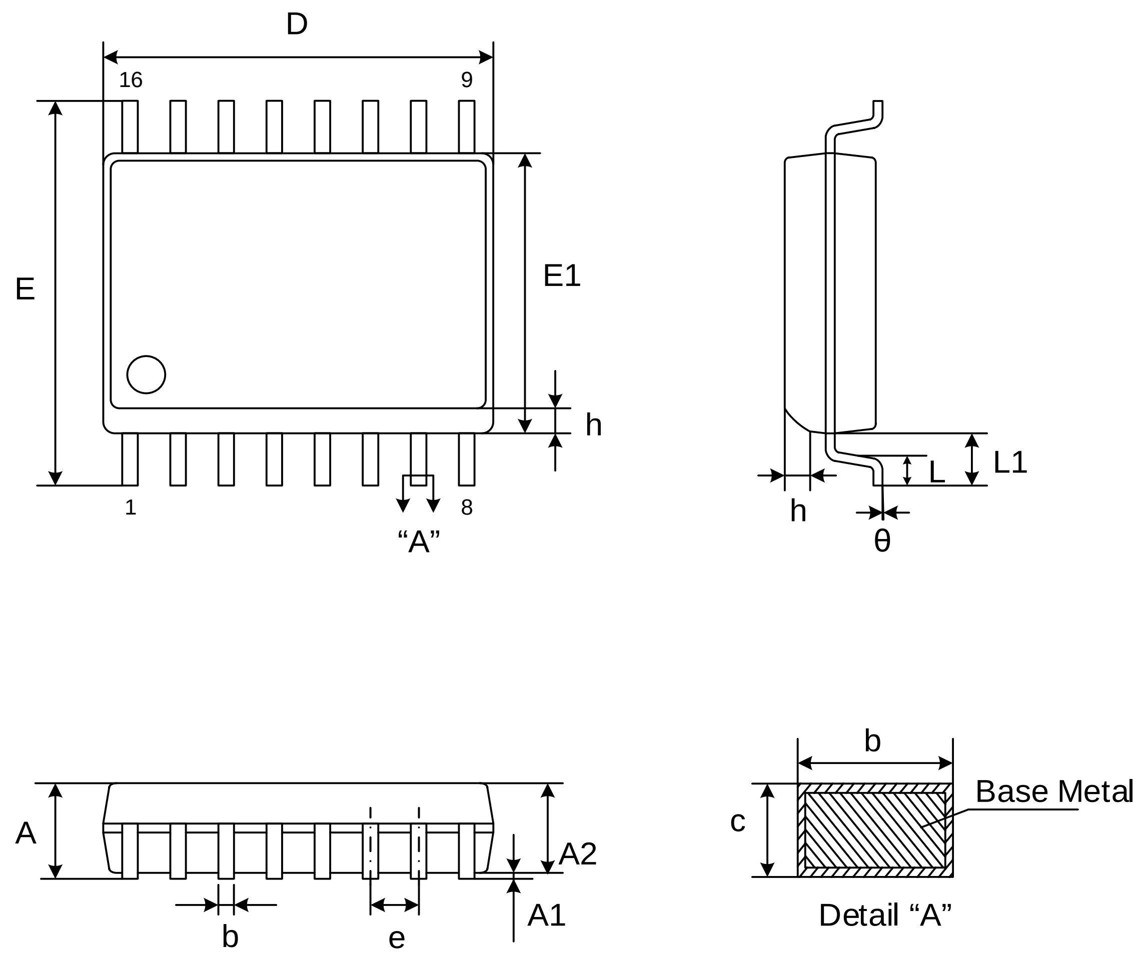
Product Number	Density	Package Type
GD25LX256EFIR	256Mbit	SOP16 300mil
GD25LX256EBIR	256Mbit	TFBGA-24ball (5x5 Ball Array)
GD25LX256E4IRR	256Mbit	WLCSP

Temperature Range F: Industrial+ (-40℃ to +85℃)

Product Number	Density	Package Type
GD25LX256EFFR	256Mbit	SOP16 300mil
GD25LX256EBFR	256Mbit	TFBGA-24ball (5x5 Ball Array)
GD25LX256E4FRR	256Mbit	WLCSP

12. PACKAGE INFORMATION

12.1. Package SOP16 300MIL



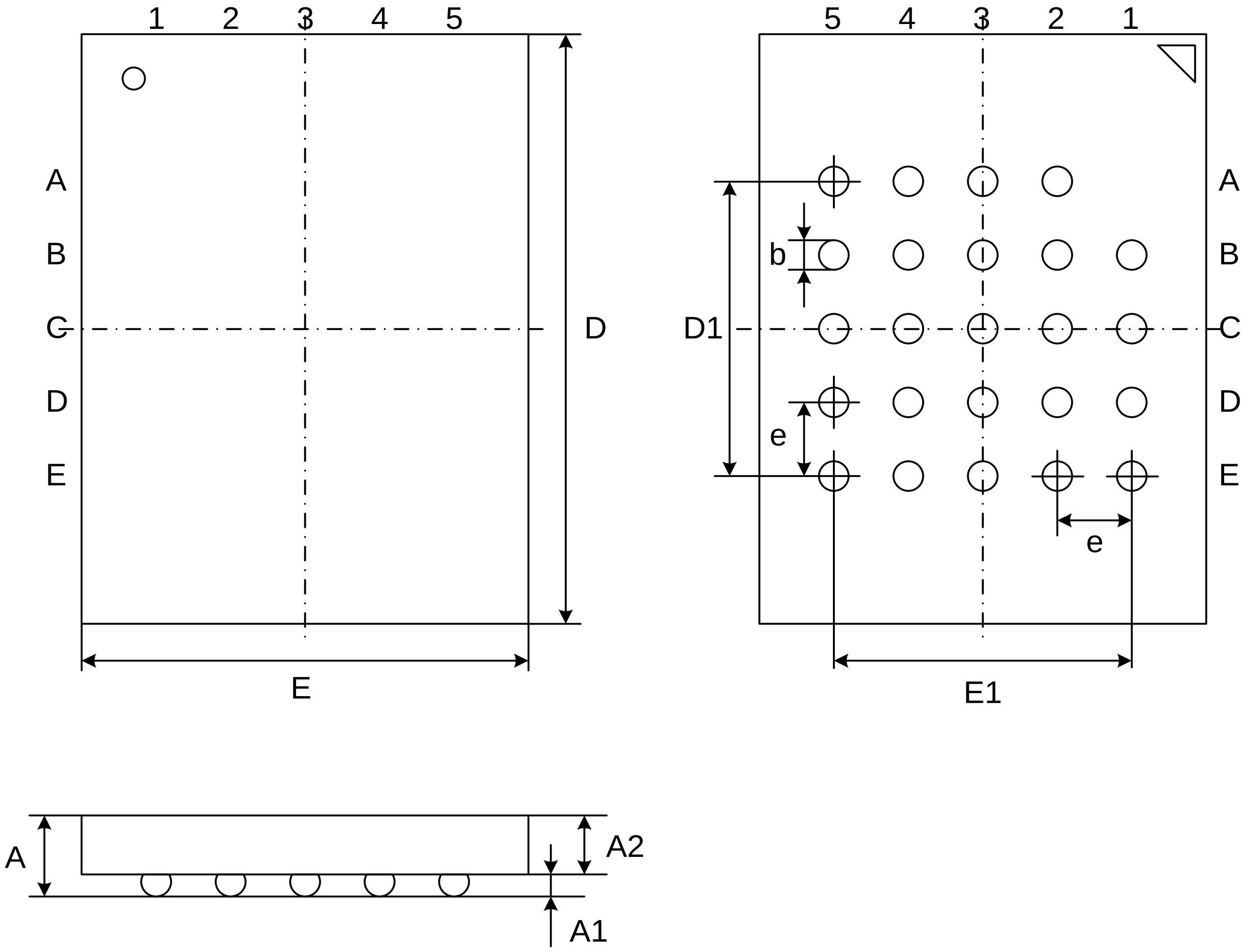
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	-
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8

Note:

1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

12.2. Package TFBGA-24BALL (5x5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.25	0.75	0.35	5.90		7.90		
	Nom	-	0.30	0.80	0.40	6.00	4.00	8.00	4.00	1.00
	Max	1.20	0.35	0.85	0.45	6.10		8.10		

Note: Both the package length and width do not include the mold flash.

12.3. Package WLCSP

(TBD)

13. REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2019-8-5

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