

GigaDevice Semiconductor Inc.

GD32A503xx

Arm[®] Cortex[®]-M33 32-bit MCU

Datasheet

Revision 1.0

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1. General description

The GD32A503xx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32A503xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 100 MHz frequency with Flash accesses 0~3 waiting time to obtain maximum efficiency. It provides up to 384 KB on-chip Flash memory and up to 48 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer two 12-bit ADCs, one DAC, one comparator, up to one general 16-bit timer, two basic timers, four PWM advanced timers, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, three USARTs, one I2S, and two CANs. Additional peripherals as trigger selection controller (TRIGSEL), multi-function communication interface (MFCOM), DMA request multiplexer (DMAMUX) are included.

The device operates from a 2.7 to 5.5 V power supply and available in -40 to +125 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32A503xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.



2. Device overview

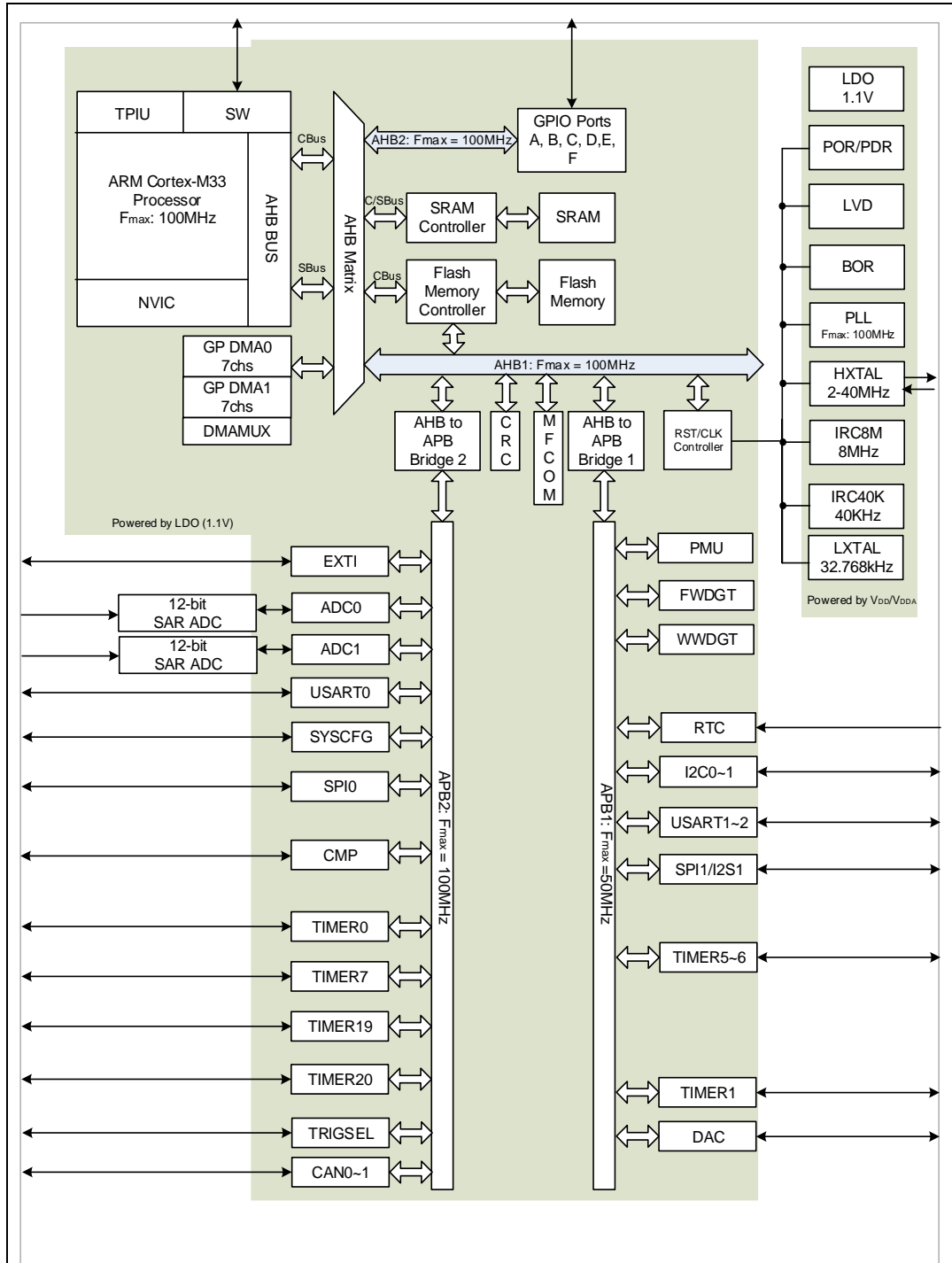
2.1. Device information

Table 2-1. GD32A503xx devices features and peripheral list

| Part Number | GD32A503xx | | | | | | | | | |
|---------------------------------|------------------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| | KB | KC | CB | CC | RB | RC | RD | VB | VC | VD |
| FLASH (KB) | 128 | 256 | 128 | 256 | 128 | 256 | 384 | 128 | 256 | 384 |
| SRAM (KB) | 24 | 32 | 24 | 32 | 24 | 32 | 48 | 24 | 32 | 48 |
| Data Flash & EEPROM backup (KB) | 32 | 64 | 32 | 64 | 32 | 64 | 64 | 32 | 64 | 64 |
| EEPROM (KB) | 2 | 4 | 2 | 4 | 2 | 4 | 4 | 2 | 4 | 4 |
| Timers | General timer(16-bit) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) | 1 (1) |
| | Advanced timer(16-bit) | 3 (0,7,19) | 4 (0,7,19,20) | 3 (0,7,19) | 4 (0,7,19,20) | 3 (0,7,19) | 4 (0,7,19,20) | 4 (0,7,19,20) | 4 (0,7,19,20) | 4 (0,7,19,20) |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer(16-bit) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) | 2 (5-6) |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 1 (0) | 1 (0) | 2 (0-1) | 2 (0-1) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) | 3 (0-2) |
| | I2C | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) | 2 (0-1) |
| | SPI/I2S | 1/0 (0)/none | 1/0 (0)/none | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) | 2/1 (0-1)/(1) |
| | MFCOM | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | CAN | 1xFD (0) | 1xFD (0) | 2xFD (0-1) | 2xFD (0-1) | 2xFD (0-1) | 2xFD (0-1) | 2xFD (0-1) | 2xFD (0-1) | 2xFD (0-1) |
| GPIO | 27 | 27 | 42 | 42 | 57 | 57 | 57 | 88 | 88 | 88 |
| DAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| CMP | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ADC | Units | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Channels | 12 | 12 | 20 | 20 | 27 | 27 | 27 | 32 | 32 |
| Package | QFN32 | | LQFP48 | | LQFP64 | | | LQFP100 | | |

2.2. Block diagram

Figure 2-1. GD32A503xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32A503Vx LQFP100 pinouts

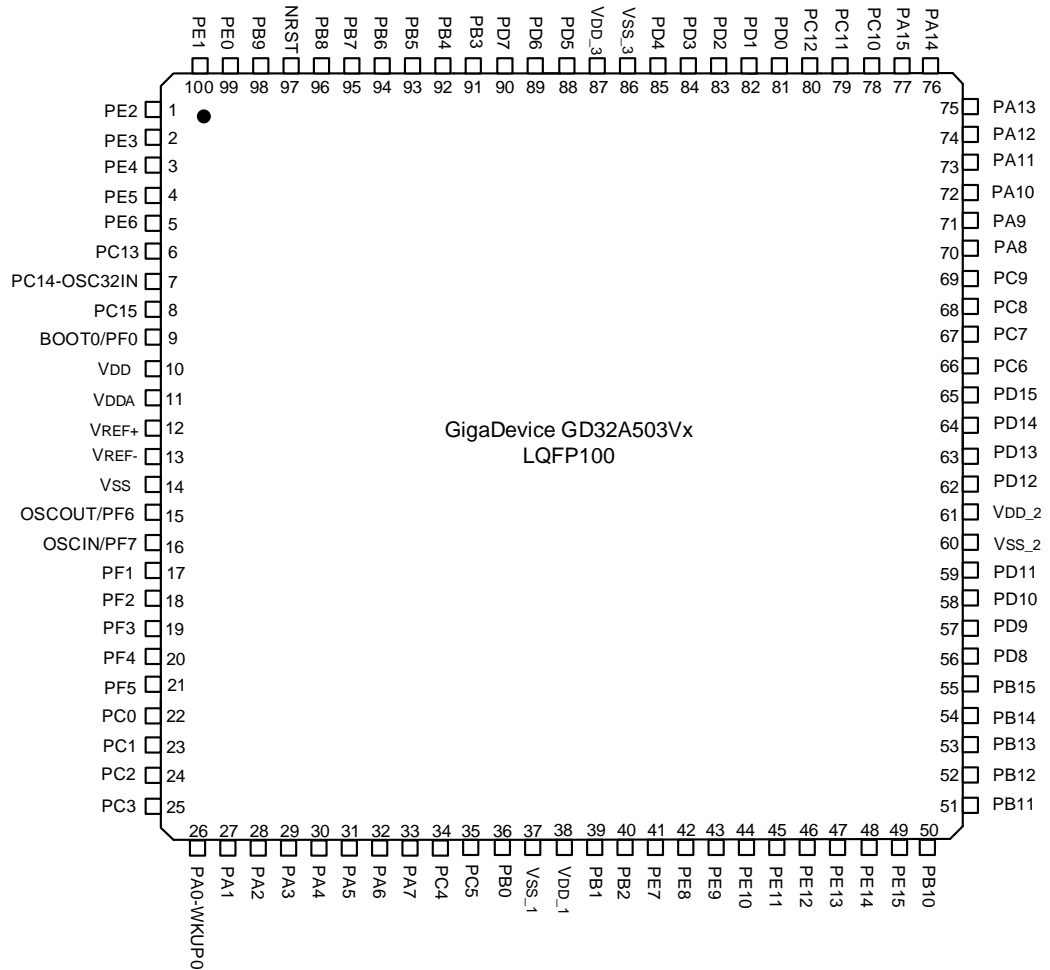


Figure 2-3. GD32A503Rx LQFP64 pinouts

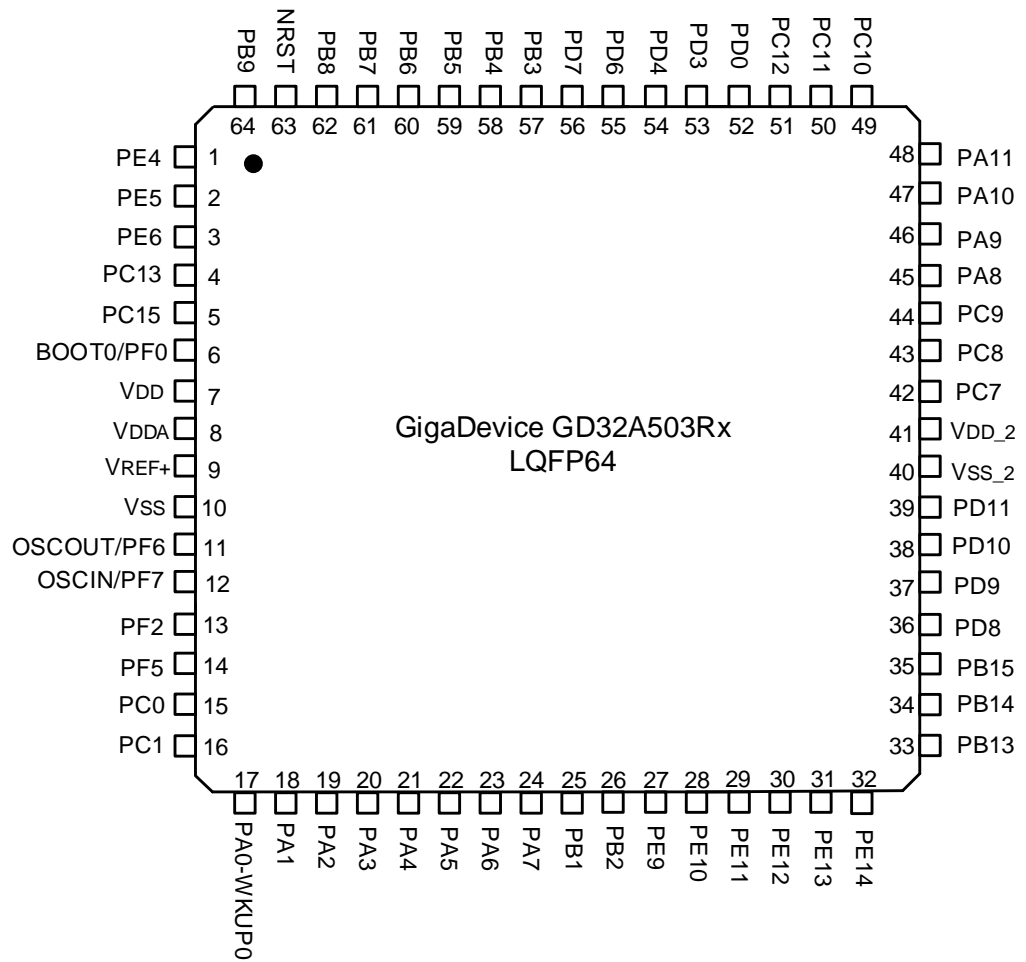


Figure 2-4. GD32A503Cx LQFP48 pinouts

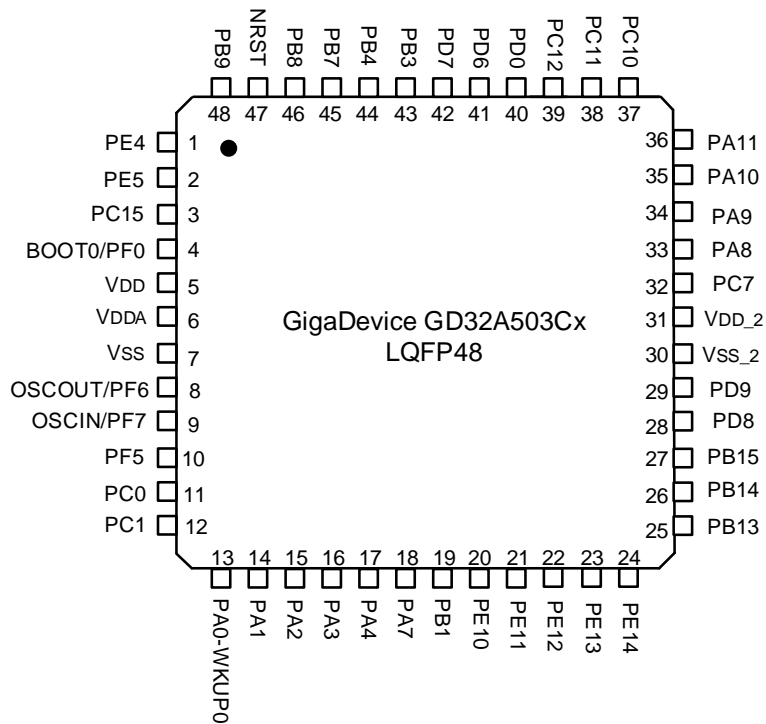
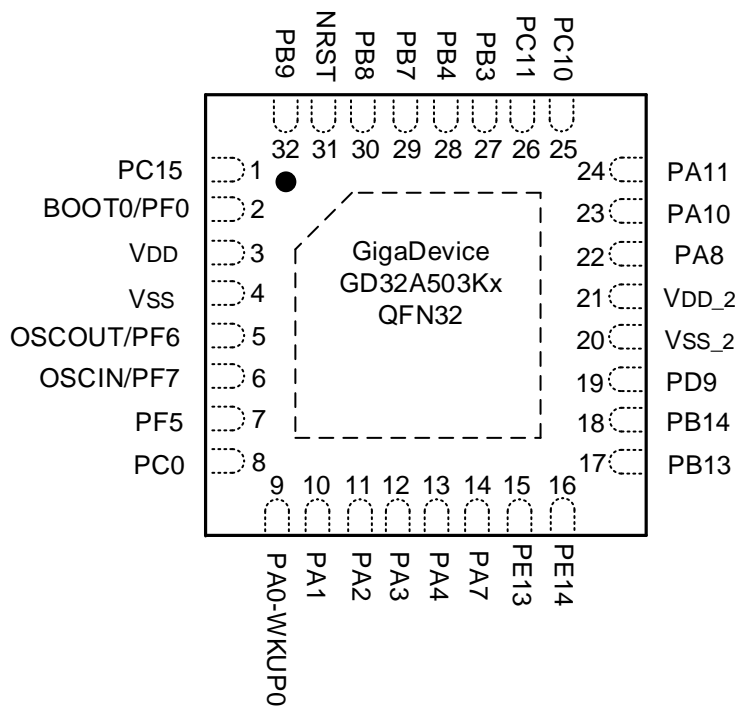


Figure 2-5. GD32A503Kx QFN32 pinouts



2.4. Memory map

Table 2-2. GD32A503xx memory map

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|---------------------------|---------------------------|---------------------------------|
| | | 0xE004 4400 - 0xE00F FFFF | Cortex M33 internal peripherals |
| | | 0xE004 4000 - 0xE004 43FF | DBG |
| | | 0xE000 0000 - 0xE004 3FFF | Cortex M33 internal peripherals |
| External RAM | | 0x6000 0000 - 0x9FFF FFFF | Reserved |
| Peripheral | AHB1 | 0x5000 0000 - 0x5FFF FFFF | Reserved |
| | AHB2 | 0x4800 1800 - 0x4FFF FFFF | Reserved |
| | | 0x4800 1400 - 0x4800 17FF | GPIOF |
| | | 0x4800 1000 - 0x4800 13FF | GPIOE |
| | | 0x4800 0C00 - 0x4800 0FFF | GPIOD |
| | | 0x4800 0800 - 0x4800 0BFF | GPIOC |
| | | 0x4800 0400 - 0x4800 07FF | GPIOB |
| | | 0x4800 0000 - 0x4800 03FF | GPIOA |
| | AHB1 | 0x4003 8C00 - 0x47FF FFFF | Reserved |
| | | 0x4003 8400 - 0x4003 8BFF | MFCOM |
| | | 0x4002 3400 - 0x4003 83FF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1C00 - 0x4002 1FFF | Reserved |
| | | 0x4002 1800 - 0x4002 1BFF | Reserved |
| | | 0x4002 1400 - 0x4002 17FF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0C00 - 0x4002 0FFF | Reserved |
| | | 0x4002 0800 - 0x4002 0BFF | DMAMUX |
| | | 0x4002 0400 - 0x4002 07FF | DMA1 |
| | | 0x4002 0000 - 0x4002 03FF | DMA0 |
| | | APB2 | 0x4001 C000 - 0x4001 FFFF |
| | 0x4001 B000 - 0x4001 BFFF | | CAN1 |
| | 0x4001 A000 - 0x4001 AFFF | | CAN0 |
| | 0x4001 8800 - 0x4001 9FFF | | Reserved |
| | 0x4001 8400 - 0x4001 87FF | | TRIGSEL |
| | 0x4001 8000 - 0x4001 83FF | | Reserved |
| | 0x4001 7C00 - 0x4001 7FFF | | CMP |
| | 0x4001 5800 - 0x4001 7BFF | | Reserved |
| | 0x4001 5400 - 0x4001 57FF | TIMER20 | |

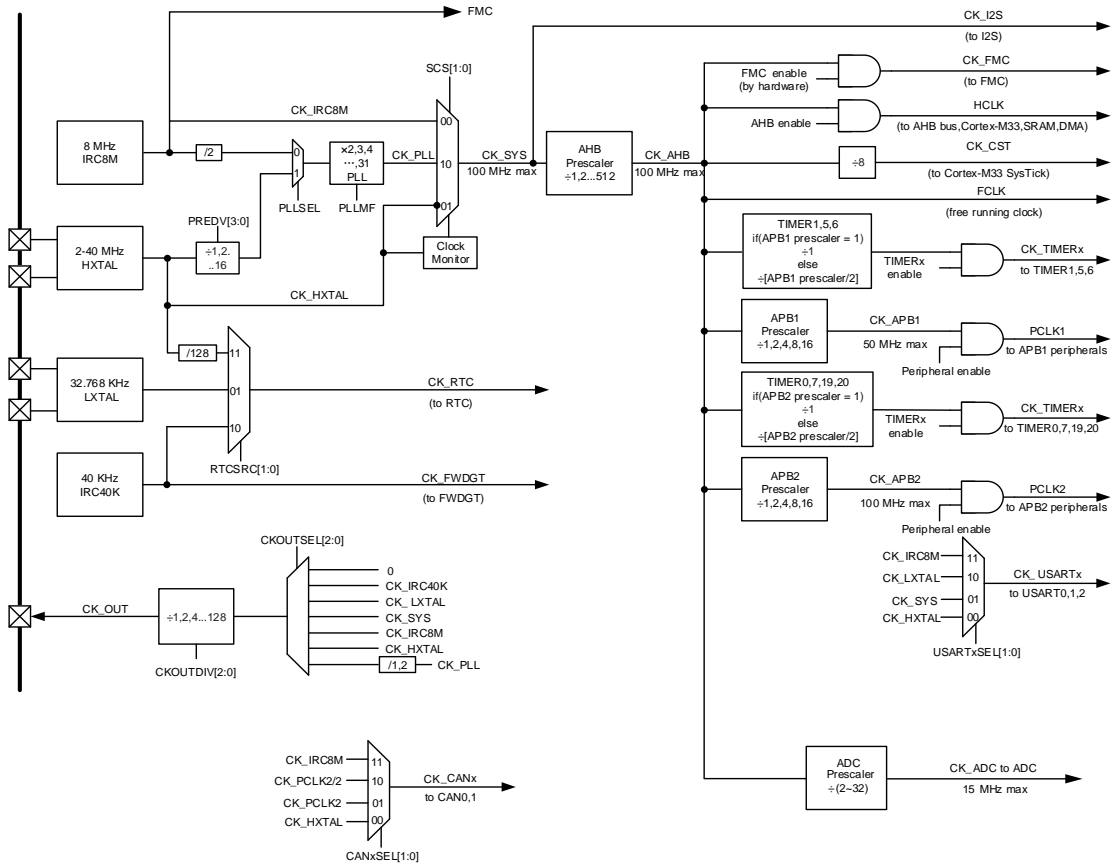
| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------------|----------|---------------------------|-------------|
| | | 0x4001 5000 - 0x4001 53FF | TIMER19 |
| | | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | | 0x4001 4800 - 0x4001 4BFF | Reserved |
| | | 0x4001 4400 - 0x4001 47FF | Reserved |
| | | 0x4001 4000 - 0x4001 43FF | Reserved |
| | | 0x4001 3C00 - 0x4001 3FFF | Reserved |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 |
| | | 0x4001 3400 - 0x4001 37FF | TIMER7 |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 - 0x4001 2FFF | TIMER0 |
| | | 0x4001 2800 - 0x4001 2BFF | ADC1 |
| | | 0x4001 2400 - 0x4001 27FF | ADC0 |
| | | 0x4001 2000 - 0x4001 23FF | Reserved |
| | | 0x4001 1C00 - 0x4001 1FFF | Reserved |
| | | 0x4001 1800 - 0x4001 1BFF | Reserved |
| | | 0x4001 1400 - 0x4001 17FF | Reserved |
| | | 0x4001 1000 - 0x4001 13FF | Reserved |
| | | 0x4001 0C00 - 0x4001 0FFF | Reserved |
| | | 0x4001 0800 - 0x4001 0BFF | Reserved |
| | | 0x4001 0400 - 0x4001 07FF | EXTI |
| | | 0x4001 0000 - 0x4001 03FF | SYSCFG |
| | APB1 | 0x4000 DC00 - 0x4000 FFFF | Reserved |
| | | 0x4000 D800 - 0x4000 DBFF | Reserved |
| | | 0x4000 D400 - 0x4000 D7FF | Reserved |
| | | 0x4000 D000 - 0x4000 D3FF | Reserved |
| | | 0x4000 CC00 - 0x4000 CFFF | Reserved |
| | | 0x4000 C800 - 0x4000 CBFF | Reserved |
| | | 0x4000 C400 - 0x4000 C7FF | Reserved |
| | | 0x4000 C000 - 0x4000 C3FF | Reserved |
| | | 0x4000 8800 - 0x4000 BFFF | Reserved |
| | | 0x4000 8400 - 0x4000 87FF | Reserved |
| | | 0x4000 8000 - 0x4000 83FF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | Reserved |
| | | 0x4000 7800 - 0x4000 7BFF | Reserved |
| | | 0x4000 7400 - 0x4000 77FF | DAC |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| 0x4000 6C00 - 0x4000 6FFF | BKP | | |
| 0x4000 6800 - 0x4000 6BFF | Reserved | | |
| 0x4000 6400 - 0x4000 67FF | Reserved | | |
| 0x4000 6000 - 0x4000 63FF | Reserved | | |

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|---------------------|
| | | 0x4000 5C00 - 0x4000 5FFF | Reserved |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | Reserved |
| | | 0x4000 4C00 - 0x4000 4FFF | Reserved |
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | Reserved |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1/I2S1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | Reserved |
| | | 0x4000 1C00 - 0x4000 1FFF | Reserved |
| | | 0x4000 1800 - 0x4000 1BFF | Reserved |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | Reserved |
| | | 0x4000 0800 - 0x4000 0BFF | Reserved |
| | | 0x4000 0400 - 0x4000 07FF | Reserved |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | | 0x2000 D000 - 0x3FFF FFFF | Reserved |
| | | 0x2000 C000 - 0x2000 CFFF | Shared SRAM(4KB) |
| | | 0x2000 5000 - 0x2000 BFFF | SRAM(48KB) |
| | | 0x2000 2000 - 0x2000 4FFF | |
| | | 0x2000 1000 - 0x2000 1FFF | |
| | | 0x2000 0000 - 0x2000 0FFF | |
| Code | | 0x1FFF FC4 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF FC00 - 0x1FFF FC0F | Reserved |
| | | 0x1FFF F818 - 0x1FFF BFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F817 | Option Bytes (24B) |
| | | 0x1FFF B000 - 0x1FFF F7FF | System memory(18KB) |
| | | 0x1FFF 7400 - 0x1FFF AFFF | Reserved |
| | | 0x1FFF 7000 - 0x1FFF 73FF | OTP(1KB) |
| | | 0x0A00 D000 - 0x1FFF 6FFF | Reserved |
| | | 0x0A00 C000 - 0x0A00 CFFF | Shared SRAM(4KB) |
| | | 0x0A00 0000 - 0x0A00 BFFF | SRAM(48KB) |

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|-----------------------------------|
| | | 0x08C0 1000 - 0x09FF FFFF | Reserved |
| | | 0x08C0 0000 - 0x08C0 0FFF | EEPROM(4KB) |
| | | 0x0881 0000 - 0x08BF FFFF | Reserved |
| | | 0x0880 0000 - 0x0880 FFFF | DFlash(64KB) |
| | | 0x0808 0000 - 0x0871 FFFF | Reserved |
| | | 0x0806 0000 - 0x0807 FFFF | Reserved |
| | | 0x0802 0000 - 0x0805 FFFF | Main Flash memory |
| | | 0x0801 0000 - 0x0801 FFFF | |
| | | 0x0800 0000 - 0x0800 FFFF | |
| | | 0x0006 0000 - 0x07FF FFFF | Reserved |
| | | 0x0002 0000 - 0x0005 FFFF | Aliased to Flash or system memory |
| | | 0x0001 0000 - 0x0001 FFFF | |
| | | 0x0000 0000 - 0x0000 FFFF | |

2.5. Clock tree

Figure 2-6. GD32A503xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

- HXTAL: High speed crystal oscillator
- LXTAL: Low speed crystal oscillator
- IRC8M: Internal 8M RC oscillator
- IRC40K: Internal 40K RC oscillator

2.6. Pin definitions

2.6.1. GD32A503Vx LQFP100 pin definitions

Table 2-3. GD32A503Vx LQFP100 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| PE2 | 1 | I/O | 5VT | Default: PE2 Alternate: TIMER19_MCH3, USART1_RTS, USART1_DE, MFCOM_D3, TRIGSEL_OUT7, EVENTOUT |
| PE3 | 2 | I/O | 5VT | Default: PE3 Alternate: TIMER19_CH3, USART1_CTS, MFCOM_D2, TRIGSEL_OUT6, EVENTOUT |
| PE4 | 3 | I/O | 5VT | Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT |
| PE5 | 4 | I/O | 5VT | Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT |
| PE6 | 5 | I/O | 5VT | Default: PE6 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER19_MCH2, I2S1_MCK, MFCOM_D5, TRIGSEL_OUT5, EVENTOUT |
| PC13 | 6 | I/O | | Default: PC13 Alternate: CK_OUT, TIMER19_CH2, MFCOM_D4, TRIGSEL_OUT4, EVENTOUT Additional: WKUP1, OSC32IN ⁽⁴⁾ |
| PC14-OSC32IN | 7 | I/O | | Default: PC14 Alternate: TIMER19_BRKIN0, EVENTOUT Additional: OSC32IN ⁽⁴⁾ |
| PC15 | 8 | I/O | | Default: PC15 Alternate: TIMER_ETI2 ⁽³⁾ , TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT |
| BOOT0/PF0 | 9 | I | | Default: PF0 ⁽⁴⁾ Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0 |
| V _{DD} | 10 | P | | Default: V _{DD} |
| V _{DDA} | 11 | P | | Default: V _{DDA} |
| V _{REF+} | 12 | P | | Default: V _{REF+} |
| V _{REF-} | 13 | P | | Default: V _{REF-} |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|--|
| V _{SS} | 14 | P | | Default: V _{SS} |
| PF6-OSCOU | 15 | O | | Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT |
| PF7-OSCIN | 16 | I | | Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN |
| PF1 | 17 | I/O | | Default: PF1 Alternate: TIMER0_BRKIN1, TIMER19_BRKIN1, EVENTOUT |
| PF2 | 18 | I/O | | Default: PF2 Alternate: TIMER0_BRKIN0, TIMER19_BRKIN0, USART2_RTS, USART2_DE, TRIGSEL_IN6, CMP_OUT, EVENTOUT |
| PF3 | 19 | I/O | | Default: PF3 Alternate: TIMER0_BRKIN3, USART2_TX, EVENTOUT |
| PF4 | 20 | I/O | | Default: PF4 Alternate: TIMER0_BRKIN2, USART2_RX, EVENTOUT |
| PF5 | 21 | I/O | | Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT |
| PC0 | 22 | I/O | | Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT |
| PC1 | 23 | I/O | | Default: PC1 Alternate: TIMER0_MCH3, USART2_CTS, EVENTOUT |
| PC2 | 24 | I/O | | Default: PC2 Alternate: CK_OUT, TIMER19_MCH2, USART1_TX, EVENTOUT |
| PC3 | 25 | I/O | | Default: PC3 Alternate: TIMER19_CH2, USART1_RX, EVENTOUT |
| PA0-WKUP0 | 26 | I/O | | Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0 |
| PA1 | 27 | I/O | | Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT |
| PA2 | 28 | I/O | | Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT |
| PA3 | 29 | I/O | | Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| PA4 | 30 | I/O | | Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5 |
| PA5 | 31 | I/O | | Default: PA5 Alternate: TIMER19_BRKIN3, USART2_TX, EVENTOUT Additional: CMP_IM_IP6 |
| PA6 | 32 | I/O | | Default: PA6 Alternate: TIMER19_BRKIN2, USART2_RX, EVENTOUT Additional: CMP_IM_IP7 |
| PA7 | 33 | I/O | | Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT, USART2_CK Additional: DAC_OUT |
| PC4 | 34 | I/O | | Default: PC4 Alternate: TIMER19_CH1, USART2_RTS, USART2_DE, EVENTOUT |
| PC5 | 35 | I/O | | Default: PC5 Alternate: TIMER19_MCH0, TIMER19_CH0, USART2_CTS, EVENTOUT |
| PB0 | 36 | I/O | | Default: PB0 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT |
| V _{SS_1} | 37 | P | | Default: V _{SS_1} |
| V _{DD_1} | 38 | P | | Default: V _{DD_1} |
| PB1 | 39 | I/O | | Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9 ⁽⁵⁾ |
| PB2 | 40 | I/O | 5VT | Default: PB2 Alternate: TIMER0_CH0, TIMER7_CH3, EVENTOUT Additional: ADC0_IN8 ⁽⁵⁾ |
| PE7 | 41 | I/O | 5VT | Default: PE7 Alternate: TIMER7_MCH2, TIMER19_BRKIN3, MFCOM_D0, EVENTOUT |
| PE8 | 42 | I/O | 5VT | Default: PE8 Alternate: TIMER7_CH2, TIMER19_BRKIN2, MFCOM_D1, EVENTOUT |
| PE9 | 43 | I/O | 5VT | Default: PE9 Alternate: TIMER7_BRKIN3, EVENTOUT Additional: ADC0_IN15 |
| PE10 | 44 | I/O | 5VT | Default: PE10 Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| PE11 | 45 | I/O | 5VT | Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13 |
| PE12 | 46 | I/O | 5VT | Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12 |
| PE13 | 47 | I/O | 5VT | Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7 |
| PE14 | 48 | I/O | 5VT | Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6 |
| PE15 | 49 | I/O | 5VT | Default: PE15 Alternate: TIMER20_MCH3, TIMER19_MCH3, SPI0_IO2, USART2_RTS, USART2_DE, EVENTOUT |
| PB10 | 50 | I/O | 5VT | Default: PB10 Alternate: TIEMR20_CH3, TIMER19_CH3, SPI0_IO3, USART2_CTS, EVENTOUT |
| PB11 | 51 | I/O | 5VT | Default: PB11 Alternate: TIMER20_MCH2, TRIGSEL_IN10, TIMER1_CH3, EVENTOUT |
| PB12 | 52 | I/O | 5VT | Default: PB12 Alternate: TIMER20_CH2, TRIGSEL_IN11, EVENTOUT |
| PB13 | 53 | I/O | 5VT | Default: PB13 Alternate: TIMER_ETIO ⁽³⁾ , SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15 ⁽⁵⁾ |
| PB14 | 54 | I/O | 5VT | Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14 ⁽⁵⁾ |
| PB15 | 55 | I/O | 5VT | Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT |
| PD8 | 56 | I/O | 5VT | Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT |
| PD9 | 57 | I/O | 5VT | Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| | | | | USART1_DE, EVENTOUT Additional: ADC0_IN3 |
| PD10 | 58 | I/O | 5VT | Default: PD10 Alternate: TIMER0_BRKIN1, SPI1_NSS, I2S1_WS, USART1_CTS, EVENTOUT Additional: ADC0_IN2 |
| PD11 | 59 | I/O | 5VT | Default: PD11 Alternate: TIMER0_MCH3, TIMER20_BRKIN0, EVENTOUT, I2C1_SMBA |
| V _{SS_2} | 60 | P | | Default: V _{SS_2} |
| V _{DD_2} | 61 | P | | Default: V _{DD_2} |
| PD12 | 62 | I/O | 5VT | Default: PD12 Alternate: TIMER0_CH3, TIMER20_BRKIN0, EVENTOUT |
| PD13 | 63 | I/O | 5VT | Default: PD13 Alternate: TIMER0_MCH2, SPI1_NSS, I2S1_WS, EVENTOUT |
| PD14 | 64 | I/O | 5VT | Default: PD14 Alternate: TIMER0_CH2, SPI1_MOSI, I2S1_SD, EVENTOUT Additional: ADC1_IN15 ⁽⁵⁾ |
| PD15 | 65 | I/O | 5VT | Default: PD15 Alternate: TIMER0_MCH1, SPI1_MISO, EVENTOUT Additional: ADC1_IN14 ⁽⁵⁾ |
| PC6 | 66 | I/O | 5VT | Default: PC6 Alternate: TIMER0_CH1, SPI1_SCK, I2S1_CK, EVENTOUT Additional: ADC1_IN9, ADC0_IN9 ⁽⁵⁾ |
| PC7 | 67 | I/O | 5VT | Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1, I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8 ⁽⁵⁾ |
| PC8 | 68 | I/O | 5VT | Default: PC8 Alternate: TIMER0_CH0, TIMER20_BRKIN2, EVENTOUT Additional: ADC1_IN7 |
| PC9 | 69 | I/O | 5VT | Default: PC9 Alternate: TIMER0_BRKIN3, TIMER20_BRKIN3, EVENTOUT Additional: ADC1_IN6 |
| PA8 | 70 | I/O | 5VT | Default: PA8 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|--|
| | | | | Alternate: TIMER0_BRKIN0, TIMER20_MCH2, SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI |
| PA9 | 71 | I/O | 5VT | Default: PA9 Alternate: TIMER20_CH2, SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2 |
| PA10 | 72 | I/O | 5VT | Default: PA10 Alternate: TIMER20_MCH0, I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1 |
| PA11 | 73 | I/O | 5VT | Default: PA11 Alternate: TIMER20_CH0, I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0 |
| PA12 | 74 | I/O | 5VT | Default: PA12 Alternate: TIMER20_MCH1, I2C0_SMBA, USART0_CK, EVENTOUT |
| PA13 | 75 | I/O | 5VT | Default: PA13 Alternate: TIMER20_CH1, I2C0_SDA, EVENTOUT |
| PA14 | 76 | I/O | 5VT | Default: PA14 Alternate: TIMER20_MCH0, I2C0_SCL, EVENTOUT |
| PA15 | 77 | I/O | 5VT | Default: PA15 Alternate: TIMER20_CH0, EVENTOUT, TRIGSEL_IN12 |
| PC10 | 78 | I/O | 5VT | Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1 |
| PC11 | 79 | I/O | 5VT | Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0 |
| PC12 | 80 | I/O | 5VT | Default: PC12 Alternate: TIMER20_MCH1, TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT Additional: ADC1_IN5 |
| PD0 | 81 | I/O | 5VT | Default: PD0 Alternate: TIMER20_CH1, TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| PD1 | 82 | I/O | 5VT | Default: PD1 Alternate: TIMER7_MCH1, SPI1_NSS, I2S1_WS, EVENTOUT Additional: ADC1_IN13 |
| PD2 | 83 | I/O | 5VT | Default: PD2 Alternate: TIMER7_CH1, SPI0_NSS, EVENTOUT Additional: ADC1_IN12 |
| PD3 | 84 | I/O | 5VT | Default: PD3 Alternate: TIMER20_MCH3, SPI0_NSS, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC1_IN11 |
| PD4 | 85 | I/O | 5VT | Default: PD4 Alternate: TIMER20_CH3, TIMER1_CH2, SPI0_MOSI, USART1_CTS, EVENTOUT Additional: ADC1_IN10 |
| V _{SS_3} | 86 | P | | Default: V _{SS_3} |
| V _{DD_3} | 87 | P | | Default: V _{DD_3} |
| PD5 | 88 | I/O | 5VT | Default: PD5 Alternate: TIMER0_BRKIN0, TIMER20_BRKIN1, TIMER7_BRKIN0, USART1_CK, EVENTOUT |
| PD6 | 89 | I/O | 5VT | Default: PD6 Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL |
| PD7 | 90 | I/O | 5VT | Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA |
| PB3 | 91 | I/O | 5VT | Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT |
| PB4 | 92 | I/O | 5VT | Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT |
| PB5 | 93 | I/O | | Default: PB5 Alternate: TIMER7_BRKIN1, I2C0_SMBA, SPI0_MISO, SPI1_NSS, I2S1_WS, EVENTOUT |
| PB6 | 94 | I/O | 5VT | Default: PB6 Alternate: TIMER7_BRKIN2, TIMER_ETI1 ⁽³⁾ , SPI0_SCK, SPI1_MOSI, I2S1_SD, EVENTOUT |
| PB7 | 95 | I/O | 5VT | Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL |
| PB8 | 96 | I/O | 5VT | Default: JTCK, SWCLK, PB8 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| | | | | Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2 |
| NRST | 97 | I/O | | Default: NRST |
| PB9 | 98 | I/O | 5VT | Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1 |
| PE0 | 99 | I/O | 5VT | Default: PE0 Alternate: TIMER20_BRKIN2, TIMER7_BRKIN3, USART2_TX, MFCOM_D7, EVENTOUT |
| PE1 | 100 | I/O | 5VT | Default: PE1 Alternate: TIMER20_BRKIN3, USART2_RX, MFCOM_D6, EVENTOUT |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) This function is controlled by SYSCFG_TIMERINSEL register.
- (4) This function is controlled by SYSCFG_CFG0 register.
- (5) This function is controlled by SYSCFG_CFG1 register.

2.6.2. GD32A503Rx LQFP64 pin definitions

Table 2-4. GD32A503Rx LQFP64 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| PE4 | 1 | I/O | 5VT | Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT |
| PE5 | 2 | I/O | 5VT | Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT |
| PE6 | 3 | I/O | 5VT | Default: PE6 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER19_MCH2, I2S1_MCK, MFCOM_D5, TRIGSEL_OUT5, EVENTOUT |
| PC13 | 4 | I/O | | Default: PC13 Alternate: CK_OUT, TIMER19_CH2, MFCOM_D4, TRIGSEL_OUT4, EVENTOUT Additional: WKUP1, OSC32IN ⁽⁴⁾ |
| PC15 | 5 | I/O | | Default: PC15 Alternate: TIMER_ETI2 ⁽³⁾ , TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT |
| BOOT0/PF0 | 6 | I | | Default: PF0 ⁽⁴⁾ Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0 |
| V _{DD} | 7 | P | | Default: V _{DD} |
| V _{DDA} | 8 | P | | Default: V _{DDA} |
| V _{REF+} | 9 | P | | Default: V _{REF+} |
| V _{SS} | 10 | P | | Default: V _{SS} |
| PF6-OSCOUT | 11 | O | | Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT |
| PF7-OSCIN | 12 | I | | Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN |
| PF2 | 13 | I/O | | Default: PF2 Alternate: TIMER0_BRKIN0, TIMER19_BRKIN0, USART2_RTS, USART2_DE, TRIGSEL_IN6, CMP_OUT, EVENTOUT |
| PF5 | 14 | I/O | | Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT |
| PC0 | 15 | I/O | | Default: PC0 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------|------|-------------------------|--------------------------|--|
| | | | | Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT |
| PC1 | 16 | I/O | | Default: PC1 Alternate: TIMER0_MCH3, USART2_CTS, EVENTOUT |
| PA0-WKUP0 | 17 | I/O | | Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0 |
| PA1 | 18 | I/O | | Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT |
| PA2 | 19 | I/O | | Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT |
| PA3 | 20 | I/O | | Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4 |
| PA4 | 21 | I/O | | Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5 |
| PA5 | 22 | I/O | | Default: PA5 Alternate: TIMER19_BRKIN3, USART2_TX, EVENTOUT Additional: CMP_IM_IP6 |
| PA6 | 23 | I/O | | Default: PA6 Alternate: TIMER19_BRKIN2, USART2_RX, EVENTOUT Additional: CMP_IM_IP7 |
| PA7 | 24 | I/O | | Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT, USART2_CK Additional: DAC_OUT |
| PB1 | 25 | I/O | | Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9 |
| PB2 | 26 | I/O | 5VT | Default: PB2 Alternate: TIMER0_CH0, TIMER7_CH3, EVENTOUT Additional: ADC0_IN8 ⁽⁵⁾ |
| PE9 | 27 | I/O | 5VT | Default: PE9 Alternate: TIMER7_BRKIN3, EVENTOUT Additional: ADC0_IN15 |
| PE10 | 28 | I/O | 5VT | Default: PE10 Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|---|
| PE11 | 29 | I/O | 5VT | Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13 |
| PE12 | 30 | I/O | 5VT | Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12 |
| PE13 | 31 | I/O | 5VT | Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7 |
| PE14 | 32 | I/O | 5VT | Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6 |
| PB13 | 33 | I/O | 5VT | Default: PB13 Alternate: TIMER_ETIO ⁽³⁾ , SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15 ⁽⁵⁾ |
| PB14 | 34 | I/O | 5VT | Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14 ⁽⁵⁾ |
| PB15 | 35 | I/O | 5VT | Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT |
| PD8 | 36 | I/O | 5VT | Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT |
| PD9 | 37 | I/O | 5VT | Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC0_IN3 |
| PD10 | 38 | I/O | 5VT | Default: PD10 Alternate: TIMER0_BRKIN1, SPI1_NSS, I2S1_WS, USART1_CTS, EVENTOUT Additional: ADC0_IN2 |
| PD11 | 39 | I/O | 5VT | Default: PD11 Alternate: TIMER0_MCH3, TIMER20_BRKIN0 ⁽⁶⁾ , EVENTOUT, I2C1_SMBA |
| V _{SS_2} | 40 | P | | Default: V _{SS_2} |
| V _{DD_2} | 41 | P | | Default: V _{DD_2} |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| PC7 | 42 | I/O | 5VT | Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1 ⁽⁶⁾ , I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8 ⁽⁵⁾ |
| PC8 | 43 | I/O | 5VT | Default: PC8 Alternate: TIMER0_CH0, TIMER20_BRKIN2 ⁽⁶⁾ , EVENTOUT Additional: ADC1_IN7 |
| PC9 | 44 | I/O | 5VT | Default: PC9 Alternate: TIMER0_BRKIN3, TIMER20_BRKIN3 ⁽⁶⁾ , EVENTOUT Additional: ADC1_IN6 |
| PA8 | 45 | I/O | 5VT | Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2 ⁽⁶⁾ , SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI |
| PA9 | 46 | I/O | 5VT | Default: PA9 Alternate: TIMER20_CH2 ⁽⁶⁾ , SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2 |
| PA10 | 47 | I/O | 5VT | Default: PA10 Alternate: TIMER20_MCH0 ⁽⁶⁾ , I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1 |
| PA11 | 48 | I/O | 5VT | Default: PA11 Alternate: TIMER20_CH0 ⁽⁶⁾ , I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0 |
| PC10 | 49 | I/O | 5VT | Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1 |
| PC11 | 50 | I/O | 5VT | Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0 |
| PC12 | 51 | I/O | 5VT | Default: PC12 Alternate: TIMER20_MCH1 ⁽⁶⁾ , TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT Additional: ADC1_IN5 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|--|
| PD0 | 52 | I/O | 5VT | Default: PD0 Alternate: TIMER20_CH1 ⁽⁶⁾ , TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4 |
| PD3 | 53 | I/O | 5VT | Default: PD3 Alternate: TIMER20_MCH3 ⁽⁶⁾ , SPI0_NSS, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC1_IN11 |
| PD4 | 54 | I/O | 5VT | Default: PD4 Alternate: TIMER20_CH3 ⁽⁶⁾ , TIMER1_CH2, SPI0_MOSI, USART1_CTS, EVENTOUT Additional: ADC1_IN10 |
| PD6 | 55 | I/O | 5VT | Default: PD6 Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL |
| PD7 | 56 | I/O | 5VT | Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA |
| PB3 | 57 | I/O | 5VT | Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT |
| PB4 | 58 | I/O | 5VT | Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT |
| PB5 | 59 | I/O | | Default: PB5 Alternate: TIMER7_BRKIN1, I2C0_SMBA, SPI0_MISO, SPI1_NSS, I2S1_WS, EVENTOUT |
| PB6 | 60 | I/O | 5VT | Default: PB6 Alternate: TIMER7_BRKIN2, TIMER_ET11 ⁽³⁾ , SPI0_SCK, SPI1_MOSI, I2S1_SD, EVENTOUT |
| PB7 | 61 | I/O | 5VT | Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL |
| PB8 | 62 | I/O | 5VT | Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2 |
| NRST | 63 | I/O | | Default: NRST |
| PB9 | 64 | I/O | 5VT | Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1 |

Notes:

(1) Type: I = input, O = output, P = power.

- (2) I/O Level: 5VT = 5 V tolerant.
- (3) This function is controlled by SYSCFG_TIMERINSEL register.
- (4) This function is controlled by SYSCFG_CFG0 register.
- (5) This function is controlled by SYSCFG_CFG1 register.
- (6) Functions are available on GD32A503RC/D devices only.

2.6.3. GD32A503Cx LQFP48 pin definitions

Table 2-5. GD32A503Cx LQFP48 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|--|
| PE4 | 1 | I/O | 5VT | Default: PE4 Alternate: TIMER0_MCH1, TIMER19_MCH0, SPI1_MISO, MFCOM_D1, TRIGSEL_OUT2, EVENTOUT |
| PE5 | 2 | I/O | 5VT | Default: PE5 Alternate: TIMER0_CH1, TIMER19_CH0, SPI1_SCK, I2S1_CK, MFCOM_D0, TRIGSEL_OUT1, EVENTOUT |
| PC15 | 3 | I/O | | Default: PC15 Alternate: TIMER_ETI2 ⁽³⁾ , TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT |
| BOOT0/PF0 | 4 | I | | Default: PF0 ⁽⁴⁾ Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0 |
| V _{DD} | 5 | P | | Default: V _{DD} |
| V _{DDA} | 6 | P | | Default: V _{DDA} |
| V _{SS} | 7 | P | | Default: V _{SS} |
| PF6-OSCOUT | 8 | O | | Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT |
| PF7-OSCIN | 9 | I | | Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN |
| PF5 | 10 | I/O | | Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, USART1_CTS, EVENTOUT |
| PC0 | 11 | I/O | | Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT |
| PC1 | 12 | I/O | | Default: PC1 Alternate: TIMER0_MCH3, EVENTOUT |
| PA0-WKUP0 | 13 | I/O | | Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0 |
| PA1 | 14 | I/O | | Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT |
| PA2 | 15 | I/O | | Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT |
| PA3 | 16 | I/O | | Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| | | | | Additional: ADC0_IN11, CMP_IM_IP4 |
| PA4 | 17 | I/O | | Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5 |
| PA7 | 18 | I/O | | Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT Additional: DAC_OUT |
| PB1 | 19 | I/O | | Default: PB1 Alternate: TIMER0_MCH0, TIMER7_MCH3, EVENTOUT Additional: ADC0_IN9 ⁽⁵⁾ |
| PE10 | 20 | I/O | 5VT | Default: PE10 Alternate: TIMER7_BRKIN2, EVENTOUT, I2C1_SCL Additional: ADC0_IN14 |
| PE11 | 21 | I/O | 5VT | Default: PE11 Alternate: TIMER7_MCH1, TRIGSEL_IN8, EVENTOUT, I2C1_SDA Additional: ADC0_IN13 |
| PE12 | 22 | I/O | 5VT | Default: PE12 Alternate: TIMER7_CH1, TRIGSEL_IN9, EVENTOUT, I2C1_SMBA Additional: ADC0_IN12 |
| PE13 | 23 | I/O | 5VT | Default: PE13 Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7 |
| PE14 | 24 | I/O | 5VT | Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6 |
| PB13 | 25 | I/O | 5VT | Default: PB13 Alternate: TIMER_ETIO ⁽³⁾ , SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15 ⁽⁵⁾ |
| PB14 | 26 | I/O | 5VT | Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14 ⁽⁵⁾ |
| PB15 | 27 | I/O | 5VT | Default: PB15 Alternate: TIMER7_BRKIN1, USART1_TX, USART0_RTS, USART0_DE, EVENTOUT |
| PD8 | 28 | I/O | 5VT | Default: PD8 Alternate: TIMER7_BRKIN0, USART1_RX, USART0_CTS, EVENTOUT |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|---|
| PD9 | 29 | I/O | 5VT | Default: PD9 Alternate: TIMER0_BRKIN2, USART1_RTS, USART1_DE, EVENTOUT Additional: ADC0_IN3 |
| V _{SS_2} | 30 | P | | Default: V _{SS_2} |
| V _{DD_2} | 31 | P | | Default: V _{DD_2} |
| PC7 | 32 | I/O | 5VT | Default: PC7 Alternate: TIMER0_MCH0, TIMER20_BRKIN1 ⁽⁶⁾ , I2S1_MCK, EVENTOUT Additional: ADC1_IN8, ADC0_IN8 ⁽⁵⁾ |
| PA8 | 33 | I/O | 5VT | Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2 ⁽⁶⁾ , SPI1_NSS, I2S1_WS, MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI |
| PA9 | 34 | I/O | 5VT | Default: PA9 Alternate: TIMER20_CH2 ⁽⁶⁾ , SPI1_MOSI, I2S1_SD, MFCOM_D6, MFCOM_D4, TRIGSEL_IN5, EVENTOUT Additional: ADC1_IN2 |
| PA10 | 35 | I/O | 5VT | Default: PA10 Alternate: TIMER20_MCH0 ⁽⁶⁾ , I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1 |
| PA11 | 36 | I/O | 5VT | Default: PA11 Alternate: TIMER20_CH0 ⁽⁶⁾ , I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0 |
| PC10 | 37 | I/O | 5VT | Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1 |
| PC11 | 38 | I/O | 5VT | Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0 |
| PC12 | 39 | I/O | 5VT | Default: PC12 Alternate: TIMER20_MCH1 ⁽⁶⁾ , TIMER7_CH0, USART1_TX, CAN1_TX, EVENTOUT Additional: ADC1_IN5 |
| PD0 | 40 | I/O | 5VT | Default: PD0 Alternate: TIMER20_CH1 ⁽⁶⁾ , TIMER7_CH1, USART1_RX, CAN1_RX, EVENTOUT Additional: ADC1_IN4 |
| PD6 | 41 | I/O | 5VT | Default: PD6 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|--|
| | | | | Alternate: TIMER7_MCH3, TIMER19_CH0, CAN1_TX, EVENTOUT, I2C1_SCL |
| PD7 | 42 | I/O | 5VT | Default: PD7 Alternate: TIMER7_CH3, TIMER19_CH1, CAN1_RX, EVENTOUT, I2C1_SDA |
| PB3 | 43 | I/O | 5VT | Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT |
| PB4 | 44 | I/O | 5VT | Default: JTDO, PB4 Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT |
| PB7 | 45 | I/O | 5VT | Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL |
| PB8 | 46 | I/O | 5VT | Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2 |
| NRST | 47 | I/O | | Default: NRST |
| PB9 | 48 | I/O | 5VT | Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) This function is controlled by SYSCFG_TIMERINSEL register.
- (4) This function is controlled by SYSCFG_CFG0 register.
- (5) This function is controlled by SYSCFG_CFG1 register.
- (6) Functions are available on GD32A503CC devices only.

2.6.4. GD32A503Kx QFN32 pin definitions

Table 2-6. GD32A503Kx QFN32 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|--|
| PC15 | 1 | I/O | | Default: PC15 Alternate: TIMER_ETI2 ⁽³⁾ , TIMER19_MCH1, TIMER19_CH1, CAN0_TX, MFCOM_D7, EVENTOUT Additional: OSC32OUT |
| BOOT0/PF0 | 2 | I | | Default: PF0 ⁽⁴⁾ Alternate: TIMER19_CH1, CAN0_RX, MFCOM_D6, EVENTOUT Additional: BOOT0 |
| V _{DD} | 3 | P | | Default: V _{DD} |
| V _{SS} | 4 | P | | Default: V _{SS} |
| PF6-OSCOUT | 5 | O | | Default: PF6 Alternate: I2C0_SCL, EVENTOUT Additional: OSCOUT |
| PF7-OSCIN | 6 | I | | Default: PF7 Alternate: I2C0_SDA, EVENTOUT Additional: OSCIN |
| PF5 | 7 | I/O | | Default: PF5 Alternate: TIMER0_MCH0, SPI0_MISO, EVENTOUT |
| PC0 | 8 | I/O | | Default: PC0 Alternate: TIMER0_CH0, SPI0_SCK, EVENTOUT |
| PA0-WKUP0 | 9 | I/O | | Default: PA0 Alternate: TIMER0_CH3, EVENTOUT Additional: CMP_IM_IP3, WKUP0 |
| PA1 | 10 | I/O | | Default: PA1 Alternate: CK_OUT, TIMER0_MCH2, SPI0_NSS, TRIGSEL_IN0, EVENTOUT |
| PA2 | 11 | I/O | | Default: PA2 Alternate: TIMER0_CH2, SPI0_MOSI, TRIGSEL_IN1, EVENTOUT |
| PA3 | 12 | I/O | | Default: PA3 Alternate: TIMER0_MCH1, USART0_TX, CAN0_TX, TIMER1_CH3, EVENTOUT Additional: ADC0_IN11, CMP_IM_IP4 |
| PA4 | 13 | I/O | | Default: PA4 Alternate: TIMER0_CH1, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN10, CMP_IM_IP5 |
| PA7 | 14 | I/O | | Default: PA7 Alternate: TIMER19_MCH1, TIMER1_CH1, TIMER19_BRKIN1, TRIGSEL_IN7, EVENTOUT Additional: DAC_OUT |
| PE13 | 15 | I/O | 5VT | Default: PE13 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--|
| | | | | Alternate: TIMER7_MCH0, TIMER7_CH0, SPI0_MISO, TRIGSEL_IN2, EVENTOUT Additional: ADC0_IN7 |
| PE14 | 16 | I/O | 5VT | Default: PE14 Alternate: TIMER7_CH0, TIMER7_CH1, SPI0_SCK, TRIGSEL_IN3, EVENTOUT Additional: ADC0_IN6 |
| PB13 | 17 | I/O | 5VT | Default: PB13 Alternate: TIMER_ETIO ⁽³⁾ , SPI0_MOSI, USART0_TX, CAN0_TX, EVENTOUT Additional: ADC0_IN5, ADC1_IN15 ⁽⁵⁾ |
| PB14 | 18 | I/O | 5VT | Default: PB14 Alternate: TIMER1_CH2, SPI0_NSS, USART0_RX, CAN0_RX, EVENTOUT Additional: ADC0_IN4, ADC1_IN14 ⁽⁵⁾ |
| PD9 | 19 | I/O | 5VT | Default: PD9 Alternate: TIMER0_BRKIN2, EVENTOUT Additional: ADC0_IN3 |
| V _{SS_2} | 20 | P | | Default: V _{SS_2} |
| V _{DD_2} | 21 | P | | Default: V _{DD_2} |
| PA8 | 22 | I/O | 5VT | Default: PA8 Alternate: TIMER0_BRKIN0, TIMER20_MCH2 ⁽⁶⁾ , MFCOM_D7, MFCOM_D5, TRIGSEL_IN4, EVENTOUT Additional: ADC1_IN3, NMI |
| PA10 | 23 | I/O | 5VT | Default: PA10 Alternate: TIMER20_MCH0 ⁽⁶⁾ , I2C0_SCL, USART0_TX, MFCOM_D5, EVENTOUT Additional: ADC1_IN1 |
| PA11 | 24 | I/O | 5VT | Default: PA11 Alternate: TIMER20_CH0 ⁽⁶⁾ , I2C0_SDA, USART0_RX, MFCOM_D4, EVENTOUT, TRIGSEL_IN13 Additional: ADC1_IN0 |
| PC10 | 25 | I/O | 5VT | Default: PC10 Alternate: TIMER7_MCH0, TIMER7_CH0, I2C0_SDA, USART0_RTS, USART0_DE, MFCOM_D3, TRIGSEL_OUT0, EVENTOUT Additional: ADC0_IN1, CMP_IM_IP1 |
| PC11 | 26 | I/O | 5VT | Default: PC11 Alternate: TIMER19_MCH0, TIMER19_CH0, I2C0_SCL, USART0_CTS, MFCOM_D2, TRIGSEL_OUT3, EVENTOUT Additional: ADC0_IN0, CMP_IM_IP0 |
| PB3 | 27 | I/O | 5VT | Default: NJTRST, PB3 Alternate: TIMER7_MCH2, SPI0_IO2, MFCOM_D1, EVENTOUT |
| PB4 | 28 | I/O | 5VT | Default: JTDO, PB4 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|--|
| | | | | Alternate: TIMER7_CH2, SPI0_IO3, MFCOM_D0, EVENTOUT |
| PB7 | 29 | I/O | 5VT | Default: JTDI, PB7 Alternate: TIMER19_CH0, TIMER19_CH1, EVENTOUT, I2C1_SCL |
| PB8 | 30 | I/O | 5VT | Default: JTCK, SWCLK, PB8 Alternate: TIMER7_CH0, TIMER7_CH1, EVENTOUT, I2C1_SDA Additional: CMP_IM_IP2 |
| NRST | 31 | I/O | | Default: NRST |
| PB9 | 32 | I/O | 5VT | Default: JTMS, SWDIO, PB9 Alternate: CMP_OUT, EVENTOUT, I2C1_SMBA Additional: BOOT1 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) This function is controlled by SYSCFG_TIMERINSEL register.
- (4) This function is controlled by SYSCFG_CFG0 register.
- (5) This function is controlled by SYSCFG_CFG1 register.
- (6) Functions are available on GD32A503KC devices only.

2.6.5. GD32A503xx pin alternate functions

Table 2-7. Port A alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|--------|---------------------------------|---------------------------------|--------------------|---|------------------------------|--------------|------------------|-----|----------|
| PA0 | | TIMER0_C H3 | | | | | | | | EVENTOUT |
| PA1 | CK_OUT | TIMER0_M CH2 | | | SPI0_NSS | | | TRIGSEL _IN0 | | EVENTOUT |
| PA2 | | TIMER0_C H2 | | | SPI0_MOS I | | | TRIGSEL _IN1 | | EVENTOUT |
| PA3 | | TIMER0_M CH1 | TIMER1_C H3 | | | USART0 _TX | CAN0_TX | | | EVENTOUT |
| PA4 | | TIMER0_C H1 | | | | USART0 _RX | CAN0_RX | | | EVENTOUT |
| PA5 | | | TIMER19_ BRKIN3 | | | USART2 _TX | | | | EVENTOUT |
| PA6 | | | TIMER19_ BRKIN2 | | | USART2 _RX | | | | EVENTOUT |
| PA7 | | TIMER19_ MCH1 | TIMER1_C H1 | TIMER19_ BRKIN1 | | USART2 _CK ⁽³⁾ | | TRIGSEL _IN7 | | EVENTOUT |
| PA8 | | TIMER0_B RKIN0 | TIMER20_ MCH2 ⁽⁴⁾ | | SPI1_NSS ⁽²⁾ / I2S1_WS ⁽²⁾ | MFCOM_ D7 | MFCOM_D 5 | TRIGSEL _IN4 | | EVENTOUT |
| PA9 | | TIMER20_ CH2 ⁽⁴⁾ | | | SPI1_MOS I/I2S1_SD | MFCOM_ D6 | MFCOM_D 4 | TRIGSEL _IN5 | | EVENTOUT |
| PA10 | | TIMER20_ MCH0 ⁽⁴⁾ | | I2C0_SCL | | USART0 _TX | MFCOM_D 5 | | | EVENTOUT |
| PA11 | | TIMER20_ CH0 ⁽⁴⁾ | | I2C0_SDA | | USART0 _RX | MFCOM_D 4 | TRIGSEL _IN13 | | EVENTOUT |
| PA12 | | TIMER20_ MCH1 | | I2C0_SMB A | | USART0 _CK | | | | EVENTOUT |
| PA13 | | TIMER20_ CH1 | | I2C0_SDA | | | | | | EVENTOUT |
| PA14 | | TIMER20_ MCH0 | | I2C0_SCL | | | | | | EVENTOUT |
| PA15 | | TIMER20_ CH0 | | | | | | TRIGSEL _IN12 | | EVENTOUT |

Table 2-8. Port B alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|------------------|------------------|-----|-----|-----|-----|-----|-----|----------|
| PB0 | | TIMER19_ MCH0 | TIMER19_ MCH1 | | | | | | | EVENTOUT |



| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-------------------------------|------------------|-------------------|-------------------------------|---------------|----------------------------------|--------------|------------------|-----|----------|
| | | CH0 | CH1 | | | | | | | |
| PB1 | | TIMER0_M CH0 | TIMER7_M CH3 | | | | | | | EVENTOUT |
| PB2 | | TIMER0_C H0 | TIMER7_C H3 | | | | | | | EVENTOUT |
| PB3 | NJTRST | TIMER7_M CH2 | | | SPI0_IO2 | | MFCOM_D 1 | | | EVENTOUT |
| PB4 | JTDO | TIMER7_C H2 | | | SPI0_IO3 | | MFCOM_D 0 | | | EVENTOUT |
| PB5 | | | TIMER7_B RKIN1 | I2C0_SMB A | SPI0_MIS O | SPI1_NS S/I2S1_ WS | | | | EVENTOUT |
| PB6 | | | TIMER7_B RKIN2 | TIMER_ETI 1 ⁽¹⁾ | SPI0_SCK | SPI1_MO SI/I2S1_ SD | | | | EVENTOUT |
| PB7 | JTDI | TIMER19_ CH0 | TIMER19_ CH1 | | | I2C1_SC L | | | | EVENTOUT |
| PB8 | JTCK/SW CLK | TIMER7_C H0 | TIMER7_C H1 | | | I2C1_SD A | | | | EVENTOUT |
| PB9 | JTMS/SW DIO | | | | | I2C1_SM BA | | CMP_OU T | | EVENTOUT |
| PB10 | | TIMER20_ CH3 | TIMER19_ CH3 | | SPI0_IO3 | USART2 _CTS | | | | EVENTOUT |
| PB11 | | TIMER20_ MCH2 | TIMER1_C H3 | | | | | TRIGSEL _IN10 | | EVENTOUT |
| PB12 | | TIMER20_ CH2 | | | | | | TRIGSEL _IN11 | | EVENTOUT |
| PB13 | TIMER_E T10 ⁽¹⁾ | | | | SPI0_MOS I | USART0 _TX | CAN0_TX | | | EVENTOUT |
| PB14 | | TIMER1_C H2 | | | SPI0_NSS | USART0 _RX | CAN0_RX | | | EVENTOUT |
| PB15 | | | TIMER7_B RKIN1 | | USART1_T X | USART0 _RTS/ USART0 _DE | | | | EVENTOUT |

Table 2-9. Port C alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|----------------|-----|-----|----------|-----|-----|-----|-----|----------|
| PC0 | | TIMER0_C H0 | | | SPI0_SCK | | | | | EVENTOUT |



| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|---------------------------|-----------------------------|-------------------------------|----------|----------------------|---------------------------|----------|--------------|-----|----------|
| PC1 | | TIMER0_MCH3 | | | | USART2_CTS ⁽³⁾ | | | | EVENTOUT |
| PC2 | CK_OUT | TIMER19_MCH2 | | | | USART1_TX | | | | EVENTOUT |
| PC3 | | TIMER19_CH2 | | | | USART1_RX | | | | EVENTOUT |
| PC4 | | TIMER19_CH1 | | | | USART2_RTS/ USART2_DE | | | | EVENTOUT |
| PC5 | | TIMER19_MCH0 | TIMER19_CH0 | | | USART2_CTS | | | | EVENTOUT |
| PC6 | | TIMER0_CH1 | | | SPI1_SCK/ I2S1_CK | | | | | EVENTOUT |
| PC7 | | TIMER0_MCH0 | TIMER20_BRKIN1 ⁽⁴⁾ | | I2S1_MCK | | | | | EVENTOUT |
| PC8 | | TIMER0_CH0 | TIMER20_BRKIN2 ⁽⁴⁾ | | | | | | | EVENTOUT |
| PC9 | | TIMER0_BRKIN3 | TIMER20_BRKIN3 ⁽⁴⁾ | | | | | | | EVENTOUT |
| PC10 | | TIMER7_MCH0 | TIMER7_CH0 | I2C0_SDA | | USART0_RTS/ USART0_DE | MFCOM_D3 | TRIGSEL_OUT0 | | EVENTOUT |
| PC11 | | TIMER19_MCH0 | TIMER19_CH0 | I2C0_SCL | | USART0_CTS | MFCOM_D2 | TRIGSEL_OUT3 | | EVENTOUT |
| PC12 | | TIMER20_MCH1 ⁽⁴⁾ | TIMER7_CH0 | | | USART1_TX | CAN1_TX | | | EVENTOUT |
| PC13 | CK_OUT | | TIMER19_CH2 | | | | MFCOM_D4 | TRIGSEL_OUT4 | | EVENTOUT |
| PC14 | | | TIMER19_BRKIN0 | | | | | | | EVENTOUT |
| PC15 | TIMER_ETI2 ⁽¹⁾ | TIMER19_MCH1 | TIMER19_CH1 | | | | CAN0_TX | MFCOM_D7 | | EVENTOUT |

Table 2-10. Port D alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|----------------------------|------------|-----|-----------|-----------|---------|-----|-----|----------|
| PD0 | | TIMER20_CH1 ⁽⁴⁾ | TIMER7_CH1 | | | USART1_RX | CAN1_RX | | | EVENTOUT |
| PD1 | | TIMER7_M | | | SPI1_NSS/ | | | | | EVENTOUT |

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|---------------------------------|-----------------------------------|-------------------|-----------------------|---|---------|-----|-----|----------|
| | | CH1 | | | I2S1_WS | | | | | |
| PD2 | | TIMER7_C H1 | | | SPI0_NSS | | | | | EVENTOUT |
| PD3 | | TIMER20_ MCH3 ⁽⁴⁾ | | | SPI0_NSS | USART1 _RTS/ USART1 _DE | | | | EVENTOUT |
| PD4 | | TIMER20_ CH3 ⁽⁴⁾ | TIMER1_C H2 | | SPI0_MOS I | USART1 _CTS | | | | EVENTOUT |
| PD5 | | TIMER0_B RKIN0 | TIMER20_ BRKIN1 | TIMER7_B RKIN0 | | USART1 _CK | | | | EVENTOUT |
| PD6 | | TIMER7_M CH3 | TIMER19_ CH0 | | | I2C1_SC L | CAN1_TX | | | EVENTOUT |
| PD7 | | TIMER7_C H3 | TIMER19_ CH1 | | | I2C1_SD A | CAN1_RX | | | EVENTOUT |
| PD8 | | | TIMER7_B RKIN0 | | USART1_R X | USART0 _CTS | | | | EVENTOUT |
| PD9 | | | TIMER0_B RKIN2 | | | USART1 _RTS ⁽²⁾ / USART1 _DE ⁽²⁾ | | | | EVENTOUT |
| PD10 | | | TIMER0_B RKIN1 | | SPI1_NSS/ I2S1_WS | USART1 _CTS | | | | EVENTOUT |
| PD11 | | TIMER0_M CH3 | TIMER20_ BRKIN0 ⁽⁴⁾ | | | I2C1_SM BA | | | | EVENTOUT |
| PD12 | | TIMER0_C H3 | TIMER20_ BRKIN0 | | | | | | | EVENTOUT |
| PD13 | | TIMER0_M CH2 | | | SPI1_NSS/ I2S1_WS | | | | | EVENTOUT |
| PD14 | | TIMER0_C H2 | | | SPI1_MOS I/I2S1_SD | | | | | EVENTOUT |
| PD15 | | TIMER0_M CH1 | | | SPI1_MIS O | | | | | EVENTOUT |

Table 2-11. Port E alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|--------------------|-------------------|-----|-----|---------------|--------------|-----|-----|----------|
| PE0 | | TIMER20_ BRKIN2 | TIMER7_B RKIN3 | | | USART2 _TX | MFCOM_D 7 | | | EVENTOUT |
| PE1 | | TIMER20_ BRKIN3 | | | | USART2 _RX | MFCOM_D 6 | | | EVENTOUT |

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|---------------------------|----------------|-----|----------------------|--------------------------|----------|--------------|-----|----------|
| PE2 | | | TIMER19_MCH3 | | | USART1_RTS/ USART1_DE | MFCOM_D3 | TRIGSEL_OUT7 | | EVENTOUT |
| PE3 | | | TIMER19_CH3 | | | USART1_CTS | MFCOM_D2 | TRIGSEL_OUT6 | | EVENTOUT |
| PE4 | | TIMER0_MCH1 | TIMER19_MCH0 | | SPI1_MISO | | MFCOM_D1 | TRIGSEL_OUT2 | | EVENTOUT |
| PE5 | | TIMER0_CH1 | TIMER19_CH0 | | SPI1_SCK/ I2S1_CK | | MFCOM_D0 | TRIGSEL_OUT1 | | EVENTOUT |
| PE6 | | TIMER1_CH0, TIMER1_ETI | TIMER19_MCH2 | | I2S1_MCK | | MFCOM_D5 | TRIGSEL_OUT5 | | EVENTOUT |
| PE7 | | TIMER7_MCH2 | TIMER19_BRKIN3 | | | | MFCOM_D0 | | | EVENTOUT |
| PE8 | | TIMER7_CH2 | TIMER19_BRKIN2 | | | | MFCOM_D1 | | | EVENTOUT |
| PE9 | | | TIMER7_BRKIN3 | | | | | | | EVENTOUT |
| PE10 | | | TIMER7_BRKIN2 | | | I2C1_SCL | | | | EVENTOUT |
| PE11 | | TIMER7_MCH1 | | | | I2C1_SDA | | TRIGSEL_IN8 | | EVENTOUT |
| PE12 | | TIMER7_CH1 | | | | I2C1_SMBA | | TRIGSEL_IN9 | | EVENTOUT |
| PE13 | | TIMER7_MCH0 | TIMER7_CH0 | | SPI0_MISO | | | TRIGSEL_IN2 | | EVENTOUT |
| PE14 | | TIMER7_CH0 | TIMER7_CH1 | | SPI0_SCK | | | TRIGSEL_IN3 | | EVENTOUT |
| PE15 | | TIMER20_MCH3 | TIMER19_MCH3 | | SPI0_IO2 | USART2_RTS/ USART2_DE | | | | EVENTOUT |

Table 2-12. Port F alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|-------------|----------|-----|-----|-----|---------|----------|-----|----------|
| PF0 | | TIMER19_CH1 | | | | | CAN0_RX | MFCOM_D6 | | EVENTOUT |
| PF1 | | TIMER0_B | TIMER19_ | | | | | | | EVENTOUT |



| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 |
|----------|-----|-------------------|--------------------|----------|---------------|----------------------------------|-----------------|-------------|-----|----------|
| | | RKIN1 | BRKIN1 | | | | | | | |
| PF2 | | TIMER0_B RKIN0 | TIMRE19_ BRKIN0 | | | USART2 _RTS/ USART2 _DE | TRIGSEL_I N6 | CMP_OU T | | EVENTOUT |
| PF3 | | | TIMER0_B RKIN3 | | | USART2 _TX | | | | EVENTOUT |
| PF4 | | | TIMER0_B RKIN2 | | | USART2 _RX | | | | EVENTOUT |
| PF5 | | TIMER0_M CH0 | | | SPI0_MIS O | USART1 _CTS ⁽²⁾ | | | | EVENTOUT |
| PF6 | | | | I2C0_SCL | | | | | | EVENTOUT |
| PF7 | | | | I2C0_SDA | | | | | | EVENTOUT |

Notes:

- (1) This function is controlled by SYSCFG_TIMERINSEL register.
- (2) Functions are available on GD32A503Vx/Rx/Cx devices only.
- (3) Functions are available on GD32A503Vx/Rx devices only.
- (4) Functions are available on GD32A503xC/xD/VB devices only.

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core

- Up to 100 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. Embedded memory

- Up to 384 Kbytes of Flash memory
- Max 4KB emulated EEPROM
- Extend Block: 64KB shared for data flash and EEPROM backup
- 4KB shared RAM for basic SRAM or EEPROM SRAM or fast program buffer
- ECC of on-chip Flash memory with single bit error corrected and double bit errors detected
- Up to 48 Kbytes of SRAM with ECC check

384 Kbytes of inner Flash and 48 Kbytes of inner SRAM at most is available for storing programs and data. 0~3 waiting time within Bank0/Bank1/Data Flash when CPU executes

instructions and data. [Table 2-2. GD32A503xx memory map](#) shows the memory map of the GD32A503xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 2 to 40 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.7 to 5.5 V application supply and I/Os

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 100 MHz/100 MHz/50 MHz. See [Figure 2-6. GD32A503xx clock tree](#) for details on the clock tree.

The Reset Control Unit (RCTL) controls three kinds of reset: system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the backup domain. Power-on reset (POR) and power-down reset (PDR) are always active. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security. The embedded over voltage detector (OVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.7 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} range: 2.7 to 5.5 V, external analog power supplies for ADC, DAC, reset blocks, RCs and PLL.
- V_{BAK} range: 2.7 to 5.5 V, power supply for RTC, external clock 32 kHz oscillator, backup registers and three pads, including PC13 to PC15.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory

by using USART0 (PA10 and PA11), LIN (PA3 and PA4), and CAN0 (PB13 and PB14).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In Deep-sleep mode, all clocks in the 1.1V domain are off, and all of IRC8M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, CAN0 wakeup, CAN1 wakeup, USART0 wakeup, USART1 wakeup, USART2 wakeup, CMP output and over voltage output. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In Standby mode, the whole 1.1V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pins.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{REF-} to V_{REF+}
- Temperature sensor

Two 12-bit 1 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between V_{REF-} and V_{REF+} . An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered by TRIGSEL, or by software. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to V_{REF+}/V_{REF-} pins. According to the different packages, V_{REF+} pin can be connected to V_{DDA} pin, or external reference voltage, V_{REF-} pin must be connected to V_{SSA} pin. The V_{REF+} pin is only available on no less than 64-pin packages, or else the V_{REF+} pin is not available and internally connected to V_{DDA} . The V_{REF-} pin is only available on no less than 100-pin packages, or else the V_{REF-} pin is not available and internally connected to V_{SSA} .

3.7. Digital to analog converter (DAC)

- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channel can be triggered by TRIGSEL or by software with DMA support. The maximum output value of the DAC is V_{REF+} .

3.8. Controller area network (CAN)

- Two CAN interfaces supports the CAN protocols version 2.0A and B, ISO11891-1:2015 and BOSCH CAN FD specification with baud rates up to 1 Mbit/s when classical frames and 8 Mbit/s when FD frames.
- Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0).
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- 32 mailboxes when configures with 8 bytes data length each, configurable as Rx or Tx mailbox.
- Receive public filter register for Rx mailboxes and receive public filter register for Rx FIFO.

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private filter register for up to 32 ID filter table elements.

3.9. Comparators (CMP)

- One fast rail-to-rail low-power comparator with software configurable
- Comparator has configurable analog input source

One Comparator (CMP) is implemented within the devices. It can work either standalone (all terminal are available on I/Os) or together with the timers. It could be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieves some current control by working together with a PWM output of a timer and the DAC. Its blanking function can be used for false overcurrent detection in motor control applications.

3.10. Direct memory access controller (DMA)

- 7 channels for DMA0 controller and 5 channels for DMA1 controller, and each channel are configurable
- Each channel is connected to flexible hardware DMA request.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to flexible hardware DMA requests. Each channel is dedicated to manage memory access requests from one or more peripherals. Transfer size of source and destination are independent and configurable.

3.11. DMA request multiplexer (DMAMUX)

- 12 channels for DMAMUX request multiplexer and 4 channels for DMAMUX request generator
- Support 27 trigger inputs
- Support 27 synchronization inputs

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

3.12. General-purpose inputs/outputs (GPIOs)

- Up to 88 fast GPIOs, all mappable on 16 external interrupt lines

- Analog input/output configurable
- Alternate function input/output configurable

There are up to 88 general purpose I/O pins (GPIO) in GD32A503xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, and PF0 ~ PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.13. Inter-integrated circuit (I2C)

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.14. Inter-IC sound (I2S)

- One I2S bus Interface with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32A503xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.15. Multi-function communication Interface (MFCOM)

- Programmable logic mode by integrating external digital logic function chip or combining

pin / shifter / timer function to produce complex output.

- USART, I2C, SPI, I2S, PWM waveform generation supported

The MFCOM is a highly configurable module provide emulation of a variety of serial communication protocols and flexible timers. Data can be signaled by timer, loaded, stored and compared between shifter and shiftbuf using DMA/Polling/Interrupt method. Program trigger, pin or shifter flag for the timer to produce shift clock that transfers data and generate specific events.

3.16. Real time clock (RTC)

- 32-bit programmable counter with a programmable 20-bit prescaler
- Alarm function

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock of HXTAL clock divided by 128, or LXTAL oscillator clock, or IRC40K oscillator clock.

3.17. Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 22.5 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI1)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI1.

3.18. Trigger selection controller (TRIGSEL)

- Trigger input source could be external input signal or output of peripheral
- Trigger selection output could be for external output or peripheral
- Supports different optional trigger inputs

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. With TRIGSEL, there are up to 4 trigger selection outputs could be selected for each peripheral. And every output could select from different trigger input signal.

3.19. Timers and PWM generation

- Four 16-bit advanced timer (TIMER0, TIMER7, TIMER19, TIMER20), one 16-bit general timer (TIMER1), and two 16-bit basic timer (TIMER5, TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0, TIMER7, TIMER19, TIMER20) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMER1. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32A503xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep, and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.20. Universal synchronous asynchronous receiver transmitter (USART)

- Maximum speed up to 12.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.21. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.22. Package and operation temperature

- LQFP100(GD32A503Vx), LQFP64 (GD32A503Rx), LQFP48(GD32A503Cx) and QFN32(GD32A503Kx).
- Operation temperature range: -40°C to +125°C (automotive level).

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings^{(1) (4)}

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|---|------------------------|------------------------|------|
| V _{DD} | External voltage range ⁽²⁾ | V _{SS} - 0.3 | V _{SS} + 5.5 | V |
| V _{DDA} | External analog supply voltage | V _{SSA} - 0.3 | V _{SSA} + 5.5 | V |
| V _{IN} | Input voltage on all I/O pins ⁽³⁾ | V _{SS} - 0.3 | V _{DD} + 0.3 | V |
| ΔV _{DDX} | Variations between different V _{DD} power pins | — | 50 | mV |
| V _{SSX} - V _{SS} | Variations between different ground pins | — | 50 | mV |
| T _A | Operating temperature range | -40 | +125 | °C |
| P _D | Power dissipation at T _A = 125°C of LQFP100 | — | 441 | mW |
| | Power dissipation at T _A = 125°C of LQFP64 | — | TBD | |
| | Power dissipation at T _A = 125°C of LQFP48 | — | TBD | |
| | Power dissipation at T _A = 125°C of QFN32 | — | TBD | |
| T _{STG} | Storage temperature range | -65 | +150 | °C |
| T _J | Maximum junction temperature | — | 150 | °C |

- (1) Guaranteed by design, not tested in production.
- (2) All main power and ground pins should be connected to an external power source within the allowable range.
- (3) V_{IN} maximum value cannot exceed 5.5 V.
- (4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

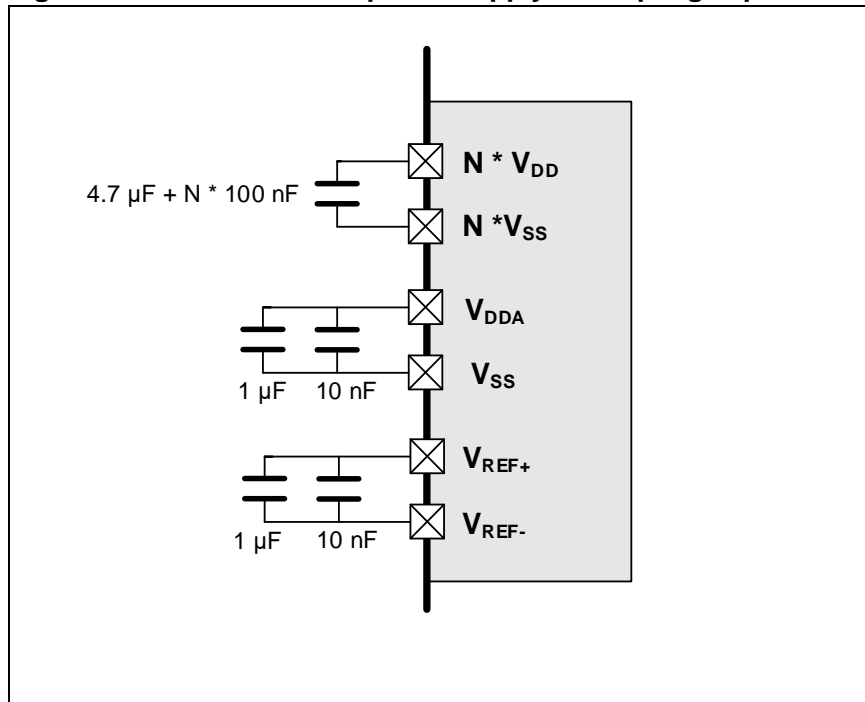
4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|--------------------------------|-----------------------|-------------------------|--------------------|-----|--------------------|------|
| V _{DD} ⁽²⁾ | Supply voltage | — | 2.7 | 5.0 | 5.5 | V |
| V _{DDA} | Analog supply voltage | Same as V _{DD} | 2.7 | 5.0 | 5.5 | V |

- (1) Guaranteed by design, not tested in production.
- (2) If the voltage is below 3V, the flash erasing may be interrupted and FMC_STAT0->RSTERR=1.

Figure 4-1. Recommended power supply decoupling capacitors⁽¹⁾⁽²⁾



- (1) The V_{REF+} and V_{REF-} pins are only available on 100-pin package, or else the V_{REF+}/V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.
- (2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|----------------------|------------|-----|-----|------|
| f_{HCLK} | AHB clock frequency | — | — | 100 | MHz |
| f_{APB1} | APB1 clock frequency | — | — | 50 | MHz |
| f_{APB2} | APB2 clock frequency | — | — | 100 | MHz |

- (1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | — | 0 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | | 100 | ∞ | |

- (1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------------|---------------|--|-----|---------------|
| $t_{\text{start-up}}$ | Start-up time | Clock source from HXTAL (HXTALSCAL off) | 5.2 | ms |
| | | Clock source from HXTAL (HXTALSCAL on) | 2.1 | ms |
| | | Clock source from IRC8M | 105 | μs |

- (1) Based on characterization, not tested in production.
- (2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.
- (3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics⁽¹⁾⁽²⁾

| Symbol | Parameter | Typ | Unit |
|-------------------------------|---|-----|---------------|
| t_{Sleep} | Wakeup from Sleep mode | 1.3 | μs |
| $t_{\text{Deep-sleep}}^{(3)}$ | Wakeup from Deep-sleep mode (LDO in normal power mode and normal driver mode) | 2.3 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode and normal driver mode) | 2.3 | |
| | Wakeup from Deep-sleep mode (LDO in normal power mode and low driver mode) | 2.3 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode and low driver mode) | 2.3 | |
| t_{Standby} | Wakeup from Standby mode | 110 | |

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, IRC8M = System clock = 8 MHz.

(3) DSLPVS[1:0] bit in Register RCU_DSV is 0x11.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics⁽²⁾⁽³⁾⁽⁴⁾

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------------------------------|---------------------------|---|-----|--------------------|-----|------|
| $I_{\text{DD}}+I_{\text{DDA}}$ | Supply current (Run mode) | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 100 MHz, All peripherals enabled | — | 24.6 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 100 MHz, All peripherals disabled | — | 11.9 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled | — | 18.5 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled | — | 9.3 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals enabled | — | 15 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 64 MHz, All peripherals disabled | — | 6.7 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled | — | 11.6 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled | — | 5.4 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 32 MHz, All peripherals enabled | — | 8.3 | — | mA |
| | | $V_{\text{DD}} = V_{\text{DDA}} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 32 MHz, All peripherals disabled | — | 4.2 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------|--------------------------------|--|-----|--------------------|-----|------|
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled | — | 6.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled | — | 3.5 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled | — | 5 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled | — | 2.9 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled | — | 3.3 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled | — | 2.2 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals enabled | — | 2.5 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 4 MHz, All peripherals disabled | — | 1.9 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 2 MHz, All peripherals enabled | — | 2 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 2 MHz, All peripherals disabled | — | 1.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 1 MHz, All peripherals enabled | — | 1.8 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 1 MHz, All peripherals disabled | — | 1.6 | — | mA |
| | Supply current (Sleep mode) | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 100 MHz, CPU clock off, All peripherals enabled | — | 19.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 100 MHz, CPU clock off, All peripherals disabled | — | 6.1 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals enabled | — | 14.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals disabled | — | 4.8 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 64 MHz, CPU clock off, All peripherals enabled | — | 13.3 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 64 MHz, CPU clock off, All peripherals disabled | — | 4.5 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------|-----------|---|-----|--------------------|-----|------|
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals enabled | — | 10.3 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals disabled | — | 3.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 32 MHz, CPU clock off, All peripherals enabled | — | 7.5 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 32 MHz, CPU clock off, All peripherals disabled | — | 3 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals enabled | — | 6 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals disabled | — | 2.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled | — | 4.6 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled | — | 2.3 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled | — | 3.1 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled | — | 2 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 4 MHz, CPU clock off, All peripherals enabled | — | 2.4 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 4 MHz, CPU clock off, All peripherals disabled | — | 1.7 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 2 MHz, CPU clock off, All peripherals enabled | — | 2 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 2 MHz, CPU clock off, All peripherals disabled | — | 1.6 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--|----------------------------------|--|------|--------------------|-----|------|
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 1 MHz, CPU clock off, All peripherals enabled | — | 1.8 | — | mA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, HXTAL = 8 MHz, System clock = 1 MHz, CPU clock off, All peripherals disabled | — | 1.58 | — | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD} = V_{DDA} = 5\text{ V}$, LDO in normal power and normal driver mode, IRC40K off, RTC off, All GPIOs analog mode, SRAM1 and SRAM2 on, $V_{core} = 1.1\text{V}$ | — | 160.79 | — | uA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, LDO in low power and normal driver mode, RTC off, All GPIOs analog mode, SRAM1 and SRAM2 on, $V_{core} = 1.1\text{V}$ | — | 134.79 | — | uA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, LDO in normal power and low driver mode, IRC40K off, RTC off, All GPIOs analog mode, SRAM1 and SRAM2 on, $V_{core} = 1.1\text{V}$ | — | 107.79 | — | uA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, LDO in low power and low driver mode, IRC40K off, RTC off, All GPIOs analog mode, SRAM1 and SRAM2 on, $V_{core} = 1.1\text{V}$ | — | 81.46 | — | uA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, LDO in low power and low driver mode, IRC40K off, RTC off, All GPIOs analog mode, SRAM1 and SRAM2 off, $V_{core} = 0.8\text{V}$ | — | 39.79 | — | uA |
| | Supply current (Standby mode) | $V_{DD} = V_{DDA} = 5\text{ V}$, IRC40K on, RTC on, BOR on | — | 8.59 | — | μA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, IRC40K on, RTC off, BOR on | — | 7.65 | — | μA |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, IRC40K off, RTC off, BOR on | — | 6.11 | — | μA |
| $V_{DD} = V_{DDA} = 5\text{ V}$, IRC40K off, RTC off, BOR off | | — | 2.31 | — | μA | |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for $T_A = 25\text{ }^\circ\text{C}$ and test result is mean value.

(3) Run mode and sleep mode use WS_WSCNT_3 and PLL on.

(4) When analog peripheral blocks such as ADCs, DACs, HXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

Figure 4-2. Typical supply current consumption in Run mode

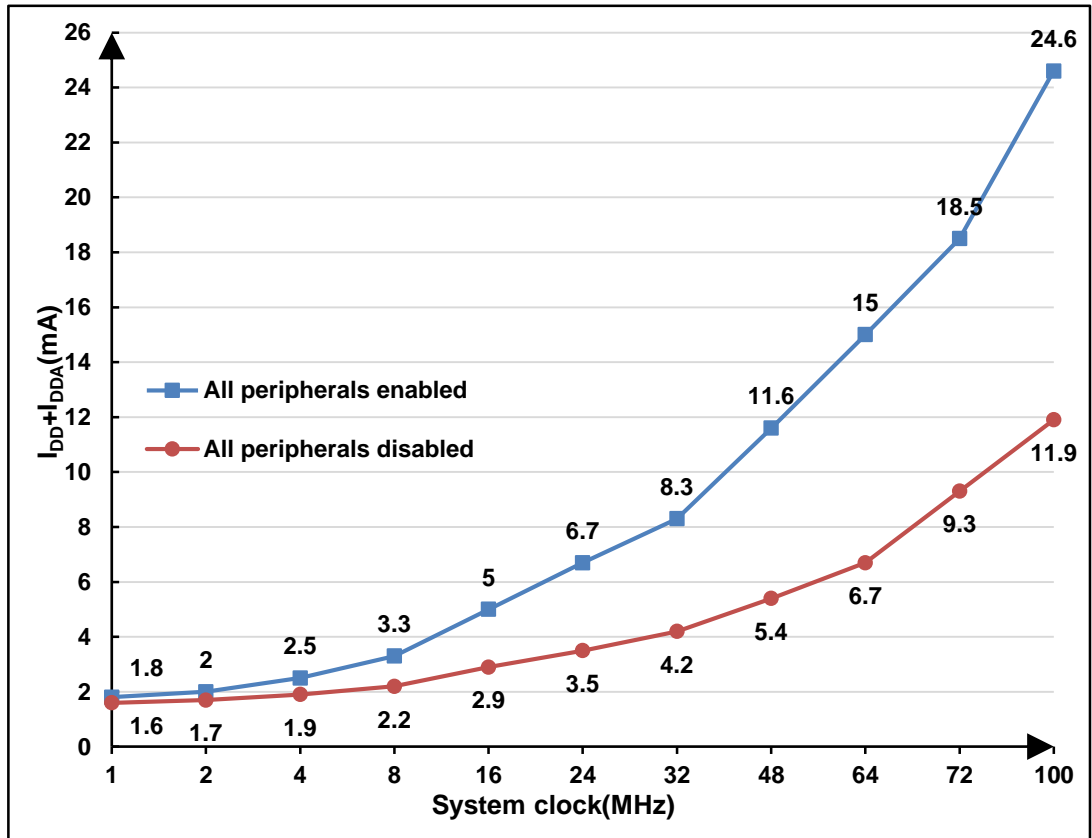
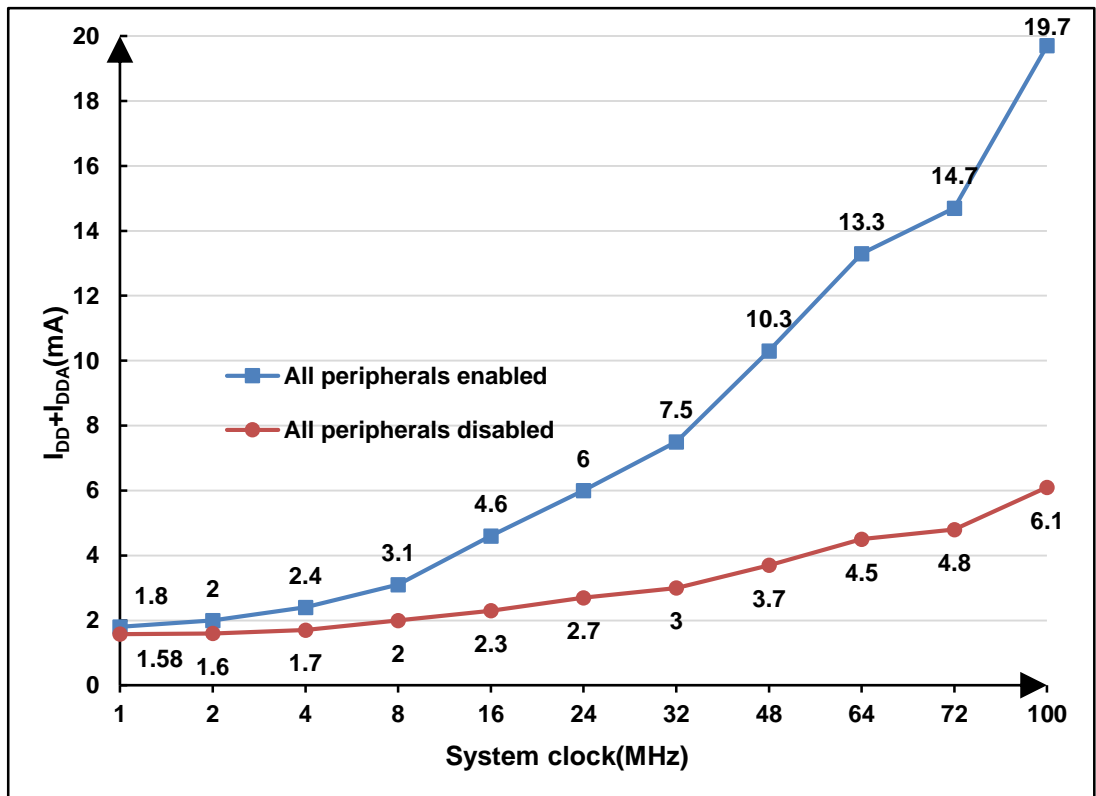


Figure 4-3. Typical supply current consumption in Sleep mode



4.4. EMC characteristics

EMI (Electromagnetic Interference) emission test result is given in the [Table 4-8. EMI characteristics](#). The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-8. EMI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Tested frequency band | Max vs. | Unit |
|------------------|------------|--|-----------------------|--|------|
| | | | | [f _{HXTAL} /f _{HCLK}] | |
| | | | | 8/100 MHz | |
| S _{EMI} | Peak level | V _{DD} = 5.5 V, T _A = +25 °C, LQFP100, f _{HCLK} = 100 MHz, conforms to SAE J1752-3:2017 | 0.15 MHz to 30 MHz | -8.45 | dBμV |
| | | | 30 MHz to 130 MHz | 10.34 | |
| | | | 130 MHz to 1 GHz | 28.86 | |
| | | V _{DD} = 5.5 V, T _A = +25 °C, LQFP64, f _{HCLK} = 100 MHz, conforms to SAE J1752-3:2017 | 0.15 MHz to 30 MHz | -7.31 | |
| | | | 30 MHz to 130 MHz | 12.49 | |
| | | | 130 MHz to 1 GHz | 17.78 | |

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|--------------------------------------|-------------------------------|-----|------|-----|------|
| V _{LVD} ⁽¹⁾ | Low voltage Detector level selection | LVDT<2:0> = 000(rising edge) | — | 2.94 | — | V |
| | | LVDT<2:0> = 000(falling edge) | — | 2.84 | — | |
| | | LVDT<2:0> = 001(rising edge) | — | 3.16 | — | |
| | | LVDT<2:0> = 001(falling edge) | — | 3.03 | — | |
| | | LVDT<2:0> = 010(rising edge) | — | 3.36 | — | |
| | | LVDT<2:0> = 010(falling edge) | — | 3.24 | — | |
| | | LVDT<2:0> = 011(rising edge) | — | 3.56 | — | |
| | | LVDT<2:0> = 011(falling edge) | — | 3.44 | — | |
| | | LVDT<2:0> = 100(rising edge) | — | 4.07 | — | |
| | | LVDT<2:0> = 100(falling edge) | — | 3.95 | — | |
| | | LVDT<2:0> = 101(rising edge) | — | 4.27 | — | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|----------------------------|-------------------------------|-----|-------|-----|------|
| | | LVDT<2:0> = 101(falling edge) | — | 4.15 | — | |
| | | LVDT<2:0> = 110(rising edge) | — | 4.47 | — | |
| | | LVDT<2:0> = 110(falling edge) | — | 4.35 | — | |
| | | LVDT<2:0> = 111(rising edge) | — | 4.68 | — | |
| | | LVDT<2:0> = 111(falling edge) | — | 4.56 | — | |
| V _{LVDhyst} ⁽²⁾ | LVD hysteresis | — | — | 100 | — | mV |
| V _{POR} ⁽¹⁾ | Power on reset threshold | — | — | 2.13 | — | V |
| V _{PDR} ⁽¹⁾ | Power down reset threshold | — | — | 2.08 | — | V |
| V _{PDRhyst} ⁽¹⁾ | PDR hysteresis | — | — | 50 | — | mV |
| t _{RSTTEMPO} ⁽¹⁾ | Reset temporization | — | — | 460 | — | us |
| V _{OVD} ⁽¹⁾ | OVD threshold (OVDT=1) | Falling edge | — | 5.697 | — | V |
| | | Rising edge | — | 5.714 | — | V |
| V _{OVDhyst} ⁽¹⁾ | OVD hysteresis (OVDT=1) | — | — | 17 | — | mV |
| V _{OVD} ⁽¹⁾ | OVD threshold (OVDT=0) | Falling edge | — | 5.170 | — | V |
| | | Rising edge | — | 5.188 | — | V |
| V _{OVDhyst} ⁽¹⁾ | OVD hysteresis (OVDT=0) | — | — | 18 | — | mV |
| V _{BOR} ⁽¹⁾⁽³⁾ | Brownout threshold | Falling edge | — | 2.53 | — | V |
| | | Rising edge | — | 2.569 | — | V |
| V _{BORhyst} ⁽¹⁾ | BOR hysteresis | — | — | 39 | — | mV |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) BOR is not available when V_{DD} is lower than 3V.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD and static latch-up characteristics^{(1) (2) (3)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|---|--|-----|-----|------|------|
| $V_{ESD(HBM)}$ ⁽⁴⁾ | Electrostatic discharge voltage (human body model) | $T_A = 25\text{ }^\circ\text{C}$, LQFP100, Zap 3 pulse, Zap Interval = 500 ms | — | — | 4000 | V |
| $V_{ESD(CDM)}$ ⁽⁵⁾ | Electrostatic discharge voltage (charge device model) | All pins except the corner pins | — | — | 500 | V |
| | | Corner pins only | | | | |
| LU ⁽⁶⁾ | I-test | $T_A = 125\text{ }^\circ\text{C}$, LQFP100 | — | — | 200 | mA |
| | V_{supply} over voltage | | — | — | 8.25 | V |

- (1) All ESD testing are in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
- (2) Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature".
- (3) Based on characterization, not tested in production.
- (4) This parameter is tested in conformity with AEC-Q100-002E.
- (5) This parameter is tested in conformity with AEC-Q100-011D.
- (6) This parameter is tested in conformity with AEC-Q100-004D.

4.7. External clock characteristics

Table 4-11. High speed external clock (HXTAL) generated from a crystal / ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|--|-----|------|-----|------------|
| f_{HXTAL} ⁽¹⁾ | Crystal or ceramic frequency | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2 | 8 | 40 | MHz |
| R_F ⁽²⁾ | Feedback resistor | $V_{DD} = 5\text{ V}$ | — | 400 | — | k Ω |
| C_{HXTAL} ⁽²⁾⁽³⁾ | Recommended matching capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| Ducy _(HXTAL) ⁽²⁾ | Crystal or ceramic duty cycle | — | 30 | 50 | 70 | % |
| g_m ⁽²⁾ | Oscillator transconductance | Startup, RCU_CTL_HXTALSC AL=0 | — | 4 | — | mA/V |
| | | Startup, RCU_CTL_HXTALSC AL=1 | — | 29 | — | |
| $I_{DDHXTAL}$ ⁽¹⁾ | Crystal or ceramic operating current | $V_{DD} = 5\text{ V}$, HXTAL SCAL off | — | 0.46 | — | mA |
| $t_{SUHXTAL}$ ⁽¹⁾ | Crystal or ceramic startup time | $V_{DD} = 5\text{ V}$, HXTAL SCAL off | — | 5.1 | — | ms |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, for C_{HXTAL1} and C_{HXTAL2} , it is recommended matching capacitance on OSCIN

and OSCOUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S , it is PCB and MCU pin stray capacitance.

Table 4-12. High speed external clock characteristics (HXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|--|--------------|-----|--------------|------|
| $f_{HXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | — | 50 | MHz |
| $V_{HXTALH}^{(2)}$ | OSCIN input pin high level voltage | $V_{DD} = 5\text{ V}$ | $0.7 V_{DD}$ | — | V_{DD} | V |
| $V_{HXTALL}^{(2)}$ | OSCIN input pin low level voltage | | V_{SS} | — | $0.3 V_{DD}$ | V |
| $t_{H/L(HXTAL)}^{(2)}$ | OSCIN high or low time | — | 5 | — | — | ns |
| $t_{R/F(HXTAL)}^{(2)}$ | OSCIN rise or fall time | — | — | — | 10 | ns |
| $C_{IN}^{(2)}$ | OSCIN input capacitance | — | — | 5 | — | pF |
| $Ducy_{(HXTAL)}^{(2)}$ | Duty cycle | — | 30 | — | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-13. Low speed external user clock characteristics (LXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|--|--------------|-----|--------------|------|
| $f_{HXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | — | — | 1000 | kHz |
| $V_{HXTALH}^{(2)}$ | OSC32IN input pin high level voltage | $V_{DD} = 5\text{ V}$ | $0.7 V_{DD}$ | — | V_{DD} | V |
| $V_{HXTALL}^{(2)}$ | OSC32IN input pin low level voltage | | V_{SS} | — | $0.3 V_{DD}$ | V |
| $t_{H/L(HXTAL)}^{(2)}$ | OSC32IN high or low time | — | 450 | — | — | ns |
| $t_{R/F(HXTAL)}^{(2)}$ | OSC32IN rise or fall time | — | — | — | 50 | ns |
| $C_{IN}^{(2)}$ | OSC32IN input capacitance | — | — | 5 | — | pF |
| $Ducy_{(HXTAL)}^{(2)}$ | Duty cycle | — | 30 | — | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-14. High speed internal clock (IRC8M) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|--|-------|-----|-------|------|
| f_{IRC8M} | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 8 | — | MHz |
| ACC_{IRC8M} | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD} = V_{DDA} = 5\text{ V}$, $T_A = -40\text{ °C} \sim +125\text{ °C}$ | -3.75 | — | +3.75 | % |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, $T_A = 25\text{ °C}$ | -1.0 | — | +1.0 | % |
| | IRC8M oscillator Frequency accuracy, User trimming step ⁽²⁾ | — | — | 0.5 | — | % |
| $DUCY_{IRC8M}^{(2)}$ | IRC8M oscillator duty cycle | $V_{DD} = V_{DDA} = 5\text{ V}$ | 45 | 50 | 55 | % |
| $I_{DDAIRC8M}^{(1)}$ | IRC8M oscillator operating current | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 107 | — | uA |
| $t_{SUIRC8M}^{(1)}$ | IRC8M oscillator startup time | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 1.3 | — | us |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed internal clock (IRC40K) characteristics

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|-----------------|--|--|-----|--------------------|-----|------|
| f_{IRC40K} | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD} = V_{DDA} = 5\text{ V}$, $T_A = -40\text{ °C} \sim +125\text{ °C}$ | 38 | — | 44 | kHz |
| | | $V_{DD} = V_{DDA} = 5\text{ V}$, $T_A = 25\text{ °C}$ | 38 | — | 44 | |
| $I_{DDAIRC40K}$ | IRC40K oscillator operating current | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 0.8 | — | μA |
| $t_{SUIRC40K}$ | IRC40K oscillator startup time | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 19 | — | μs |

(1) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-16. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------------|------------|-----|-----|-----|------|
| $f_{PLLIN}^{(1)}$ | PLL input clock frequency | — | 2 | — | 16 | MHz |
| $f_{PLLOUT}^{(2)}$ | PLL output clock frequency | — | 16 | — | 100 | MHz |
| $f_{VCO}^{(2)}$ | PLL VCO output clock frequency | — | 32 | — | 200 | MHz |
| $t_{LOCK}^{(2)}$ | PLL lock time | — | — | — | 300 | μs |

| | | | | | | |
|---------------------------|--|--------------------|---|------|---|----|
| I _{DDA} (1)(3) | Current consumption on V _{DD} | VCO freq = 200 MHz | — | 1100 | — | μA |
| | Current consumption on V _{D_{DA}} | | — | 620 | — | |
| Jitter _{PLL} (4) | Cycle to cycle Jitter(rms) | System clock | — | 40 | — | ps |
| | Cycle to cycle Jitter (peak to peak) | | — | 400 | — | |

- (1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 100 MHz.
(4) Value given with main PLL running.

4.10. Memory characteristics

Table 4-17. Flash memory characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|---------------------------|---|----------------------------------|--------------------|--------------------|--------------------|---------|
| PE _{CYC} | Number of guaranteed program /erase cycles before failure (Endurance) | — | 100 | — | — | kcycles |
| t _{RET} | Data retention time | — | 20 | — | — | years |
| t _{PROG} | Double-Word programming time | T _A = -40°C ~ +125 °C | — | 45 | — | μs |
| t _{ERASE} | Sector erase time | T _A = -40°C ~ +125 °C | 1 | — | 20 | ms |
| t _{MERASE(256K)} | Mass erase time | T _A = -40°C ~ +125 °C | — | 18.06 | — | ms |
| t _{MERASE(384B)} | Mass erase time | T _A = -40°C ~ +125 °C | 146 | — | 2578 | ms |

- (1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

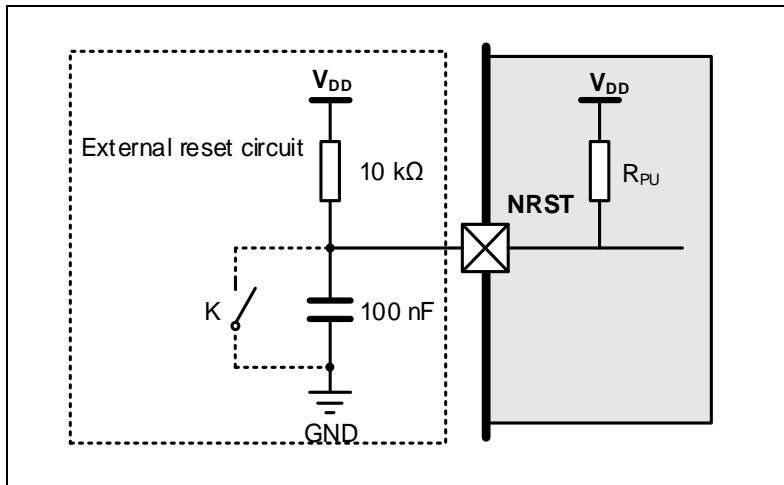
4.11. NRST pin characteristics

Table 4-18. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|------------------------------------|---|----------------------|-----|-----------------------|------|
| V _{IL(NRST)} (1) | NRST Input low level voltage | V _{DD} = V _{D_{DA}} = 2.7 V | -0.3 | — | 0.35 V _{DD} | V |
| V _{IH(NRST)} (1) | NRST Input high level voltage | | 0.65 V _{DD} | — | V _{DD} + 0.3 | |
| V _{hyst} (1) | Schmidt trigger Voltage hysteresis | | — | 380 | — | |
| V _{IL(NRST)} (1) | NRST Input low level voltage | V _{DD} = V _{D_{DA}} = 5 V | -0.3 | — | 0.35 V _{DD} | V |
| V _{IH(NRST)} (1) | NRST Input high level voltage | | 0.65 V _{DD} | — | V _{DD} + 0.3 | |
| V _{hyst} (1) | Schmidt trigger Voltage hysteresis | | — | 570 | — | |
| V _{IL(NRST)} (1) | NRST Input low level voltage | V _{DD} = V _{D_{DA}} = 5.5 V | -0.3 | — | 0.35 V _{DD} | V |
| V _{IH(NRST)} (1) | NRST Input high level voltage | | 0.65 V _{DD} | — | V _{DD} + 0.3 | |
| V _{hyst} (1) | Schmidt trigger Voltage hysteresis | | — | 610 | — | |
| R _{pu} (2) | Pull-up equivalent resistor | — | — | 40 | — | kΩ |

- (1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit⁽¹⁾



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12. GPIO characteristics

Table 4-19. I/O port DC characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|--|--------------|------|--------------|------|
| V_{IL} | All IO Pins level input voltage | $2.7\text{ V} \leq V_{DD} = V_{DDA} \leq 5.5\text{ V}$ | — | — | $0.3 V_{DD}$ | V |
| V_{IH} | All IO Pins High level input voltage | $2.7\text{ V} \leq V_{DD} = V_{DDA} \leq 5.5\text{ V}$ | $0.7 V_{DD}$ | — | — | |
| IO_speed=50MHz | | | | | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +8\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 0.16 | — | V |
| | | $V_{DD} = 5\text{ V}$ | — | 0.10 | — | |
| | | $V_{DD} = 5.5\text{ V}$ | — | 0.09 | — | |
| | Low level output voltage for an IO Pin ($I_{IO} = +20\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 0.44 | — | |
| | | $V_{DD} = 5\text{ V}$ | — | 0.25 | — | |
| | | $V_{DD} = 5.5\text{ V}$ | — | 0.24 | — | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +8\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 2.51 | — | |
| | | $V_{DD} = 5\text{ V}$ | — | 4.87 | — | |
| | | $V_{DD} = 5.5\text{ V}$ | — | 5.37 | — | |
| | High level output voltage for an IO Pin ($I_{IO} = +20\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 2.16 | — | |
| | | $V_{DD} = 5\text{ V}$ | — | 4.67 | — | |
| | | $V_{DD} = 5.5\text{ V}$ | — | 5.19 | — | |
| IO_speed=10MHz | | | | | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +8\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 0.26 | — | V |
| | | $V_{DD} = 5\text{ V}$ | — | 0.18 | — | |
| | | $V_{DD} = 5.5\text{ V}$ | — | 0.17 | — | |
| | ($I_{IO} = +12\text{ mA}$) | $V_{DD} = 2.7\text{ V}$ | — | 0.69 | — | |
| | Low level output | $V_{DD} = 5\text{ V}$ | — | 0.60 | — | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|----------------|---|--------------------------|-----|------|-----|------------|--|
| | voltage for an IO Pin ($I_{IO} = +20 \text{ mA}$) | $V_{DD} = 5.5 \text{ V}$ | — | 0.56 | — | V | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +8 \text{ mA}$) | $V_{DD} = 2.7 \text{ V}$ | — | 2.38 | — | | |
| | | $V_{DD} = 5 \text{ V}$ | — | 4.79 | — | | |
| | (High level output voltage for an IO Pin ($I_{IO} = +12 \text{ mA}$)) | $V_{DD} = 5.5 \text{ V}$ | — | 5.30 | — | | |
| | | $V_{DD} = 2.7 \text{ V}$ | — | 1.86 | — | | |
| | (High level output voltage for an IO Pin ($I_{IO} = +20 \text{ mA}$)) | $V_{DD} = 5 \text{ V}$ | — | 4.23 | — | | |
| | | $V_{DD} = 5.5 \text{ V}$ | — | 4.78 | — | | |
| IO_speed=2MHz | | | | | | | |
| V_O | Low level output voltage for an IO Pin ($I_{IO} = +1 \text{ mA}$) | $V_{DD} = 2.7 \text{ V}$ | — | 0.12 | — | | |
| | | $V_{DD} = 5 \text{ V}$ | | 0.07 | | | |
| | | $V_{DD} = 5.5 \text{ V}$ | | 0.06 | | | |
| | Low level output voltage for an IO Pin ($I_{IO} = +4 \text{ mA}$) | $V_{DD} = 2.7 \text{ V}$ | — | 0.52 | — | | |
| | | $V_{DD} = 5 \text{ V}$ | | 0.27 | | | |
| | | $V_{DD} = 5.5 \text{ V}$ | — | 0.26 | — | | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +1 \text{ mA}$) | $V_{DD} = 2.7 \text{ V}$ | — | 2.50 | — | | |
| | | $V_{DD} = 5 \text{ V}$ | | 4.87 | | | |
| | | $V_{DD} = 5.5 \text{ V}$ | | 5.38 | | | |
| | High level output voltage for an IO Pin ($I_{IO} = +4 \text{ mA}$) | $V_{DD} = 2.7 \text{ V}$ | — | 1.69 | — | | |
| | | $V_{DD} = 5 \text{ V}$ | | 4.50 | | | |
| | | $V_{DD} = 5.5 \text{ V}$ | — | 5.02 | — | | |
| $R_{PU}^{(2)}$ | Internal pull-up resistor | — | — | 40 | — | k Ω | |
| $R_{PD}^{(2)}$ | Internal pull-down resistor | — | — | 40 | — | k Ω | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-20. I/O port AC characteristics⁽¹⁾⁽²⁾⁽⁴⁾

| GPIOx_OSPD[1:0] bit value ⁽³⁾ | Parameter | Conditions | Typ | Unit |
|--|---------------------|---|------|------|
| GPIOx_OSPD->OSPDy[1:0] = X0 (IO_Speed = 2 MHz) | T_{Rise}/T_{Fall} | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 10 \text{ pF}$ | 50.4 | ns |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 30 \text{ pF}$ | 61.2 | |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 50 \text{ pF}$ | 71.2 | |
| GPIOx_OSPD->OSPDy[1:0] = 01 (IO_Speed = 10 MHz) | T_{Rise}/T_{Fall} | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 10 \text{ pF}$ | 11.6 | ns |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 30 \text{ pF}$ | 14.8 | |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 50 \text{ pF}$ | 16.4 | |
| GPIOx_OSPD->OSPDy[1:0] = 11 (IO_Speed = 50 MHz) | T_{Rise}/T_{Fall} | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 10 \text{ pF}$ | 2.8 | ns |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 30 \text{ pF}$ | 3.6 | |
| | | $2.7 \leq V_{DD} \leq 5.5 \text{ V}, C_L = 50 \text{ pF}$ | 4.4 | |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for $T_A = 25 \text{ }^\circ\text{C}$.

(3) The I/O speed is configured using the GPIOx_OSPD -> OSPDy[1:0] bits.

(4) Only for reference, Depending on user's design.

4.13. ADC characteristics

Table 4-21. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|---|---|-------|------------------|-------------------|--------------------|
| V _{DDA} ⁽¹⁾ | Operating voltage | — | 2.7 | 5.0 | 5.5 | V |
| V _{REF+} ⁽²⁾ | Positive Reference Voltage | — | 2.7 | 5.0 | V _{DDA} | V |
| V _{REF-} ⁽²⁾ | Negative Reference Voltage | — | — | V _{SSA} | — | V |
| V _{IN} ⁽¹⁾ | ADC input voltage range | — | 0 | — | V _{REF+} | V |
| f _{ADC} ⁽¹⁾ | ADC clock | — | 0.1 | — | 15 | MHz |
| f _S ⁽¹⁾ | Sampling rate | 12-bit | 0.007 | — | 1 | MSPs |
| | | 10-bit | 0.008 | — | 1.15 | |
| | | 8-bit | 0.009 | — | 1.36 | |
| | | 6-bit | 0.011 | — | 1.67 | |
| V _{AIN} ⁽¹⁾ | Analog input voltage | 32 external, 2 internal | 0 | — | V _{REF+} | V |
| R _{AIN} ⁽²⁾ | External input impedance | See Equation 1 | — | — | 823 | kΩ |
| R _{ADC} ⁽²⁾ | Input sampling switch resistance | — | — | — | 500 | Ω |
| C _{ADC} ⁽²⁾ | Input sampling capacitance | No pin/pad capacitance included | — | — | 9 | pF |
| t _S ⁽²⁾ | Sampling time | f _{ADC} = 15 MHz | 0.17 | — | 32 | μs |
| | | | 2.5 | — | 479.5 | 1/f _{ADC} |
| t _{CONV} ⁽²⁾ | Total conversion time (including sampling time) | 12-bit | — | 15 | — | 1/f _{ADC} |
| | | 10-bit | — | 13 | — | |
| | | 8-bit | — | 11 | — | |
| | | 6-bit | — | 9 | — | |
| t _{SU} ⁽²⁾ | Startup time | — | — | — | 1 | μs |
| I _{VDDA} ⁽¹⁾ | ADC consumption from the V _{DDA} supply | f _{ADC} = 15 MHz, V _{DDA} = V _{REF+} = 5 V | — | 1 | — | mA |
| I _{VDD} ⁽¹⁾ | ADC consumption from the V _{DD} supply | f _{ADC} = 15 MHz, V _{DDA} = V _{REF+} = 5 V | — | 0.8 | — | mA |
| I _{VREF+} ⁽¹⁾ | ADC consumption from the V _{REF+} supply | f _{ADC} = 15 MHz, V _{DDA} = V _{REF+} = 5 V | — | 0.1 | — | mA |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula
$$R_{AIN} < \frac{T_s}{f_{ADC} \cdot C_{ADC} \cdot \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-22. ADC RAIN max for f_{ADC} = 15 MHz⁽²⁾

| T _s (cycles) | t _S (us) | R _{AIN} max (KΩ) |
|-------------------------|---------------------|---------------------------|
| 2.5 | 0.17 | 1.4 |

| T_s (cycles) | t_s (us) | $R_{AIN\ max}$ (K Ω) |
|----------------|------------|------------------------------|
| 14.5 | 0.97 | 10.5 |
| 27.5 | 1.83 | 20.5 |
| 55.5 | 3.7 | 41.8 |
| 83.5 | 5.57 | 63.2 |
| 111.5 | 7.43 | 84.6 |
| 143.5 | 9.57 | 109 |
| 479.5 | 31.97 | 365.5 |

- (1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-23. ADC dynamic accuracy at $f_{ADC} = 15\text{ MHz}^{(1)}$

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--------|--------------------------------------|--|-----|-------|-----|------|
| ENOB | Effective number of bits | $f_{ADC} = 15\text{ MHz}$ | — | 11.1 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA} = V_{REF+} = 5.0\text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C | — | 68.6 | — | dB |
| SNR | Signal-to-noise ratio | | — | 71.27 | — | |
| THD | Total harmonic distortion | | — | -81.1 | — | |

- (1) Based on characterization, not tested in production.

Table 4-24. ADC dynamic accuracy at $f_{ADC} = 15\text{ MHz}^{(1)}$

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--------|--------------------------------------|--|-----|-------|-----|------|
| ENOB | Effective number of bits | $f_{ADC} = 15\text{ MHz}$ | — | 10.8 | — | bits |
| SNDR | Signal-to-noise and distortion ratio | $V_{DDA} = V_{REF+} = 2.7\text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C | — | 66.8 | — | dB |
| SNR | Signal-to-noise ratio | | — | 67.2 | — | |
| THD | Total harmonic distortion | | — | -79.1 | — | |

- (1) Based on characterization, not tested in production.

Table 4-25. ADC static accuracy at $f_{ADC} = 15\text{ MHz}^{(1)}$

| Symbol | Parameter | Test conditions | Typ | Max | Unit |
|--------|------------------------------|---|---------|-----|------|
| Offset | Offset error | $f_{ADC} = 15\text{ MHz}$ $V_{DDA} = V_{REF+} = 5.0\text{ V}$ Temperature = 25 °C | ± 3 | — | LSB |
| DNL | Differential linearity error | | ± 3 | — | |
| INL | Integral linearity error | | ± 5 | — | |

- (1) Based on characterization, not tested in production.

Table 4-26. ADC static accuracy at $f_{ADC} = 15\text{ MHz}^{(1)}$

| Symbol | Parameter | Test conditions | Typ | Max | Unit |
|--------|------------------------------|---|---------|-----|------|
| Offset | Offset error | $f_{ADC} = 15\text{ MHz}$ $V_{DDA} = V_{REF+} = 2.7\text{ V}$ Temperature = 25 °C | ± 1 | — | LSB |
| DNL | Differential linearity error | | +2/-1 | — | |
| INL | Integral linearity error | | ± 3 | — | |

- (1) Based on characterization, not tested in production.

4.14. DAC characteristics

Table 4-27. DAC characteristics⁽³⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|---|-----|-----------|----------------|------------|
| $V_{DDA}^{(1)}$ | Operating voltage | — | 2.7 | 5 | 5.5 | V |
| $V_{REF+}^{(2)}$ | Positive Reference Voltage | — | 2.7 | — | V_{DDA} | V |
| $V_{REF-}^{(2)}$ | Negative Reference Voltage | — | — | V_{SSA} | — | V |
| $R_{LOAD}^{(2)}$ | Resistive load | Resistive load with buffer ON | 1 | — | — | k Ω |
| $R_o^{(2)}$ | Impedance output | Impedance output with buffer OFF | — | — | 35 | k Ω |
| $C_{LOAD}^{(2)}$ | Capacitive load | Capacitive load with buffer ON | — | — | 100 | pF |
| $DAC_OUT_{min}^{(2)}$ | Lower DAC_OUT voltage | Lower DAC_OUT voltage with buffer ON | 0.2 | — | — | V |
| | | Lower DAC_OUT voltage with buffer OFF | 0.5 | — | — | mV |
| $DAC_OUT_{max}^{(2)}$ | Higher DAC_OUT voltage | Higher DAC_OUT voltage with buffer ON | — | — | $V_{DDA}-0.2$ | V |
| | | Higher DAC_OUT voltage with buffer OFF | — | — | $V_{DDA}-1LSB$ | V |
| $I_{DDA}^{(1)}$ | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REF+} = 5.5$ V | — | 590 | — | μ A |
| | | With no load, worst code(0xF1C) on the input, $V_{REF+} = 5.5$ V | — | 670 | — | |
| $I_{DDVREF+}^{(1)}$ | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REF+} = 5.5$ V | — | 95 | — | μ A |
| | | With no load, worst code(0xF1C) on the input, $V_{REF+} = 5.5$ V | — | 250 | — | |
| $DNL^{(1)}$ | Differential non linearity | 10-bit configuration, buffer ON | — | — | ± 1 | LSB |
| | | 12-bit configuration, buffer ON | — | — | ± 4 | |
| $INL^{(1)}$ | Integral non linearity | 10-bit configuration, buffer ON | — | — | ± 1.5 | LSB |
| | | 12-bit configuration, buffer ON | — | — | ± 6 | |
| $Offset^{(1)}$ | Offset error | DAC in 12-bit mode | — | — | ± 22 | LSB |
| $GE^{(1)}$ | Gain error | DAC in 12-bit mode, buffer ON | — | — | ± 1 | % |
| $T_{setting}^{(1)}$ | Settling time | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω | — | 0.5 | 1 | μ s |
| $T_{wakeup}^{(2)}$ | Wakeup from off state | — | — | 5 | 10 | μ s |
| Update rate ⁽²⁾ | Max frequency for a correct DAC_OUT change from | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω | — | — | 2 | MS/s |

| | | | | | | |
|---------------------|---|------------------------------------|---|-----|-----|----|
| | code i to $i \pm 1$ LSB | | | | | |
| PSRR ⁽²⁾ | Power supply rejection ratio(to V_{DDA}) | No R_{Load} , $C_{LOAD} = 50$ pF | — | -80 | -55 | dB |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) Buffer ON mode is recommended when using DAC at high temperature.

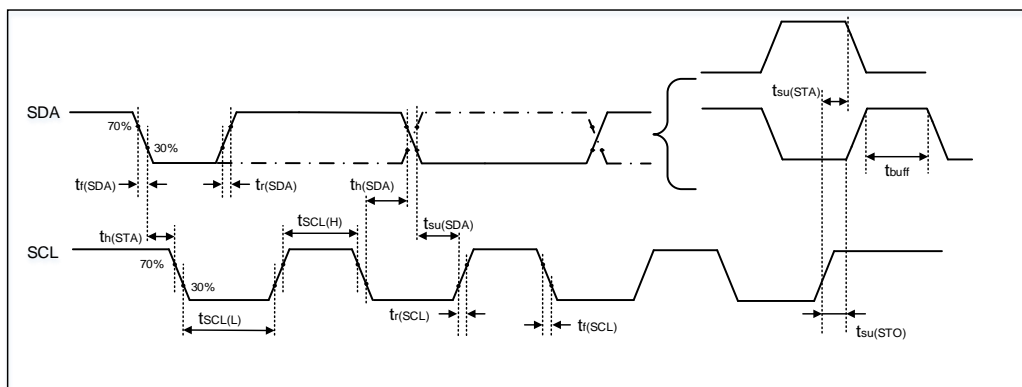
4.15. I2C characteristics

Table 4-28. I2C characteristics⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Fast mode plus | | Unit |
|----------------|---------------------------|------------|------------------|------|-----------|-----|----------------|-----|---------|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | 0.2 | — | μ s |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | 0.5 | — | μ s |
| $t_{su(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | 50 | — | ns |
| $t_h(SDA)$ | SDA data hold time | — | 0 ⁽³⁾ | 3450 | 0 | 900 | 0 | 450 | ns |
| $t_r(SDA/SCL)$ | SDA and SCL rise time | — | — | 1000 | — | 300 | — | 120 | ns |
| $t_f(SDA/SCL)$ | SDA and SCL fall time | — | — | 300 | — | 300 | — | 120 | ns |
| $t_h(STA)$ | Start condition hold time | — | 4.0 | — | 0.6 | — | 0.26 | — | μ s |

- (1) Guaranteed by design, not tested in production.
- (2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.
- (3) The external device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-5. I2C bus timing diagram



4.16. SPI characteristics

Table 4-29. Standard SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--------------------------|---|-----|-------|------|------|
| f_{SCK} | SCK clock frequency | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | — | 22.5 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | | — | 22.22 | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | | — | 22.22 | — | ns |
| SPI master mode | | | | | | |
| $t_{V(MO)}$ | Data output valid time | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | — | 7 | ns |
| $t_{SU(MI)}$ | Data input setup time | | 2 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | | 0 | — | — | ns |
| SPI slave mode | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | $V_{DD} = V_{DDA} = 5\text{ V},$ $f_{PCLK} = 100\text{ MHz}$ | 0 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | | 2 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $V_{DD} = V_{DDA} = 5\text{ V}$ | — | 6 | — | ns |
| $t_{DIS(SO)}$ | Data output disable time | | — | 9 | — | ns |
| $t_{V(SO)}$ | Data output valid time | | — | 9 | — | ns |
| $t_{SU(SI)}$ | Data input setup time | | 0 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | | 1 | — | — | ns |

(1) Based on characterization, not tested in production.

Figure 4-6. SPI timing diagram - master mode

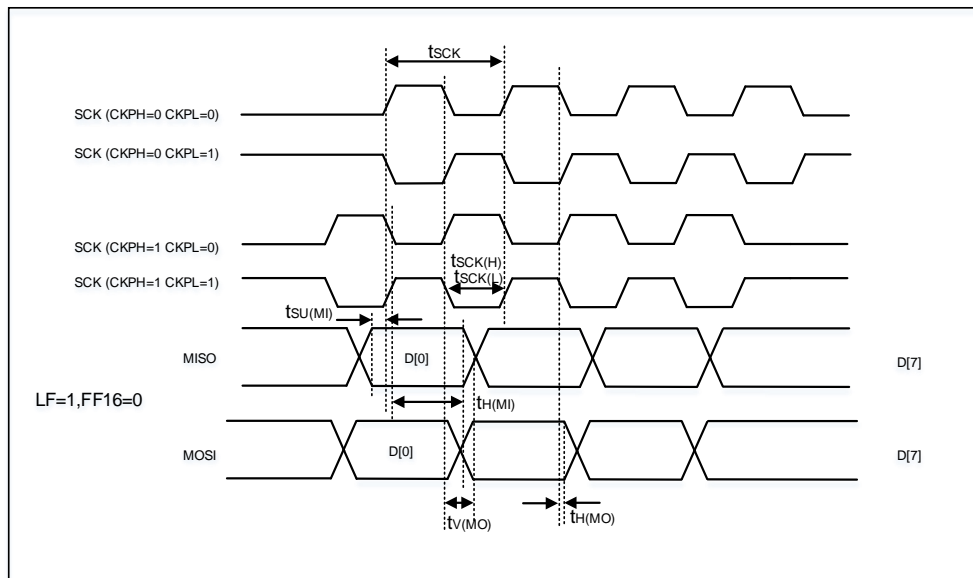
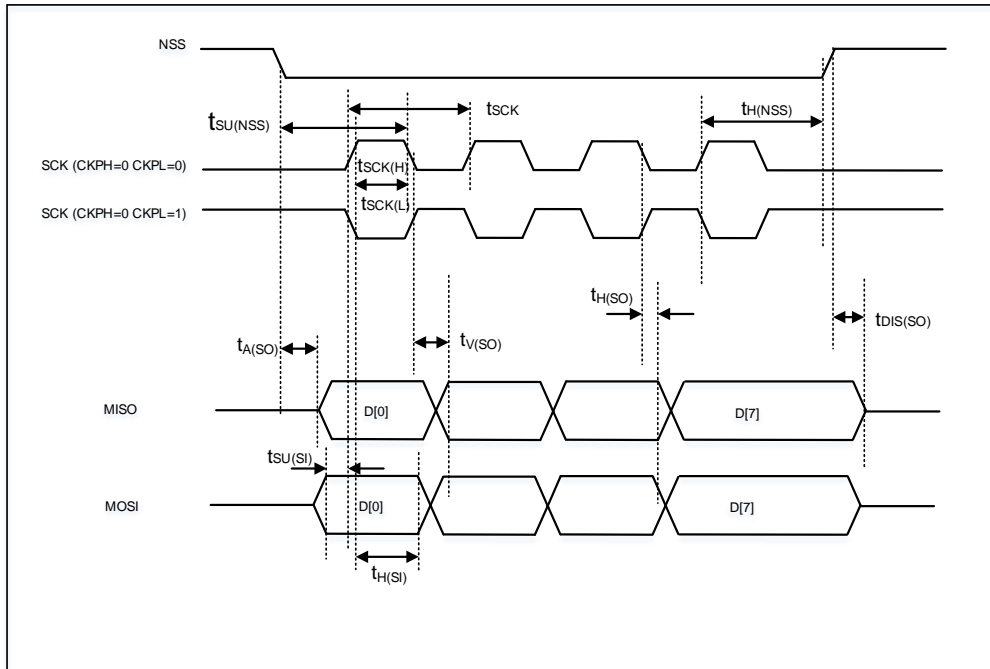


Figure 4-7. SPI timing diagram - slave mode



4.17. I2S characteristics

Table 4-30. I2S characteristics^{(1) (2)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|--|-----|------|------|------|
| f_{CK} | Clock frequency | Master mode (data: 32 bits, Audio frequency = 96 kHz) | — | 6.25 | — | MHz |
| | | Slave mode | — | — | 12.5 | |
| t_H | Clock high time | $f_{CLK} = 6.25$ MHz | — | 80 | — | ns |
| t_L | Clock low time | | — | 80 | — | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | — | 3 | — | ns |
| $t_{H(WS)}$ | WS hold time | Master mode | — | 3 | — | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 0 | — | — | ns |
| $t_{H(WS)}$ | WS hold time | Slave mode | 3 | — | — | ns |
| $D_{CY(SCK)}$ | I2S slave input clock duty cycle | Slave mode | — | 50 | — | % |
| $t_{SU(SD_MR)}$ | Data input setup time | Master mode | 1 | — | — | ns |
| $t_{SU(SD_SR)}$ | Data input setup time | Slave mode | 0 | — | — | ns |
| $t_{H(SD_MR)}$ | Data input hold time | Master receiver | 0 | — | — | ns |
| $t_{H(SD_SR)}$ | | Slave receiver | 1 | — | — | ns |
| $t_{V(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | — | — | 10 | ns |
| $t_{H(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 3 | — | — | ns |
| $t_{V(SD_MT)}$ | Data output valid time | Master transmitter (after enable edge) | — | — | 10 | ns |
| $t_{H(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Figure 4-8. I2S timing diagram - master mode

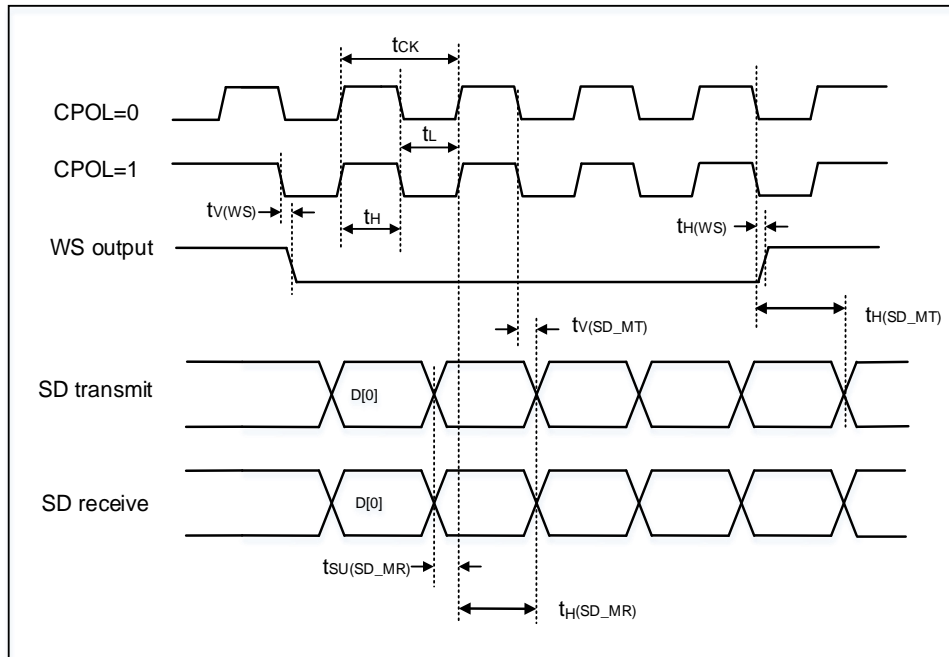
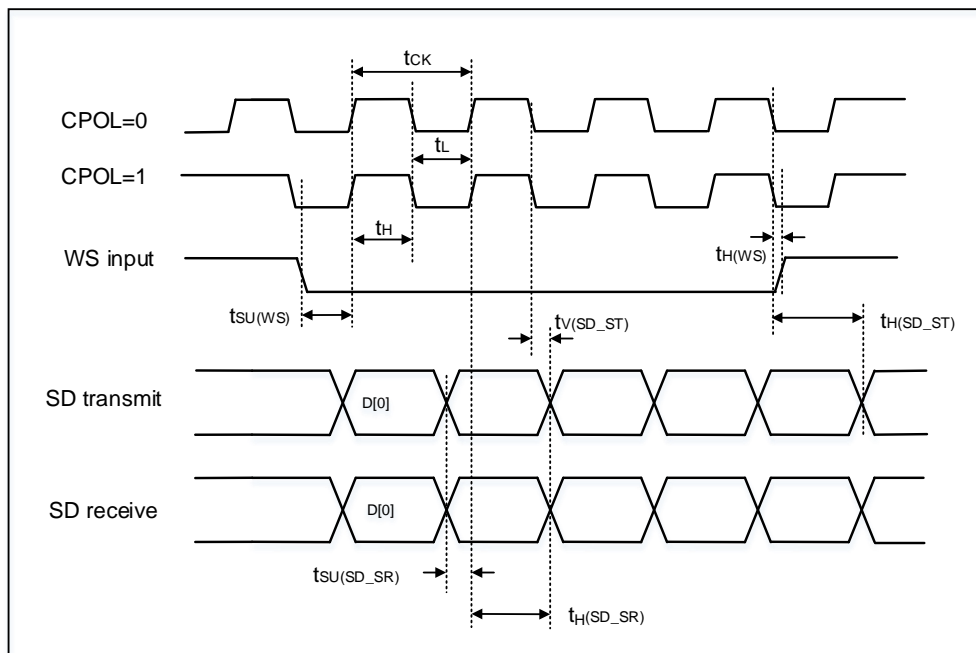


Figure 4-9. I2S timing diagram - slave mode



4.18. USART characteristics

Table 4-31. USART characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------|-------------------------------|-----|-----|------|------|
| f_{SCK} | SCK clock frequency | $f_{PCLKx} = 100 \text{ MHz}$ | — | — | 12.5 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | $f_{PCLKx} = 100 \text{ MHz}$ | 40 | — | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | $f_{PCLKx} = 100 \text{ MHz}$ | 40 | — | — | ns |

(1) Guaranteed by design, not tested in production.

4.19. CAN characteristics

Refer to [Table 4-19. I/O port DC characteristics^{\(1\)}](#) for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

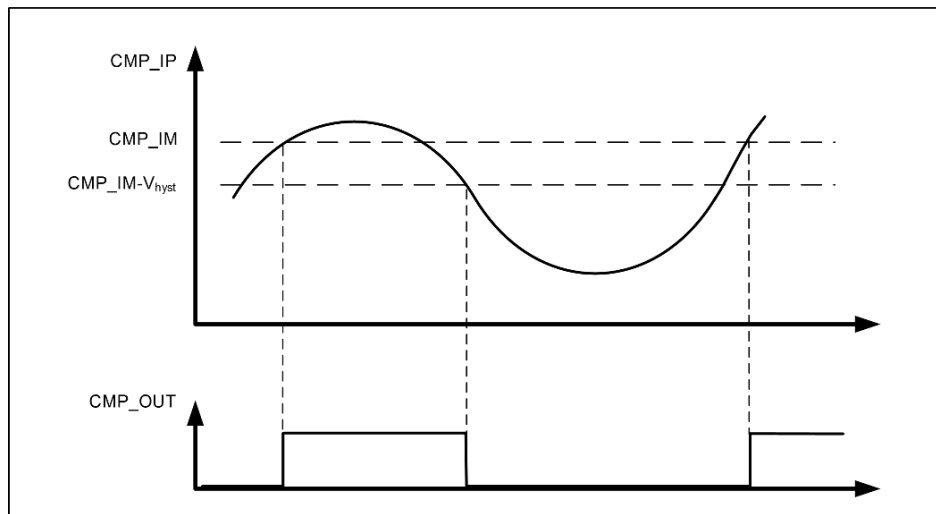
4.20. Comparators characteristics

Table 4-32. CMP characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|--------------------------|-----|---------|-----------|---------------|
| V_{DDA} | Operating voltage | — | 2.7 | 5.0 | 5.5 | V |
| V_{IN} | Input voltage range | — | 0 | — | V_{DDA} | V |
| V_{BG} | Scaler input voltage | — | — | 1.2 | — | V |
| V_{SC} | Scaler offset voltage | — | — | ± 5 | — | mV |
| $I_{DDA(SCALER)}$ | Scaler static consumption from V_{DDA} | BEN = 0 (bridge disable) | — | 750 | — | nA |
| | | BEN = 1 (bridge enable) | — | 1.95 | — | μA |
| t_{START_SCALER} | Scaler startup time | — | — | 100 | — | μs |
| t_D | Propagation delay for 200 mV step with 100 mV overdrive | low power mode | — | 320 | — | ns |
| | | Medium power mode | — | 150 | — | ns |
| | | High speed power mode | — | 50 | — | ns |
| I_{DD} | Current consumption | low power mode | — | 2.7 | — | μA |
| | | Medium power mode | — | 8.2 | — | |
| | | High speed power mode | — | 56 | — | |
| V_{offset} | Offset error | — | — | ± 5 | — | mV |
| V_{hyst} | Hysteresis Voltage | No Hysteresis | — | 0 | — | mV |
| | | Low Hysteresis | — | 18 | — | |
| | | Medium Hysteresis | — | 36 | — | |
| | | High Hysteresis | — | 54 | — | |

(1) Guaranteed by design, not tested in production.

Figure 4-10. CMP hysteresis



4.21. Temperature sensor characteristics

Table 4-33. Temperature sensor characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|--|------|-----------|-----|-------------------|
| $V_{OFF}^{(1)}$ | Uncalibrated Offset | $T_A = 30^{\circ}C$ | — | 1405.6 | — | mV |
| $E_{OFF}^{(1)}$ | Uncalibrated Offset Error | $T_A = 30^{\circ}C$ | — | 3.3 | — | mV |
| $M^{(1)}$ | Slope | — | — | 4.58 | — | mV/ $^{\circ}C$ |
| $E_M^{(1)}$ | Slope Error | — | — | 60 | — | $\mu V/^{\circ}C$ |
| $LIN^{(3)}$ | Linearity | $T_A = -40^{\circ}C$ to $125^{\circ}C$ | — | -2 to 2.5 | — | $^{\circ}C$ |
| t_{ON} | Turn-on Time | — | — | — | — | μs |
| $ETOT^{(2)(3)(4)}$ | Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset | $T_A = -40^{\circ}C$ to $125^{\circ}C$ | -4.5 | — | 5.5 | $^{\circ}C$ |

- (1) Guaranteed by design, not tested in production.
- (2) The factory-calibrated offset value is stored in the read-only area of flash in locations 0x1FFFF7F8.
- (3) Based on characterization, not tested in production.
- (4) The error is the average result of 100 times and represents the chip junction temperature error. The chip self-heating shall be considered when testing ambient temperature.

4.22. TIMER characteristics

Table 4-34. TIMER characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|--------------------------------|----------------------------------|-----|-------------------|-----------------|
| t_{res} | Timer resolution time | — | 1 | — | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK} = 100\text{ MHz}$ | 10 | — | ns |
| f_{EXT} | Timer external clock frequency | — | 0 | $f_{TIMERxCLK}/2$ | MHz |
| | | $f_{TIMERxCLK} = 100\text{ MHz}$ | 0 | 50 | MHz |

| | | | | | |
|------------------------|--|----------------------------------|------|-------------|------------------------|
| RES | Timer resolution | — | — | 16 | bit |
| t _{COUNTER} | 16-bit counter clock period when internal clock is selected | — | 1 | 65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 100 MHz | 0.01 | 655.36 | μs |
| t _{MAX_COUNT} | Maximum possible count | — | — | 65536x65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 100 MHz | — | 42.95 | s |

(1) Guaranteed by design, not tested in production.

4.23. WDGT characteristics

Table 4-35. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾

| Prescaler divider | PSC[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|-------------------|---------------|----------------------------------|----------------------------------|------|
| 1/4 | 000 | 0.03125 | 511.90625 | ms |
| 1/8 | 001 | 0.03125 | 1023.7812 | |
| 1/16 | 010 | 0.03125 | 2047.53125 | |
| 1/32 | 011 | 0.03125 | 4095.03125 | |
| 1/64 | 100 | 0.03125 | 8190.03125 | |
| 1/128 | 101 | 0.03125 | 16380.03125 | |
| 1/256 | 110 or 111 | 0.03125 | 32760.03125 | |

(1) Guaranteed by design, not tested in production.

Table 4-36. WWDGT min-max timeout value at 50 MHz (f_{PCLK1}) ⁽¹⁾

| Prescaler divider | PSC[1:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|-------------------|----------|--------------------------------------|------|--------------------------------------|------|
| 1/1 | 00 | 81.92 | μs | 5.24 | ms |
| 1/2 | 01 | 163.84 | | 10.49 | |
| 1/4 | 10 | 327.68 | | 20.97 | |
| 1/8 | 11 | 655.36 | | 41.94 | |

(1) Guaranteed by design, not tested in production.

4.24. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 5 V, T_A = 25°C.

5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

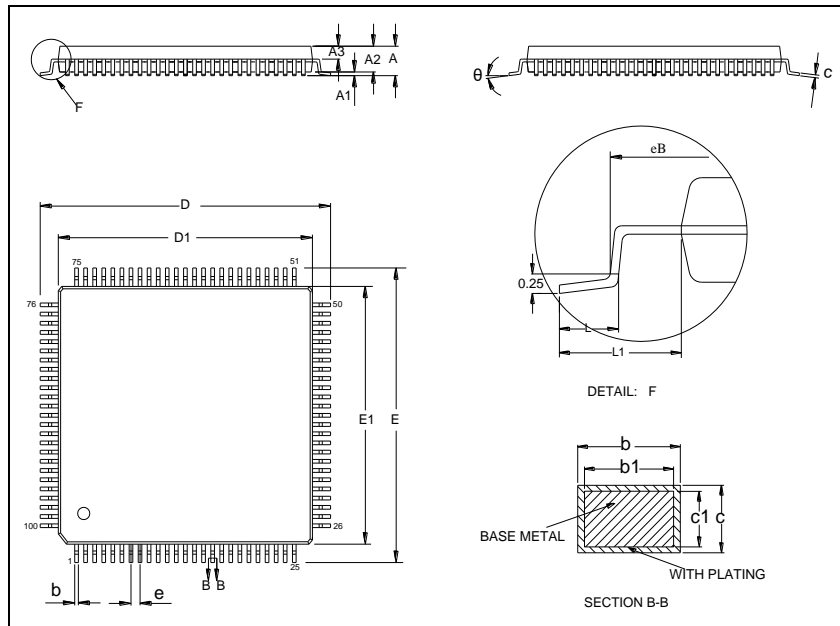
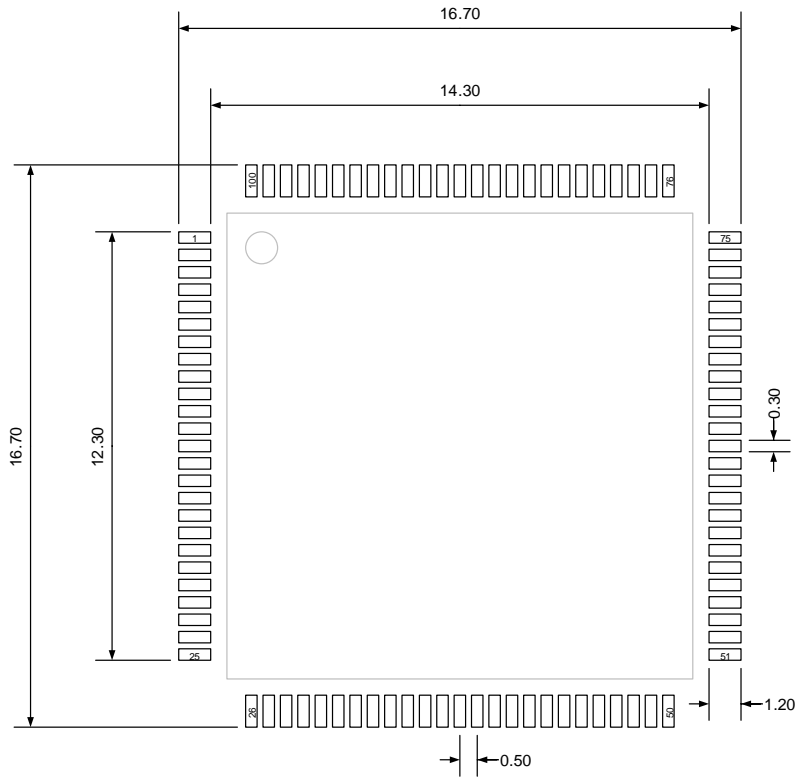


Table 5-1. LQFP100 package dimensions

| Symbol | Min | Typ | Max |
|----------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | — | 0.50 | — |
| eB | 15.05 | — | 15.35 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-2. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

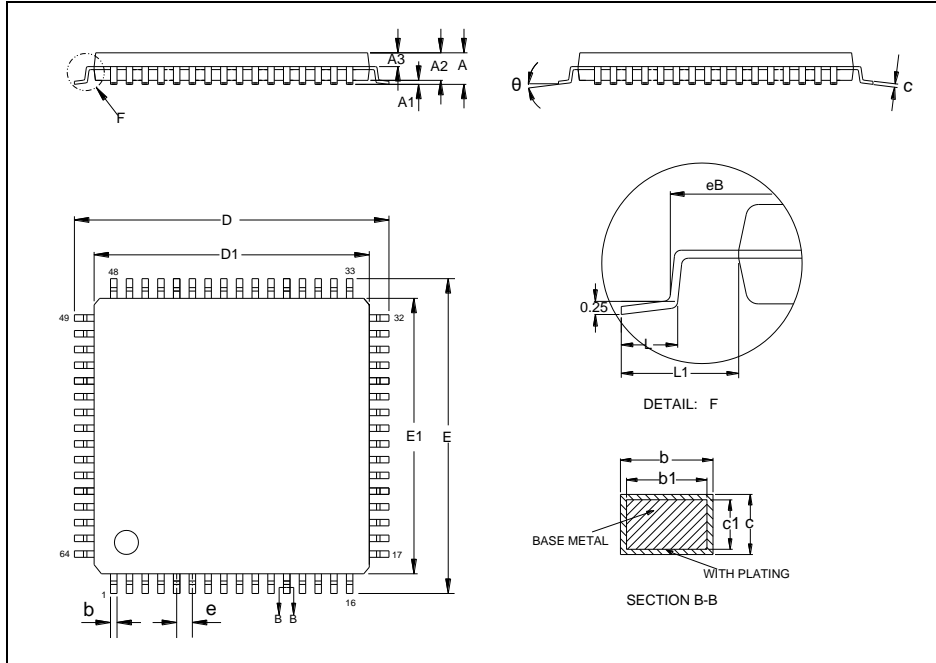
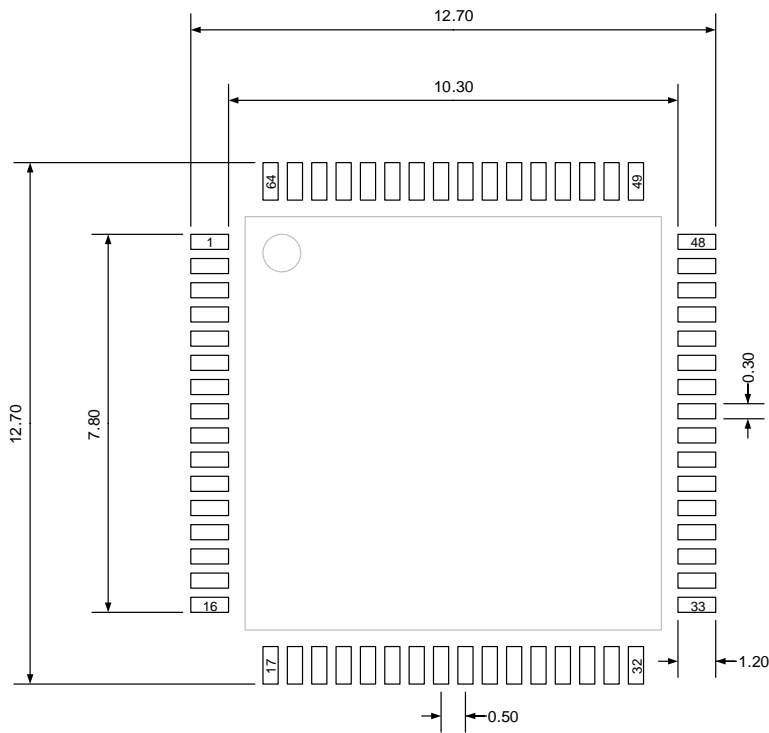


Table 5-2. LQFP64 package dimensions

| Symbol | Min | Typ | Max |
|--------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | — | 0.50 | — |
| eB | 11.25 | — | 11.45 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-4. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.3. LQFP48 package outline dimensions

Figure 5-5. LQFP48 package outline

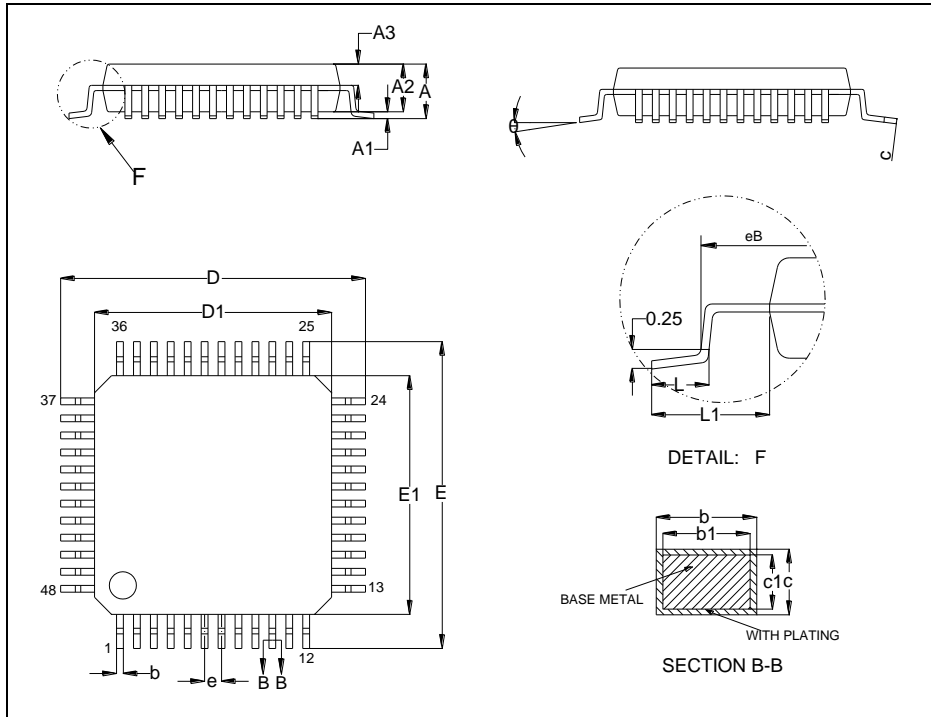
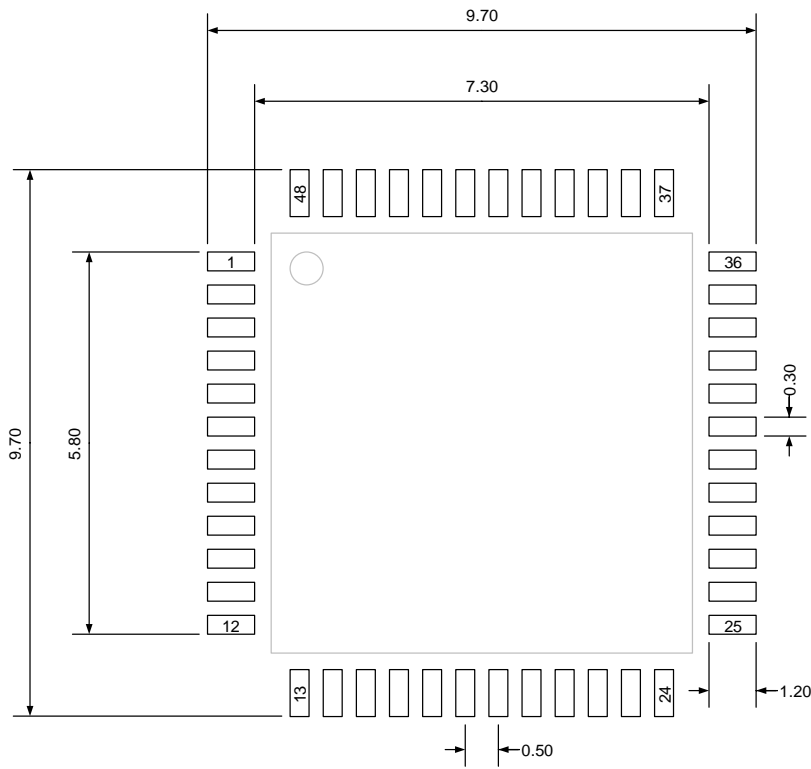


Table 5-3. LQFP48 package dimensions

| Symbol | Min | Typ | Max |
|----------|------|------|------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | — | 0.50 | — |
| eB | 8.10 | — | 8.25 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-6. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.4. QFN32 package outline dimensions

Figure 5-7. QFN32 package outline

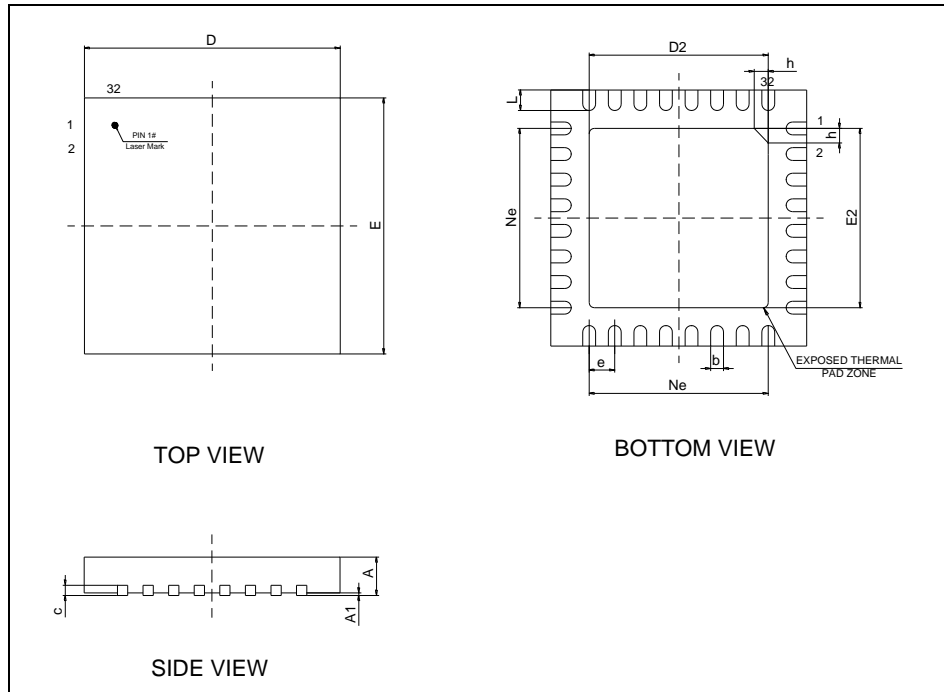
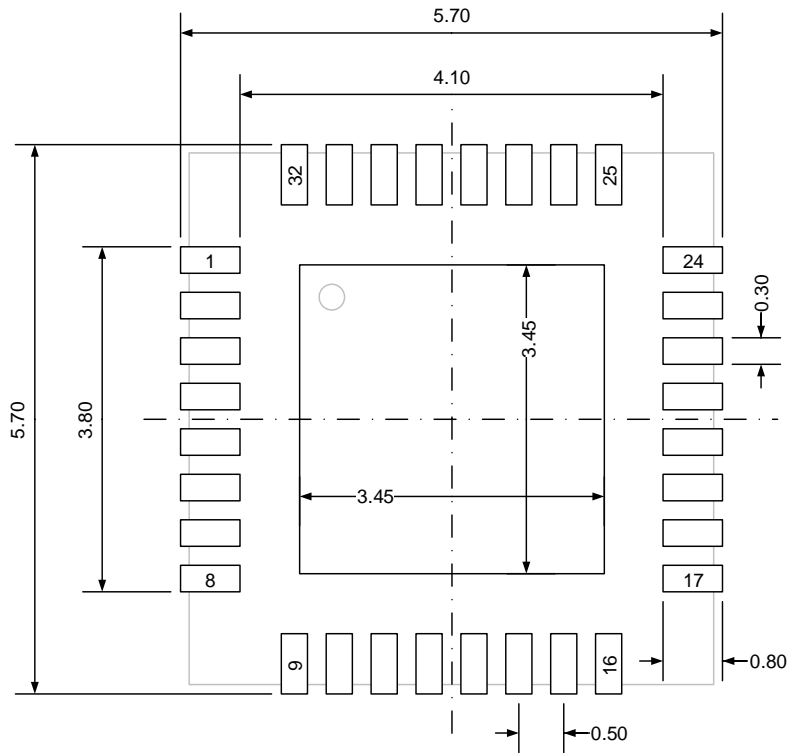


Table 5-4. QFN32 package dimensions

| Symbol | Min | Typ | Max |
|--------|------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.40 | 3.50 | 3.60 |
| e | — | 0.50 | — |
| h | 0.30 | 0.35 | 0.40 |
| L | 0.35 | 0.40 | 0.45 |
| Ne | — | 3.50 | — |

(Original dimensions are in millimeters)

Figure 5-8. QFN32 recommended footprint



(Original dimensions are in millimeters)

5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ θ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA} : Thermal resistance, junction-to-ambient.

θ_{JB} : Thermal resistance, junction-to-board.

θ_{JC} : Thermal resistance, junction-to-case.

Ψ_{JB} : Thermal characterization parameter, junction-to-board.

Ψ_{JT} : Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5-1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5-2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5-3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-5. Package thermal characteristics⁽¹⁾

| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| θ_{JA} | Natural convection, 2S2P PCB | LQFP100 | 56.74 | °C/W |
| | | LQFP64 | TBD | |
| | | LQFP48 | TBD | |
| | | QFN32 | TBD | |
| θ_{JB} | Cold plate, 2S2P PCB | LQFP100 | 42.61 | °C/W |
| | | LQFP64 | TBD | |
| | | LQFP48 | TBD | |

| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| | | QFN32 | TBD | |
| θ_{JC} | Cold plate, 2S2P PCB | LQFP100 | 15.02 | °C/W |
| | | LQFP64 | TBD | |
| | | LQFP48 | TBD | |
| | | QFN32 | TBD | |
| Ψ_{JB} | Natural convection, 2S2P PCB | LQFP100 | 43.37 | °C/W |
| | | LQFP64 | TBD | |
| | | LQFP48 | TBD | |
| | | QFN32 | TBD | |
| Ψ_{JT} | Natural convection, 2S2P PCB | LQFP100 | 1.41 | °C/W |
| | | LQFP64 | TBD | |
| | | LQFP48 | TBD | |
| | | QFN32 | TBD | |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32A503xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|-------------------------------|
| GD32A503VDT3 | 384 | LQFP100 | Green | Automotive -40°C to +125°C |
| GD32A503VCT3 | 256 | LQFP100 | Green | Automotive -40°C to +125°C |
| GD32A503VBT3 | 128 | LQFP100 | Green | Automotive -40°C to +125°C |
| GD32A503RDT3 | 384 | LQFP64 | Green | Automotive -40°C to +125°C |
| GD32A503RCT3 | 256 | LQFP64 | Green | Automotive -40°C to +125°C |
| GD32A503RBT3 | 128 | LQFP64 | Green | Automotive -40°C to +125°C |
| GD32A503CCT3 | 256 | LQFP48 | Green | Automotive -40°C to +125°C |
| GD32A503CBT3 | 128 | LQFP48 | Green | Automotive -40°C to +125°C |
| GD32A503KCU3 | 256 | QFN32 | Green | Automotive -40°C to +125°C |
| GD32A503KBU3 | 128 | QFN32 | Green | Automotive -40°C to +125°C |

7. Revision history

Table 7-1. Revision history

| Revision No. | Description | Date |
|--------------|-----------------|--------------|
| 1.0 | Initial Release | Sep.15, 2021 |

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