GDP1BFLM

DATASHEET

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1 FEATURES

- Power supply: VDD = VDDQ=1.35V (1.283 - 1.45V)
- Backward compatible to VDD = VDDQ = 1.5V ±0.075V
  – Supports DDR3L devices to be backward compatible in 1.5V application
- Package: 96 balls FBGA (x16)
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin, 933MHz f_{CK} for 1866Mb/sec/pin and 1067 MHz f_{CK} for 2133Mb/sec/pin
- Array configuration: 8 Banks
- 8-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- Operating case temperature: 0 ℃ ≤ T_{CASE} ≤ 95 ℃
- Average Refresh Period:
  -7.8 us at 0 ℃ ≤ T_{CASE} ≤ 85 ℃
  -3.9 us at 85 ℃ ≤ T_{CASE} ≤ 95 ℃
- JEDEC JESD79-3E compliant
- RoHS compliant

Note:

1. The functionality described and the timing specifications included in this data sheet are for the DLL enabled mode of operation.

1.1 Address Table

Parameter	256 Mb x 8	128 Mb x 16
Number of Banks	8	8
Bank Address	BA0 - BA2	BA0 - BA2
Auto precharge	A_{10} / AP	A_{10} / AP
BC switch on the fly	A_{12} / BC#	A_{12} / BC#
Row Address	A_0 - A_{14}	A_0 - A_{13}
Column Address	A_0 - A_9	A_0 - A_9
Page Size[1]	1KB	2KB

Note:

1. Page size is the number of bytes of the data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

   Page size = $2^{COLBITS}$ * ORG / 8

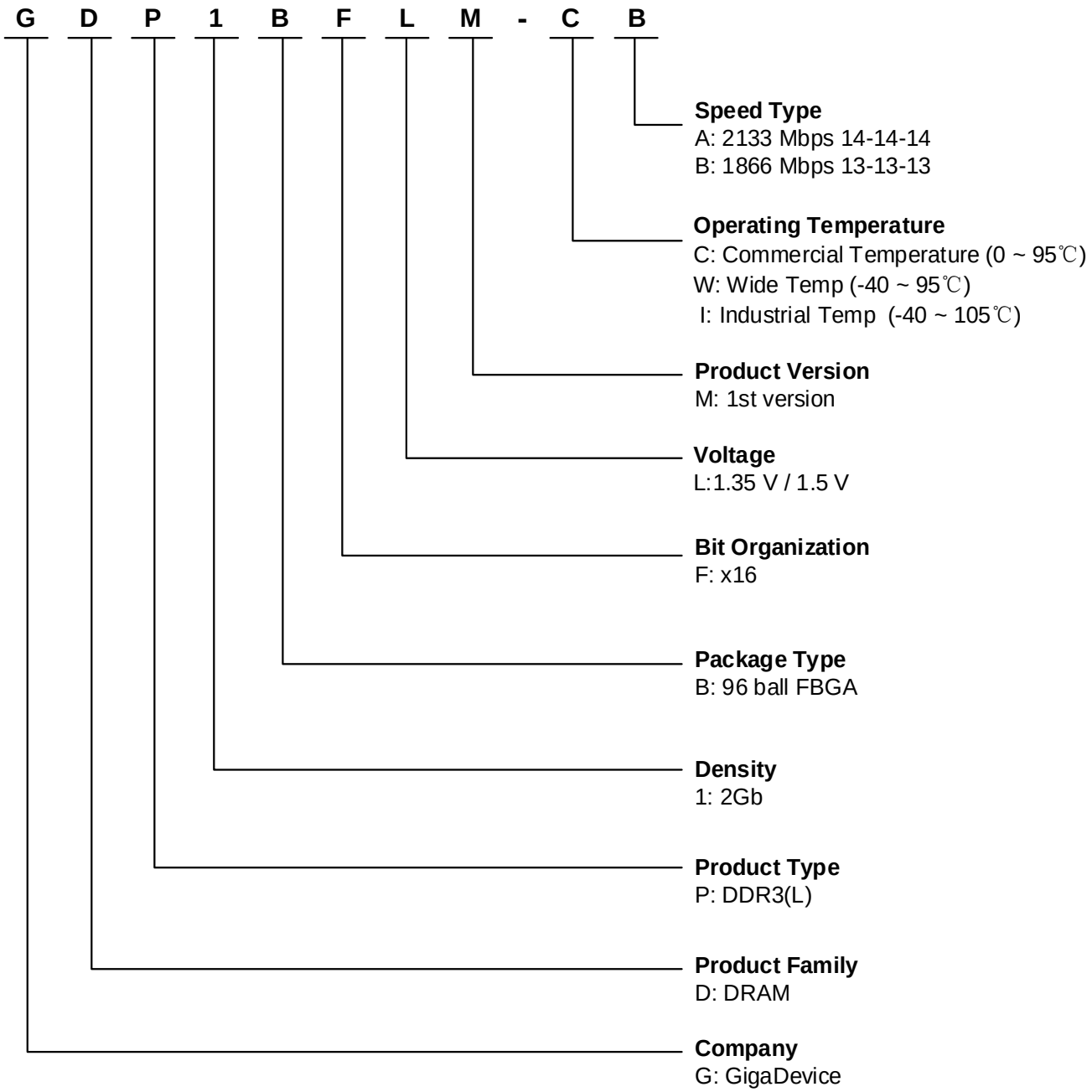
   Where

   COLBITS = the number of column address bits

   ORG = the number of I/O (DQ) bits

2 ORDERING INFORMATION

2.1 Part Number Decoding

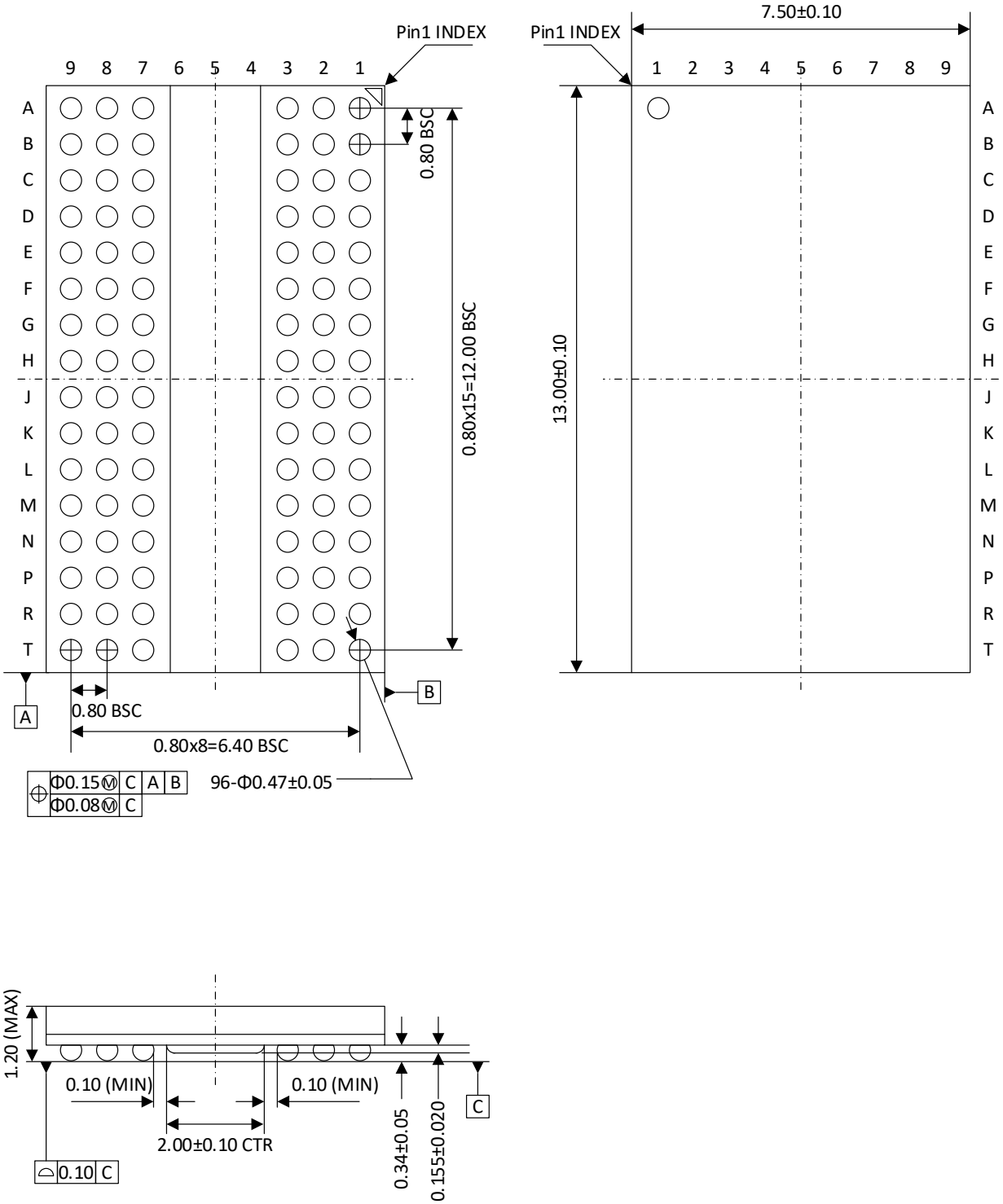


2.2 Valid Part Numbers

Part Number	Organization	Data Rate	CL-tRCD-tRP
GDP1BFLM-CB	128 Mb x16	1866 Mbps	13-13-13
GDP1BFLM-CA	128 Mb x16	2133 Mbps	14-14-14

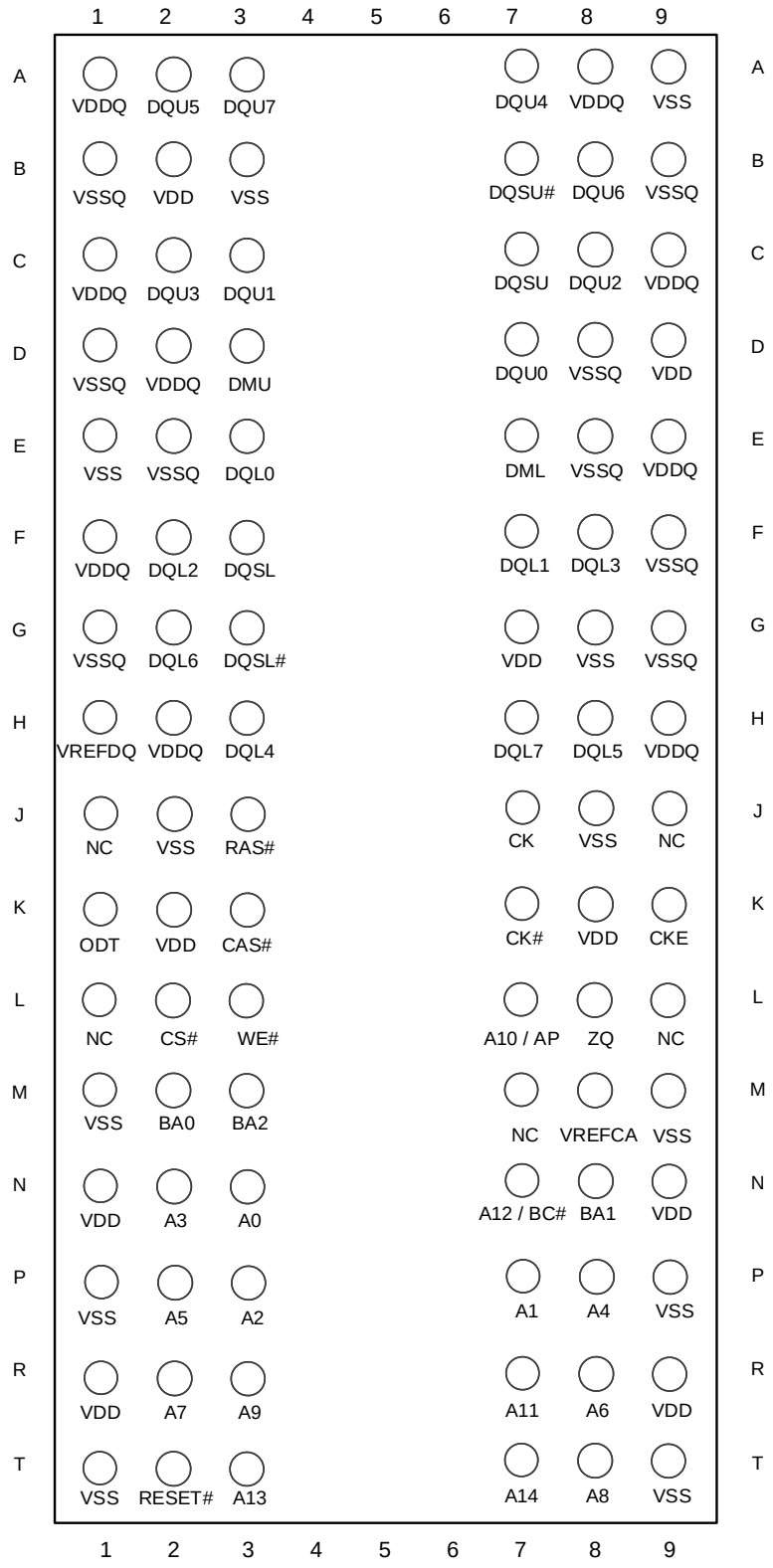
3 PACKAGE INFORMATION

3.1 Package 96-Ball FBGA (x16)



4 BALL ASSIGNMENTS

4.1 96-Ball FBGA (x16) ball assignments



4.2 Ball Description

Symbol	Type	Function
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK#.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	**Chip Select:** All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS# WE#	Input	**Command Input:** RAS#, CAS#, and WE# (along with CS#) defines the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs:** BA0-BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A14	Input	**Address Inputs:** Provide the row address for Activate commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10 / AP and A12 / BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Auto-precharge:** A10 is sampled during Read / Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses..
A12 / BC#	Input	**Burst Chop:** A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped).

Symbol	Type	Function
RESET#	Input	**Active Low Asynchronous Reset:** Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 1.20V for DC high and 0.30V for DC low.
DQ	I/O	**Data Input/Output:** Bi-directional data bus.
DQS, DQS# DQSL, DQSL# DQSU, DQSU#	I/O	**Data Strobe:** Output with Read data, input with Write data. Edge-aligned with Read data, centered in Write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during Reads and Writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, TDQS#	Output	**Termination Data Strobe:** TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC	-	**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** DDR3L operation = 1.283 to 1.45V; DDR3 operation = 1.425 to 1.575V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** DDR3L operation = 1.283 to 1.45V; DDR3 operation = 1.425 to 1.575V
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference voltage for DQ**
V_{REFCA}	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**

Note:

Input only pins (BA0-BA2, A0-A14, RAS#, CAS#, WE#, CS#, CKE, ODT and RESET#) do not supply termination.

5 FUNCTIONAL BLOCK DIAGRAMS

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 5-1. 256 Meg x 8 Functional Block Diagram

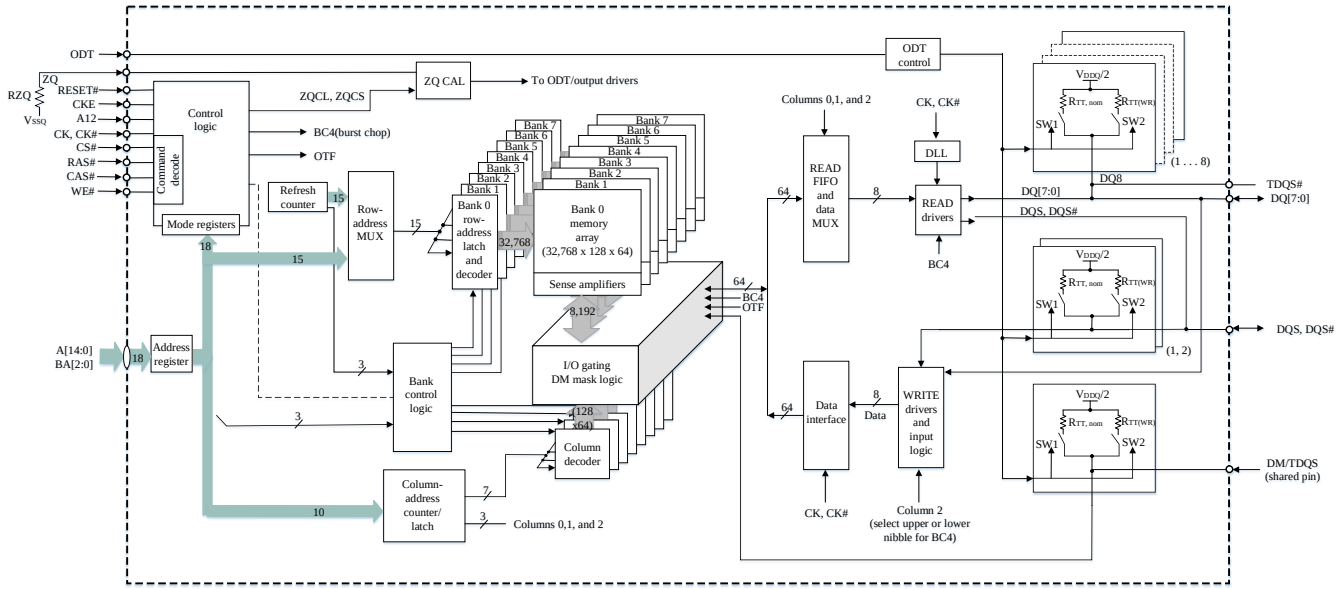
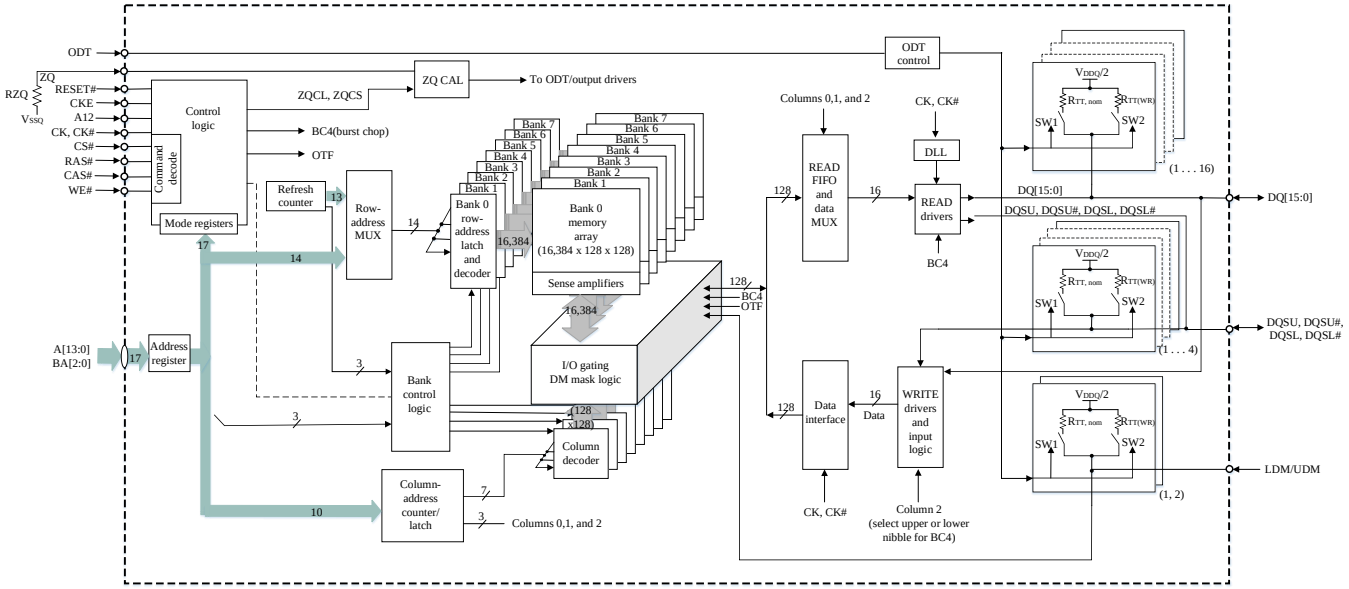


Figure 5-2. 128 Meg x 16 Functional Block Diagram



6 ABSOLUTE MAXIMUM RATINGS

6.1 Absolute Maximum DC Ratings

Table 6-1. Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Unit	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ 1.80 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ 1.80 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ 1.80 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD79-3E standard.
3. V_{DD} and V_{DDQ} must be within 300 mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

6.2 Recommended DC Operating Conditions

Table 6-2. Recommended DC Operating Conditions

Symbol	Parameter		Ratings			Unit	Note
			Min	Typ.	Max		
V_{DD}	Supply voltage	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply voltage for output	DDR3L	1.283	1.35	1.45	V	1,2,3,4,5,6
		DDR3	1.425	1.5	1.575	V	1,2

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDD (t) over a long period of time
4. If the maximum limit is exceeded, the input levels are covered by the DDR3 specification.
5. With these supply voltages, the device operates with DDR3L specifications.
6. The DDR3L product supports 1.5V operation, and if initialized as such, retains the original speed timings defined for DDR3L speed

6.3 DRAM Component Operating Temperature Range

Table 6-3. Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range (Optional)	85 to 95	°C	1,3

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD79-3E.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range.
   - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1_b and MR2 A7 = 0_b).

7 AC AND DC INPUT MEASUREMENT LEVELS

7.1 AC and DC Logic Input Levels for Single-ended Signals

7.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 7-1. Single-ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.CA}$(DC90)	DC input logic high	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	V_{DD}	V	1
$V_{IL.CA}$(DC90)	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V	1
$V_{IH.CA}$(AC160)	AC input logic high	V_{REF} + 0.16	Note 2	V_{REF} + 0.16	Note 2	-	-	V	1,2,5
$V_{IL.CA}$(AC160)	AC input logic low	Note 2	V_{REF} - 0.16	Note 2	V_{REF} - 0.16	-	-	V	1,2,5
$V_{IH.CA}$(AC135)	AC input logic high	V_{REF} + 0.135	Note 2	V_{REF} + 0.135	Note 2	V_{REF} + 0.135	Note 2	V	1,2,5
$V_{IL.CA}$(AC135)	AC input logic low	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	V	1,2,5
$V_{IH.CA}$(AC125)	AC input logic high	-	-	-	-	V_{REF} + 0.125	Note 2	V	1,2,5
$V_{IL.CA}$(AC125)	AC input logic low	-	-	-	-	Note 2	V_{REF} - 0.125	V	1,2,5
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866/2133		Unit	Note
		Min	Max	Min	Max	Min	Max		
$V_{IH.CA}$(DC100)	DC input logic high	V_{REF} + 0.10	V_{DD}	V_{REF} + 0.10	V_{DD}	V_{REF} + 0.10	V_{DD}	V	1
$V_{IL.CA}$(DC100)	DC input logic low	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V	1
$V_{IH.CA}$(AC175)	AC input logic high	V_{REF} + 0.175	Note 2	V_{REF} + 0.175	Note 2	-	-	V	1,2,5
$V_{IH.CA}$(AC175)	AC input logic low	Note 2	V_{REF} - 0.175	Note 2	V_{REF} - 0.175				
$V_{IL.CA}$(AC150)	AC input logic high	V_{REF} + 0.150	Note 2	V_{REF} + 0.150	Note 2	-	-	V	1,2,5
$V_{IH.CA}$(AC150)	AC input logic low	Note 2	V_{REF} - 0.150	Note 2	V_{REF} - 0.150	-	-	V	1,2,5
$V_{IL.CA}$(AC135)	AC input logic high	-	-	-	-	V_{REF} + 0.135	Note 2	V	1,2,5
$V_{IH.CA}$(AC135)	AC input logic low	-	-	-	-	Note 2	V_{REF} - 0.135	V	1,2,5

$V_{IL.CA}$(AC125)	AC input logic high	-	-	-	-	V_{REF} + 0.125	Note 2	V	1,2,5
$V_{IL.CA}$(AC125)	AC input logic low	-	-	-	-	Note 2	V_{REF} - 0.125	V	1,2,5
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Note:

1. For input only pins except RESET#. V_{REF} = V_{REFCA}(DC).
2. See JESD79-3E,9.6 “Overshoot/Undershoot Specification”,9.6.1.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than ± 1% VDD (for reference: approx. ± 13.5 mV)
4. For reference: DDR3 has approx. VDD/2 +/- 15mV, DDR3L has approx VDD/2 +/- 13.5mV.
5. To allow VREFCA margining, all DRAM Command and Address Input Buffers MUST use external VREF (provided by system) as the input for their VREFCA pins. All VIH/L input level MUST be compared with the external VREF level at the 1st stage of the Command and Address input buffer.

7.1.2 AC and DC Input Levels for Single-Ended Data Signals

Table 7-2. Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-1333/1600		DDR3L-1866/2133		Unit	Note
		Min	Max	Min	Max		
$V_{IH.DQ}$(DC90)	DC input logic high	V_{REF} + 0.09	V_{DD}	V_{REF} + 0.09	V_{DD}	V	1
$V_{IL.DQ}$(DC90)	DC input logic low	V_{SS}	V_{REF} - 0.09	V_{SS}	V_{REF} - 0.09	V	1
$V_{IH.DQ}$(AC160)	AC input logic high	-	-	-	-	V	1.2.5
$V_{IL.DQ}$(AC160)	AC input logic low	-	-	-	-	V	1.2.5
$V_{IH.DQ}$(AC135)	AC input logic high	V_{REF} + 0.135	Note 2	-	-	V	1.2.5
$V_{IL.DQ}$(AC135)	AC input logic low	Note 2	V_{REF} - 0.135	-	-	V	1.2.5
$V_{IH.DQ}$(AC130)	AC input logic high	-	-	V_{REF} + 0.13	Note 2	V	1.2.5
$V_{IL.DQ}$(AC130)	AC input logic low	-	-	Note 2	V_{REF} - 0.13	V	1.2.5
$V_{REFDQ(DC)}$	Reference voltage for DQ, DM inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Symbol	Parameter	DDR3-1333/1600		DDR3-1866/2133		Unit	Note
		Min	Max	Min	Max		
$V_{IH.DQ}$(DC100)	DC input logic high	V_{REF} + 0.10	V_{DD}	V_{REF} + 0.10	V_{DD}	V	1
$V_{IL.DQ}$(DC100)	DC input logic low	V_{SS}	V_{REF} - 0.10	V_{SS}	V_{REF} - 0.10	V	1
$V_{IH.DQ}$(AC175)	AC input logic high	-	-	-	-	V	1.2.5
$V_{IL.DQ}$(AC175)	AC input logic low	-	-	-	-	V	1.2.5
$V_{IH.DQ}$(AC150)	AC input logic high	V_{REF} + 0.150	Note 2	-	-	V	1.2.5
$V_{IL.DQ}$(AC150)	AC input logic low	Note 2	V_{REF} - 0.150	-	-	V	1.2.5
$V_{IH.DQ}$(AC135)	AC input logic high	V_{REF} + 0.135	Note 2	V_{REF} + 0.135	Note 2	V	1.2.5
$V_{IL.DQ}$(AC135)	AC input logic low	Note 2	V_{REF} - 0.135	Note 2	V_{REF} - 0.135	V	1.2.5
$V_{REFDQ(DC)}$	Reference voltage for DQ, DM inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3,4

Note:

1. For input only pins except RESET#. V_{REF} = $V_{REFDQ(DC)}$.
2. See JESD79-3E,9.6 “Overshoot/Undershoot Specification”,9.6.2.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFDQ(DC)}$ by more than ± 1% VDD (for reference: approx. ± 13.5 mV)
4. For reference: DDR3 has approx. VDD/2 ±15mV, and DDR3L has approx. VDD/2 ± 13.5mV.
5. Single-ended swing requirement for DQS-DQS#, is 350mV (peak to peak). Differential swing requirement for DQS-DQS#, is 700mV (peak to peak).

7.2 V_{Ref} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrate in Figure 7-1. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

$V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 7-1. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than ± 1% VDD.

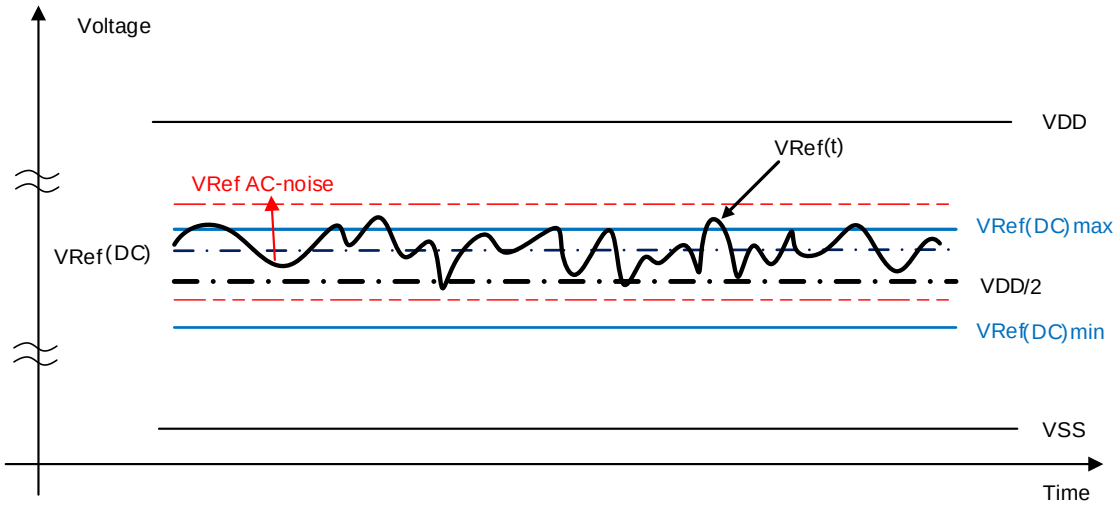


Figure 7-1. Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $VI_{H(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}.

"V_{Ref}" should be understood as $V_{Ref\,(DC)}$

This clarifies that DC-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level, and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref\,(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (± 1% of VDD) are included in DRAM timings and their associated deratings.

7.3 AC and DC Logic Input Levels for Differential Signals

7.3.1 Differential Signals Definition

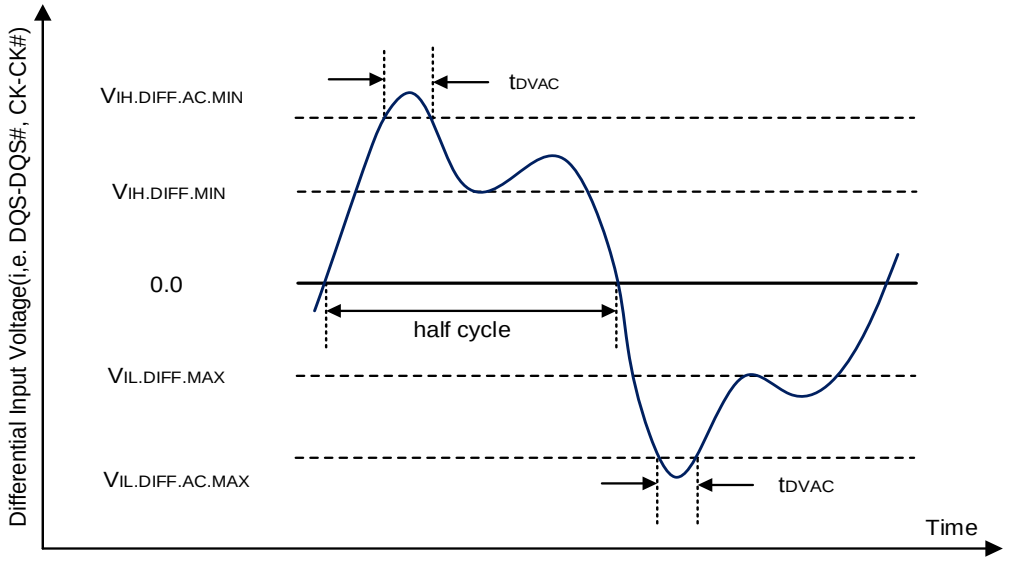


Figure 7-2. Definition of Differential AC-Swing and "Time above AC-Level" t_{DVAC}

7.3.2 Differential Swing Requirements for Clock (CK – CK#) and strobe (DQS – DQS#)

Table 7-3. Differential AC and DC Input Levels

Symbol	Parameter	DDR3L/DDR3-800/1066/1333/1600/1866				Unit	Note
		1.35V		1.5V			
		Min	Max	Min	Max		
V_{IHdiff}	Differential input high	+ 0.18	Note 3	+ 0.20	Note 3	V	1
V_{ILdiff}	Differential input logic low	Note 3	- 0.18	Note 3	- 0.20	V	1
V_{IHdiff}(AC)	Differential input high ad	2 x (V_{IH}(AC) - V_{Ref}	Note 3	2 x (V_{IH}(AC) - V_{Ref}	Note 3	V	2
V_{ILdiff}(AC)	Differential input low ac	Note 3	2 x (V_{IL}(AC) - V_{Ref}	Note 3	2 x (V_{IL}(AC) - V_{Ref}	V	2

Note:

1. Used to define a differential signal slew-rate.
2. for CK – CK# use V_{IH}/V_{IL}(AC) of ADD/CMD and V_{REFCA}; for DQS – DQS#, DQSL – DQSL#, DQSU –DQSU# use V_{IH}/V_{IL}(AC) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 7-4. Allowed Time before Ringback (tDVAC) for CK – CK# and DQS – DQS# (1.35 V)

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600				DDR3L-1866/2133					
	t_{DVAC} [ps] @ VIH/Ldiff(AC) = 320mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) = 270mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) = 270mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) = 250mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) == 260mV	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	Note	-	44	-	5	-	22	-	24	-
1.0	Note	-	Note	-	Note	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level

Table 7-5. Allowed Time before Ringback (tDVAC) for CK – CK# and DQS – DQS# (1.5 V)

Slew Rate [V/ns]	DDR3-800/1066/1333/1600						DDR3-1866/2133			
	t_{DVAC} [ps] @ VIH/Ldiff(AC) = 350mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) = 300mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) = (DQS –DQS#) only (Optional)		t_{DVAC} [ps] @ VIH/Ldiff(AC) = 300mV		t_{DVAC} [ps] @ VIH/Ldiff(AC) =(CK – CK#) only	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
> 4.0	75	-	175	-	214	-	134	-	139	-
4.0	57	-	170	-	214	-	134	-	139	-
3.0	50	-	167	-	191	-	112	-	118	-
2.0	38	-	119	-	146	-	67	-	77	-
1.8	34	-	102	-	131	-	52	-	63	-
1.6	29	-	81	-	113	-	33	-	45	-
1.4	22	-	54	-	88	-	9	-	23	-
1.2	Note	-	19	-	56	-	Note	-	Note	-
1.0	Note	-	Note	-	11	-	Note	-	Note	-
<1.0	Note	-	Note	-	Note	-	Note	-	Note	-

Note:

1. Rising input differential signal shall become equal to or greater than VIHdiff(ac) level and Falling input differential signal shall become equal to or less than VILdiff(ac) level.

7.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH}(ac)/V_{IL}(ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, DQS#, DQSL# have to reach V_{SEH}min / V_{SEL}max (approximately the ac-levels [V_{IH}(AC) / V_{IL}(AC)] for DQ signal) in every half-cycleproceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc.

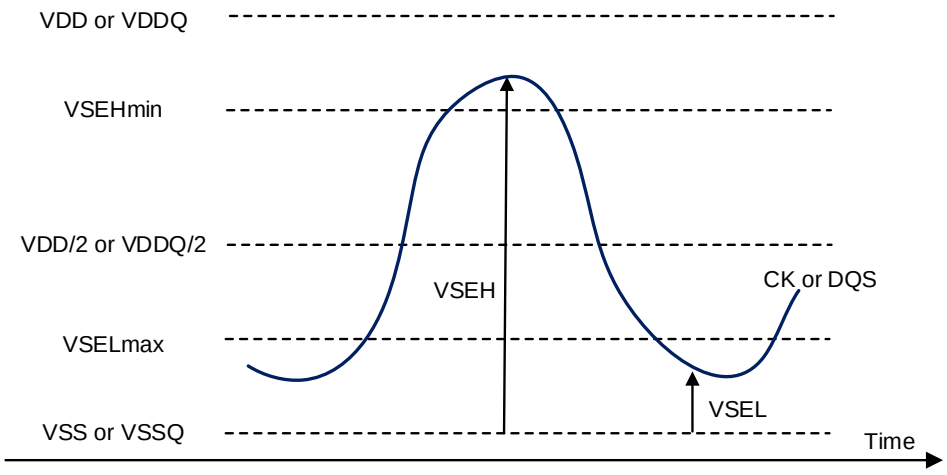


Figure 7-3. Single-ended Requirement for Differential Signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to V_{Ref}, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 7-6. Single-ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#

Symbol	Parameter	DDR3L/DDR3-800/1066/1333/1600/1866		Unit	Notes
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	(VDD/2) + 0.175	Note 3	V	1,2
	Single-ended high-level for CK, CK#	(VDD/2) + 0.175	Note 3	V	1,2
V_{SEL}	Single-ended low-level for strobes	Note 3	(VDD/2) - 0.175	V	1,2
	Single-ended low-level for CK, CK#	Note 3	(VDD/2) - 0.175	V	1,2

Note

1. For CK, CK# use V_{IH}/V_{IL}(AC) of ADD/CMD; for storbes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use V_{IH}/V_{IL}(AC) of DQs.
2. V_{IH}(AC)/V_{IL}(AC) for DQ is based on V_{REFDQ}; V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then thereduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

7.4 Differential Input Cross Point Voltage

The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

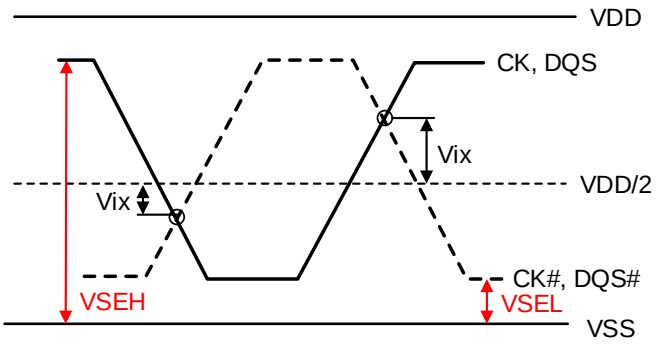


Figure 7-4. V_{IX} Definition

Table 7-7. Cross Point Voltage for Differential Input Signals (CK, DQS):1.35 V

Symbol	Parameter	DDR3L – 800/1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
V_{IX}(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	1
V_{IX}(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	

Note:

1. The relation between V_{IX} Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + V_{IX}(Min) – VSEL ≥ 25mV
   VSEH- ((VDD/2) + V_{IX}(Max)) ≥ 25mV

Table 7-8. Cross Point Voltage for Differential Input Signals (CK, DQS):1.5 V

Symbol	Parameter	DDR3 – 800/1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
V_{IX}(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	2
		-175	-175	mV	1
V_{IX}(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	2

Note:

1. Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 ±250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/ns.
2. The relation between V_{IX} Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + V_{IX}(Min) – VSEL ≥ 25mV
   VSEH- ((VDD/2) + V_{IX}(Max)) ≥ 25mV

7.5 Slew Rate Definitions for Single-Ended Input Signals

See section 12.5 “Address/Command Setup, Hold and Derating” single-ended slew rate definitions for address and command signals.

See section 12.6.1 “Data Setup, Hold and Slew Rate Derating” single-ended slew rate definitions for data signals.

7.6 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK#, and DQS, DQS#) are defined and measured as shown in Table 7-9 and Figure 7-5.

Table 7-9. Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK – CK# and DQS – DQS#).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$-$V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge (CK - CK# and DQS – DQS#).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ -$V_{ILdiffmax}$] / DeltaTFdiff

Note:

1. The differential signal (i, e., CK- CK# and DQS – DQS#) must be linear between these thresholds.

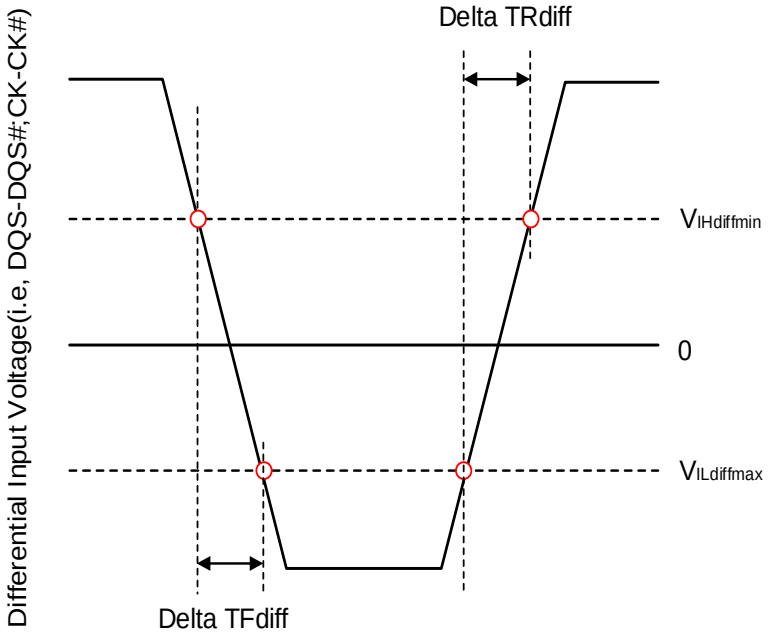


Figure 7-5. Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

8 AC&DC OUTPUT MEASUREMENT LEVELS

8.1 Single Ended AC and DC Output Levels

Table 8-1 shows the output levels used for measurements of single ended signals.

Table 8-1. Single-ended AC&DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2.

8.2 Differential AC and DC Output Levels

Table 8-2 shows the output levels used for measurements of differential signals.

Table 8-2. Differential AC&DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-0.2 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

8.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 8-3 and Figure 8-1.

Table 8-3. Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$- $V_{OL(AC)}$] / Delta TRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$- $V_{OL(AC)}$] / Delta TFse

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

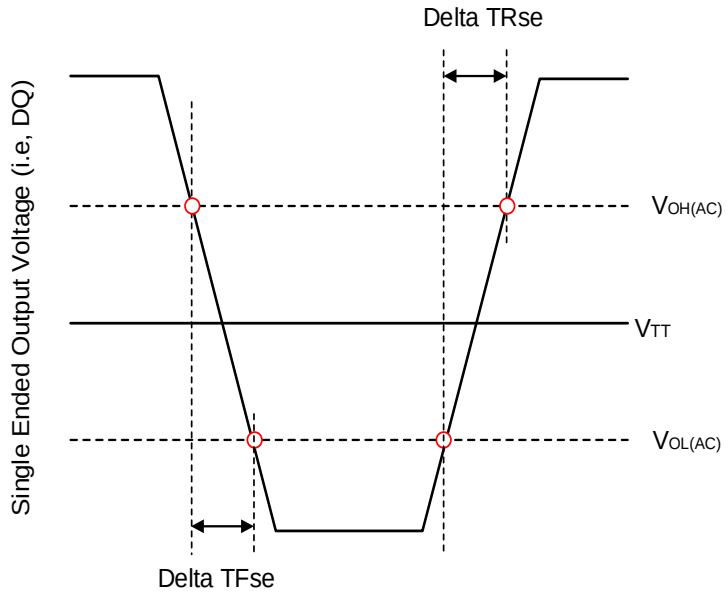


Figure 8-1. Single-ended Output Slew Rate Definition

Table 8-4. Single-ended Output Slew Rate

Parameter	Symbol	Operation Voltage	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	1.35 V	1.75	5[1]	1.75	5[1]	1.75	5[1]	1.75	5[1]	1.75	5[1]	1.75	5[1]	V/ns
		1.5 V	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5[1]	2.5	5[1]	V/ns

Description:

SR: Slew Rate;

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Singnals;

For RON = RZQ/7 setting

Note:

1. In two cases, a maximum slew rate of 6 V/ns applies for a single DQ signal within a byte lane.
   - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
   - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies).

8.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ for differential signals as shown in Table 8-5 and Figure 8-2.

Table 8-5. Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	[$V_{OHdiff(AC)}$- $V_{OLdiff(AC)}$] / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	[$V_{OHdiff(AC)}$- $V_{OLdiff(AC)}$] / Delta TFdiff

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

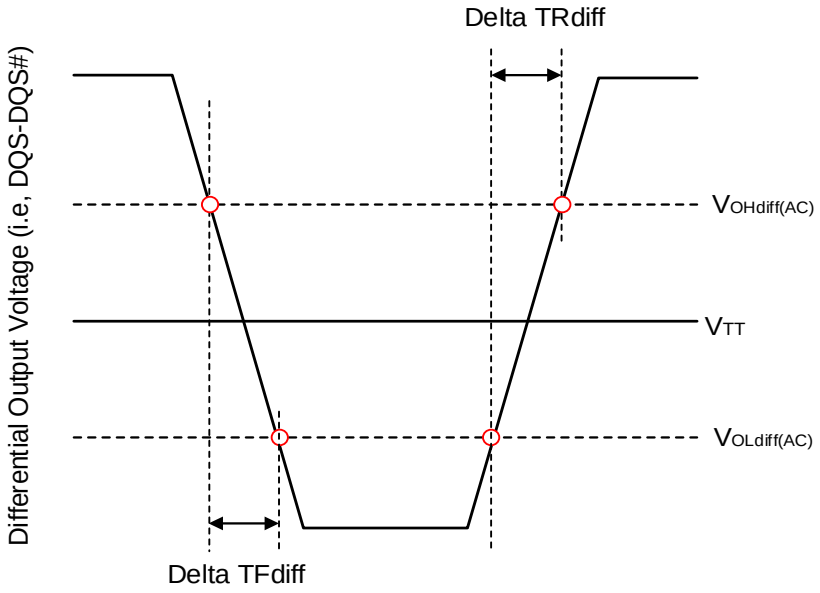


Figure 8-2. Differential Output Slew Rate Definition

Table 8-6. Differential Output Slew Rate

Parameter	Symbol	Operation Voltage	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQdiff	1.35 V	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns
		1.5 V	5	10	5	10	5	10	5	10	5	12	5	12	V/ns

Description:

SR: Slew Rate;

Q: Query Output (like in DQ, which stands for Data-in, Query-Output);

Diff: Differential Singnals;

For RON = RZQ/7 setting

8.5 Reference Load for AC Timing and Output Slew Rate

Figure 8-3 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

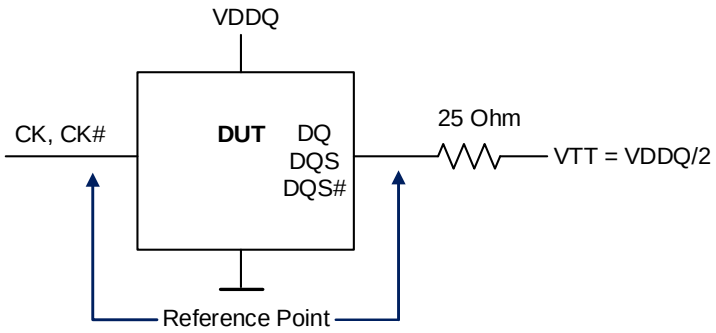


Figure 8-3. Reference Load for AC Timing and Output Slew Rate

8.6 Overshoot and Undershoot Specifications

8.6.1 Address and Control Overshoot and Undershoot Specifications

Table 8-7. AC Overshoot/Undershoot Specification for Address and Control Pins

	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Units
Maximum peak amplitude allowed for overshoot area.[1]	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.[2]	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
Maximum undershoot area below VSS	0.67	0.5	0.4	0.33	0.28	0.25	V-ns
(A0-A14, BA0-BA3, CS#, RAS#, CAS#, WE#, CKE, ODT)							

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not toexceed absolute maximum DC ratings

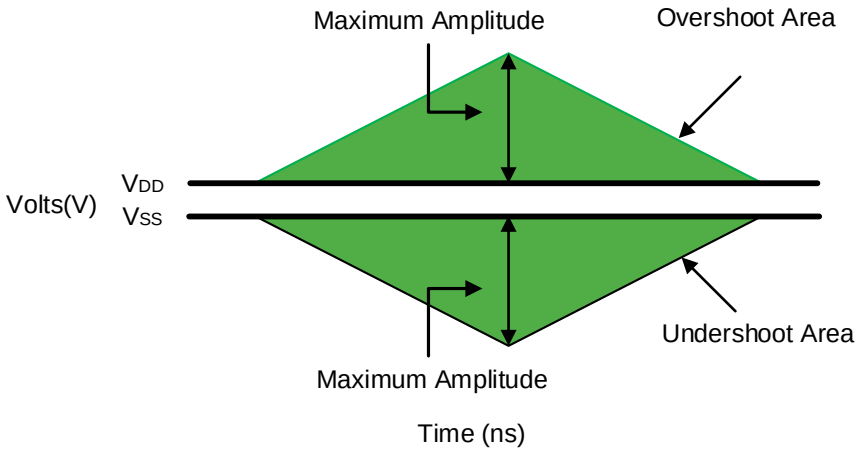


Figure 8-4. Address and Control Overshoot and Undershoot Definition

8.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Table 8-8. AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Units
Maximum peak amplitude allowed for overshoot area.[1]	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.[2]	0.4	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
Maximum undershoot area below VSSQ	0.25	0.19	0.15	0.13	0.11	0.10	V-ns
(CK,, CK#, DQ, DQS, DQS#, DM)							

Note:

1. The sum of the applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of applied voltage (VDD) and the peak amplitude undershoot voltage is not toexceed absolute maximum DC ratings.

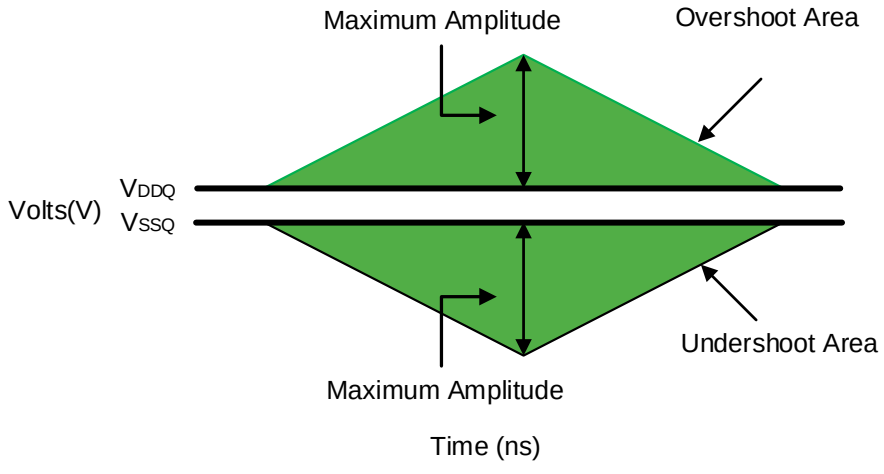


Figure 8-5. Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

8.7 34 Ohm Output Driver DC Electronic Characteristics

A functional representation of the output buffer is shown below. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:

RON_{34}= RZQ/7 (Nominal 34.3 ohms +/- 10% with nominal RZQ=240 Ω)

The individual Pull-up and Pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

RON_{Pu}= VDDQ-Vout ⍰| Iout |⍰ under the condition that RON_{Pd} is turned off

RON_{Pd}= Vout ⍰| Iout |⍰ under the condition that RON_{Pu} is turned off.

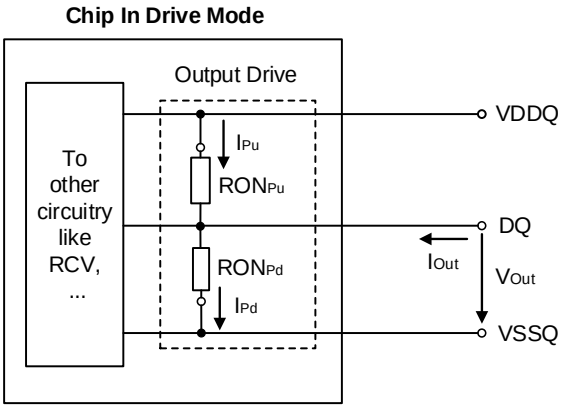


Figure 8-6. Output Driver: Definition of Voltages and Currents

Table 8-9. Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω; entire operating temperature range; after proper ZQ calibration (1.35 V)

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} =0.2 x VDDQ	0.6	1.0	1.15	R_{ZQ}/7	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.15	R_{ZQ}/7	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.9	1.0	1.45	R_{ZQ}/7	1,2,3
	RON_{34Pu}	V_{OLdc} =0.2 x VDDQ	0.9	1.0	1.45	R_{ZQ}/7	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.15	R_{ZQ}/7	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.6	1.0	1.15	R_{ZQ}/7	1,2,3
40 Ω	RON_{40Pd}	V_{OLdc} =0.2 x VDDQ	0.6	1.0	1.15	R_{ZQ}/6	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.15	R_{ZQ}/6	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.9	1.0	1.45	R_{ZQ}/6	1,2,3
	RON_{40Pu}	V_{OLdc} =0.2 x VDDQ	0.9	1.0	1.45	R_{ZQ}/6	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.15	R_{ZQ}/6	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.6	1.0	1.15	R_{ZQ}/6	1,2,3
Mismatch between pull-up and pull-down,MM_{PuPd}		V_{OMdc} =0.5 x VDDQ	-10		+10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance

limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ}=V_{SS}.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
   Measure RON_{Pu} and RON_{Pd}, both at 0.5 * VDDQ:

$$MM\_PuPd = \frac{RON\_Pu - RON\_Pd}{RON\_Nom} x100$$

Table 8-10. Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω; entire operating temperature range; after proper ZQ calibration (1.5 V)

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} =0.2 x VDDQ	0.6	1.0	1.1	R_{ZQ}/7	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.1	R_{ZQ}/7	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.9	1.0	1.4	R_{ZQ}/7	1,2,3
	RON_{34Pu}	V_{OLdc} =0.2 x VDDQ	0.9	1.0	1.4	R_{ZQ}/7	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.1	R_{ZQ}/7	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.6	1.0	1.1	R_{ZQ}/7	1,2,3
40 Ω	RON_{40Pd}	V_{OLdc} =0.2 x VDDQ	0.6	1.0	1.1	R_{ZQ}/6	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.1	R_{ZQ}/6	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.9	1.0	1.4	R_{ZQ}/6	1,2,3
	RON_{40Pu}	V_{OLdc} =0.2 x VDDQ	0.9	1.0	1.4	R_{ZQ}/6	1,2,3
		V_{OMdc} =0.5 x VDDQ	0.9	1.0	1.1	R_{ZQ}/6	1,2,3
		V_{OHdc} =0.8 x VDDQ	0.6	1.0	1.1	R_{ZQ}/6	1,2,3
Mismatch between pull-up and pull-down,MM_{PuPd}		V_{OMdc} =0.5 x VDDQ	-10		+10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ}=V_{SS}.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
   Measure RON_{Pu} and RON_{Pd}, both at 0.5 * VDDQ:

$$MM\_PuPd = \frac{RON\_Pu - RON\_Pd}{RON\_Nom} x100$$

8.7.1 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 8-11 and Table 8-12.

△T = T - T(@calibration); V= VDDQ - VDDQ(@calibration); VDD = VDDQ

Note:

1. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table 8-11. Output Driver Sensitivity Denfinition

Items	Min	Max	Unit
RONPU@ V_{OHdc}	0.6 - $dR_{ON}dTH$*|DT| - $dR_{ON}dVH$*|DV|	1.1 + $dR_{ON}dTH$*|DT| + $dR_{ON}dVH$*|DV|	RZQ/7
RON@ V_{OMdc}	0.9 - $dR_{ON}dTM$*|DT| - $dR_{ON}dVM$*|DV|	1.1 + $dR_{ON}dTM$*|DT| + $dR_{ON}dVM$*|DV|	RZQ/7
RONPD@ V_{OLdc}	0.6 - $dR_{ON}dTL$*|DT| - $dR_{ON}dVL$*|DV|	1.1 + $dR_{ON}dTL$*|DT| + $dR_{ON}dVL$*|DV|	RZQ/7

Table 8-12. Output Driver Voltage and Temperature Sensitivity

Speed Bin	800/1066/1333		1600/1866/2133		Unit
Items	Min	Max	Min	Max	
$dR_{ON}dTM$	0	1.5	0	1.5	%/℃
$dR_{ON}dVM$	0	0.15	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	0	1.5	%/℃
$dR_{ON}dVL$	0	0.15	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	0	1.5	%/℃
$dR_{ON}dVH$	0	0.15	0	0.13	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

8.8 On-die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register.

ODT is applied to the DQ, DM, DQS/DQS# and TDQS, TDQS# (x8 devices only) pins.

A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTT_{Pu} and RTT_{Pd}) are defined asfollows:

RTT_{Pu}= VDDQ-Vout □| Iout |□ under the condition that RTT_{Pd} is turned off

RTT_{Pd}= Vout □| Iout |□ under the condition that RTT_{Pu} is turned off.

Chip In Termination Mode

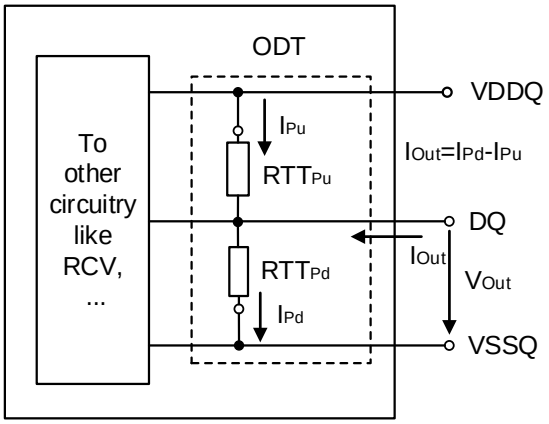


Figure 8-7. On-Die Termination: Definition of Voltages and Currents

8.8.1 ODT DC Electrical Characteristic

Table 8-13 provides and overview of the ODT DC electrical characteristics. Their values for $RTT_{60Pd120}$, $RTT_{60Pu120}$, $RTT_{120Pd240}$, $RTT_{120Pu240}$, RTT_{40Pd80}, RTT_{40Pu80}, RTT_{30Pd60}, RTT_{30Pu60}, RTT_{20Pd40}, RTT_{20Pu40} are not specification requirements, but can be used as design guide lines:

Table 8-13. ODT DC Electristics, assuming RZQ = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 (A9, A6, A2)	RTT	RESISTOR	Vout	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
(0,1,0)	120 Ω	$RTT_{120Pd240}$	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	R_{ZQ}	1,2,3,4
		$RTT_{120Pu240}$	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	R_{ZQ}	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	R_{ZQ}	1,2,3,4
		RTT_{120}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/2$	1,2,5
(0,0,1)	60 Ω	$RTT_{60Pd120}$	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/2$	1,2,3,4
		$RTT_{60Pu120}$	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/2$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/2$	1,2,3,4
		RTT_{60}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/4$	1,2,5
(0,1,1)	40 Ω	RTT_{40Pd80}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/3$	1,2,3,4
		RTT_{40Pu80}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/3$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/3$	1,2,3,4

MR1 (A9, A6, A2)	RTT	RESISTOR	Vout	Min	Nom	Max (DDR3L)	Max (DDR3)	Unit	Note
		RTT_{40}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/6$	1,2,5
(1,0,1)	30 Ω	RTT_{30Pd60}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/4$	1,2,3,4
		RTT_{30Pu60}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/4$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/4$	1,2,3,4
		RTT_{30}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/8$	1,2,5
(1,0,0)	20 Ω	RTT_{20Pd40}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3,4
		RTT_{20Pu40}	$V_{OL(DC)}$ 0.2 x V_{DDQ}	0.9	1.0	1.45	1.4	$R_{ZQ}/6$	1,2,3,4
			0.5 x V_{DDQ}	0.9	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
			$V_{OH(DC)}$ 0.8 x V_{DDQ}	0.6	1.0	1.15	1.1	$R_{ZQ}/6$	1,2,3,4
		RTT_{20}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.65	1.6	$R_{ZQ}/12$	1,2,5
Deviation of V_Mw.r.t V_{DDQ}/2, △VM				-5	-	+5	+5	%	+5

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ}= V_{DD} and that V_{SSQ}= V_{SS}
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x V_{DDQ} and 0.8 x V_{DDQ}.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
   Apply V_{IH}(AC) to pin under test and measure current I(V_{IH}(AC)), then apply V_{IL}(AC) to pin under test and measure current I(V_{IL}(AC)) respectively.

$$RTT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

6. Measurement definition for VM and △VM: Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1\right) \times 100$$

8.8.2 ODT DC Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 8-14 and Table 8-15.

△T = T - T(@calibration); △V = V_{DDQ}- V_{DDQ}(@calibration); V_{DD}= V_{DDQ}

Table 8-14. ODT Sensitivity Definition

	Min	Max	Unit
RTT	0.9 - $dR_{TT}dT$ * |△T| - $dR_{TT}dV$ * |△V|	1.6 + $dR_{TT}dT$ * |△T| + $dR_{TT}dV$ * |△V|	RZQ/2,4,6,8,12

Table 8-15. ODT Voltage and Temperature Sensitivity

	Min	Max	Unit

$dR_{TT}dT$	0	1.5	%/℃
$dR_{TT}dV$	0	0.15	%/mV

Note:

1. These parameters may not be subject to production test. They are verified by design and characterization.

8.9 ODT Timing Definitions

8.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 8-8.

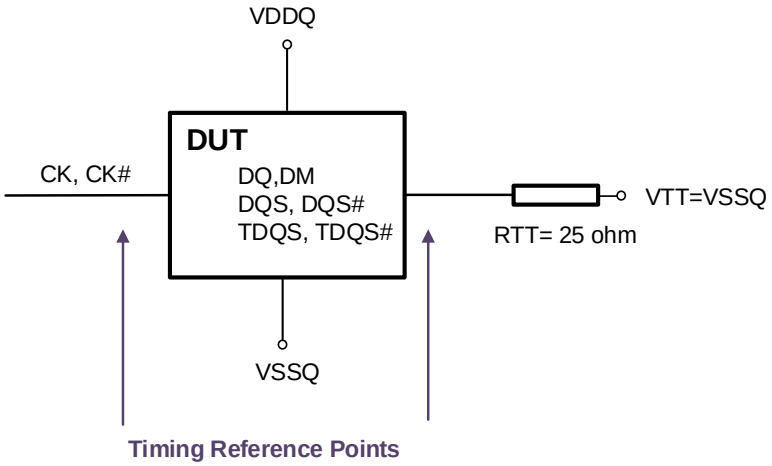


Figure 8-8. ODT Timing Reference Load

8.9.2 ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD} and t_{ADC} are provided in Table 8-16 and subsequent figures. Measurement reference settings are provided in Table 8-17.

Table 8-16. ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK –CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 8-9
t_{AONPD}	Rising edge of CK –CK# with ODT being first registered high	Extrapolated point at V_{SSQ}	Figure 8-10
t_{AOF}	Rising edge of CK –CK# defined by the end point of ODTLoff	End point: Extrapolated point at V_{RTT_Nom}	Figure 8-11
t_{AOFPD}	Rising edge of CK –CK# with ODT being first registered low	End point: Extrapolated point at V_{RTT_Nom}	Figure 8-12
t_{ADC}	Rising edge of CK –CK# defined by the end point of ODTLcnw, ODTLcwn4 of ODTLcwn8	End point: Extrapolated point at V_{RTT_Wr} and V_{RTT_Nom} respectively	Figure 8-13

Table 8-17. Reference Settings for ODT Timing Measurements

Measured Parameter		RTT_Nom Setting	RTT_Wr Setting	V_{SW1}[V]	V_{SW2}[V]
t_{AON}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AONPD}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AOF}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{AOFPD}		$R_{ZQ}/4$	NA	0.05	0.10
		$R_{ZQ}/12$	NA	0.10	0.20
t_{ADC}	DDR3L(1.35 V)	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.25
	DDR3(1.5 V)	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30

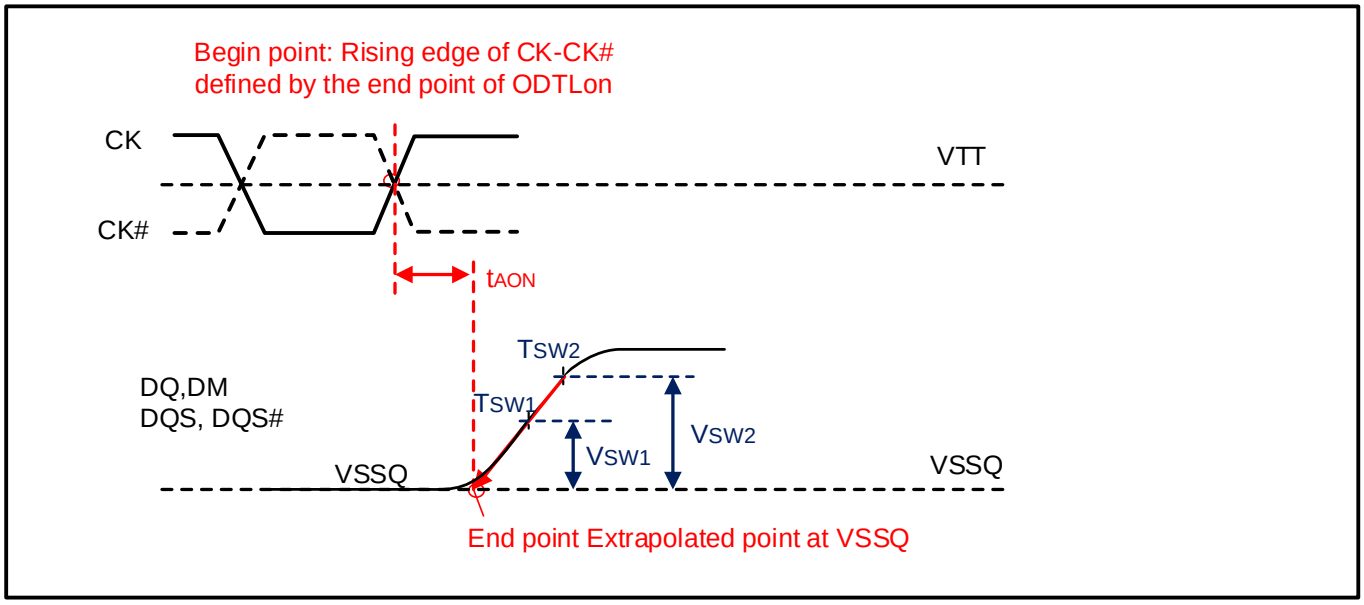


Figure 8-9. Definition of t_{AON}

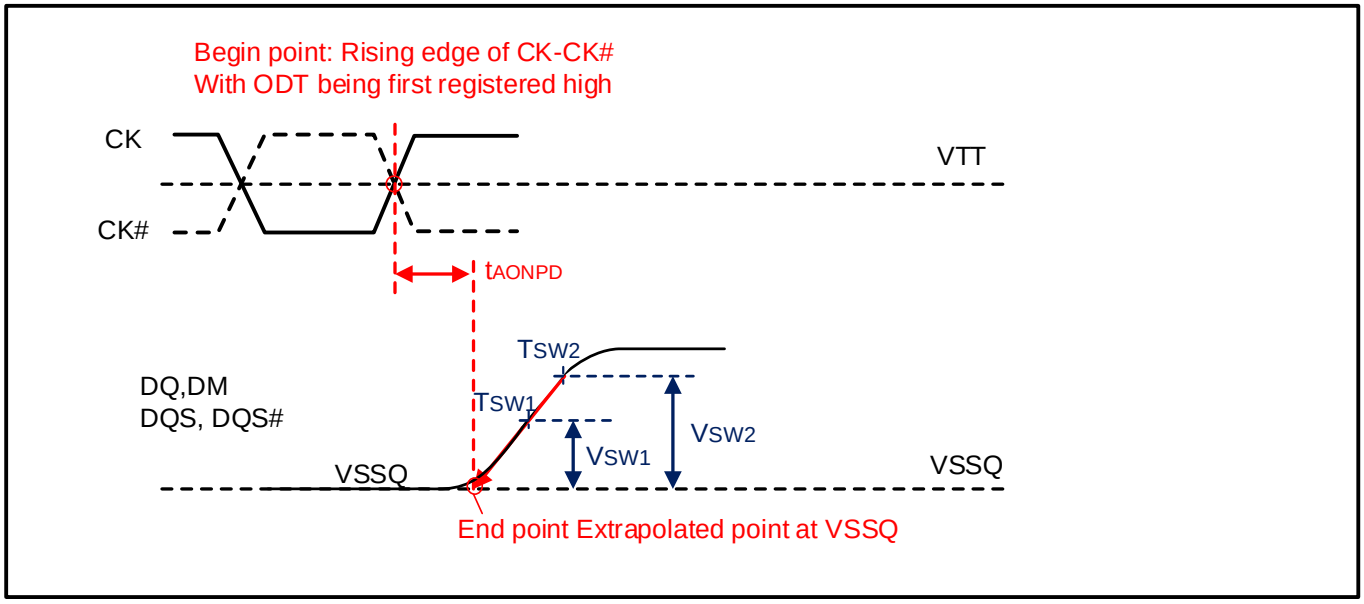


Figure 8-10. Definition of t_{AONPD}

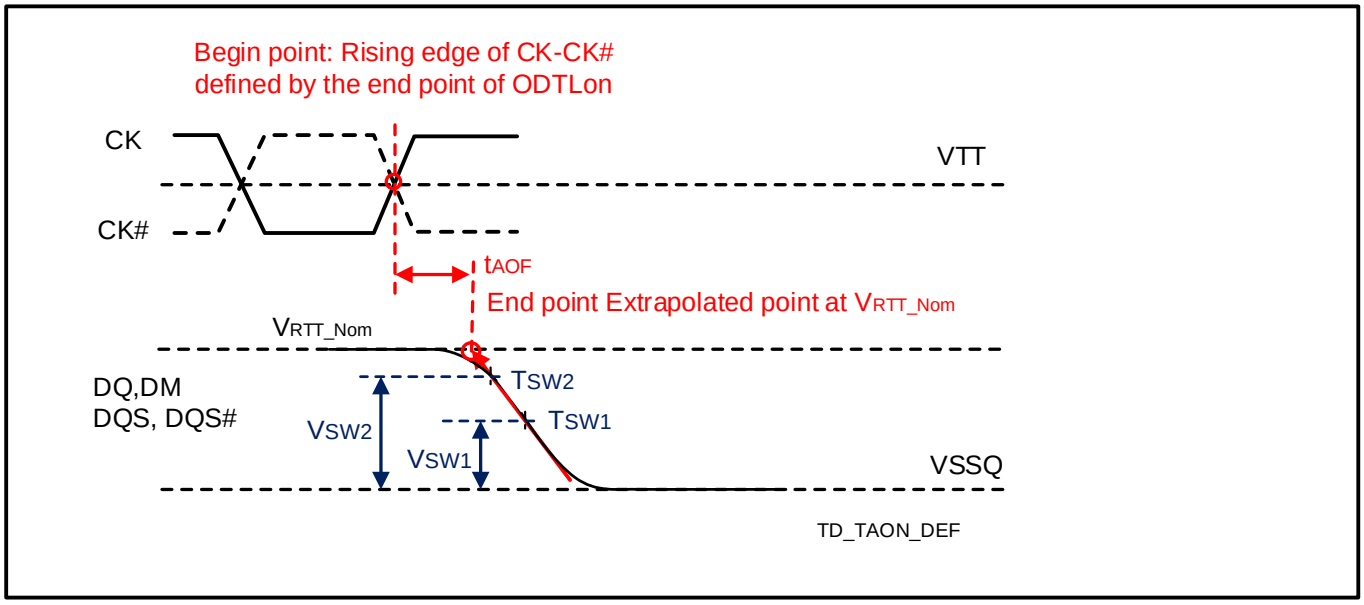


Figure 8-11. Definition of t_{AOF}

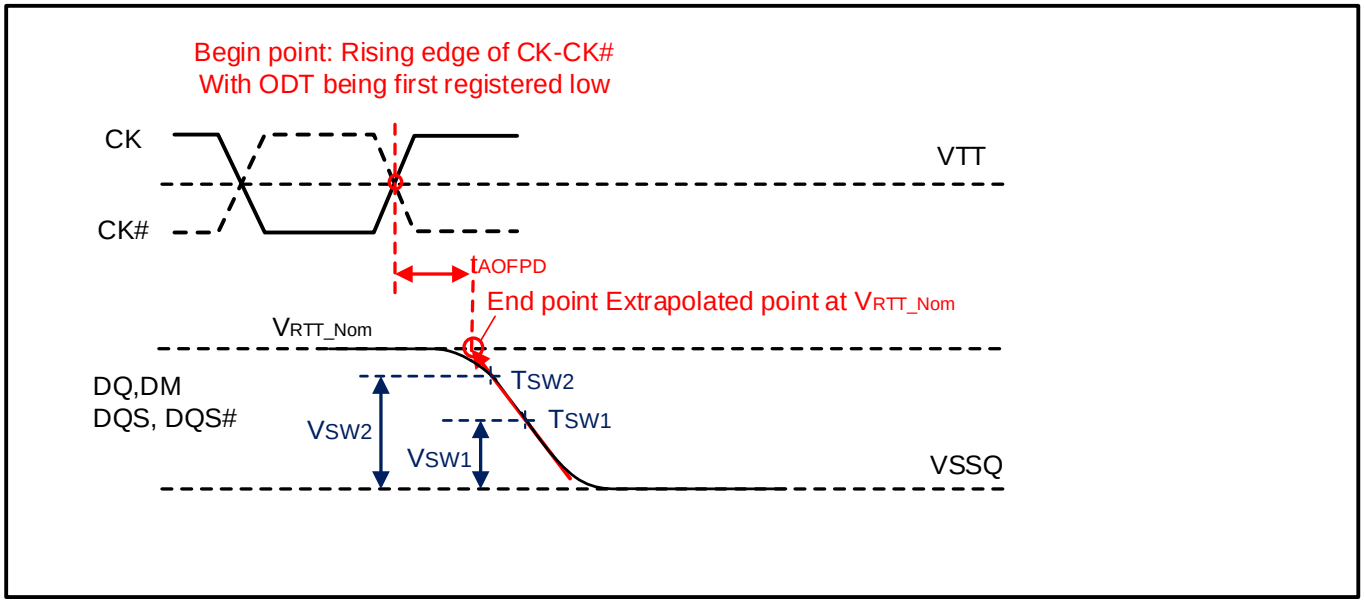


Figure 8-12. Definition of t_{AOFPD}

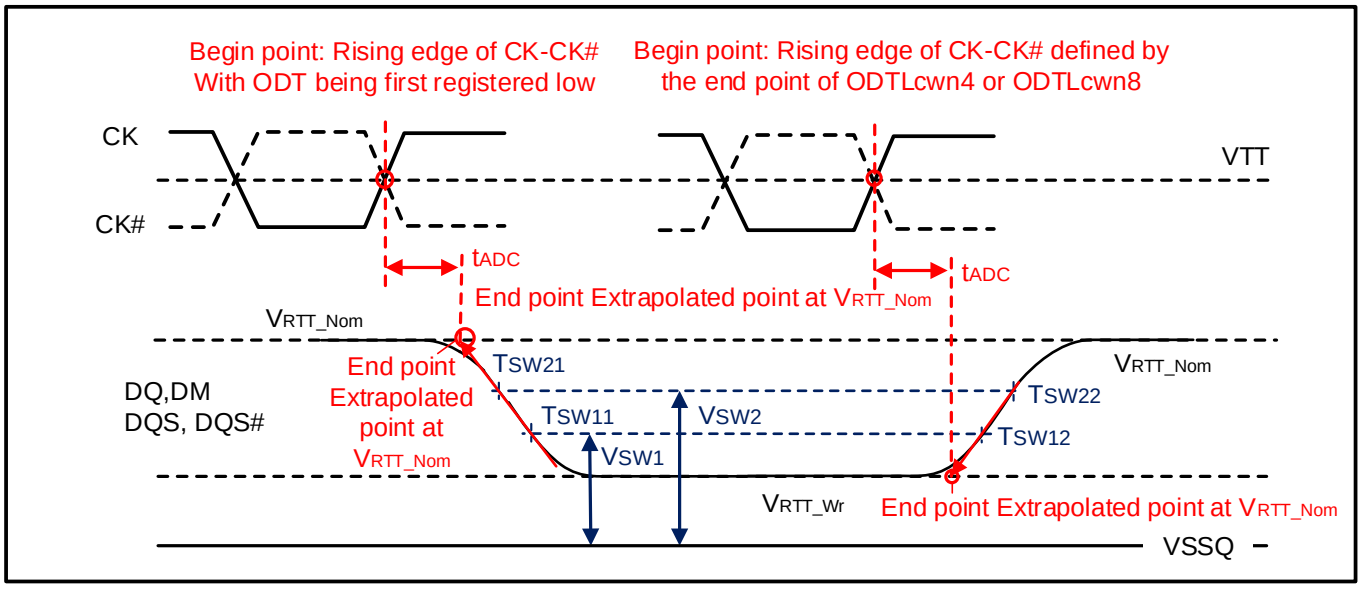


Figure 8-13. Definition of t_{ADC}

9 IDD CURRENT MEASURE METHOD

9.1 IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

Figure 9-1 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 9-2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN<= VILAC(max).
- "1" and "HIGH" is defined as VIN>= VIHAC(min).
- "FLOATING" is defined as inputs are VREF= VDD/ 2.
- "Timing used for IDD and IDDQ Measured - Loop Patterns" are provided in Table 6-1.
- "Basic IDD and IDDQ Measurement Conditions" are described in Table 9-3.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 9-4 through Table 9-11.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- **Attention**: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS#, RAS#, CAS#, WE#}: = {HIGH, LOW, LOW, LOW}
- Define D# = {{CS#, RAS#, CAS#, WE#}: = {HIGH, HIGH, HIGH, HIGH}

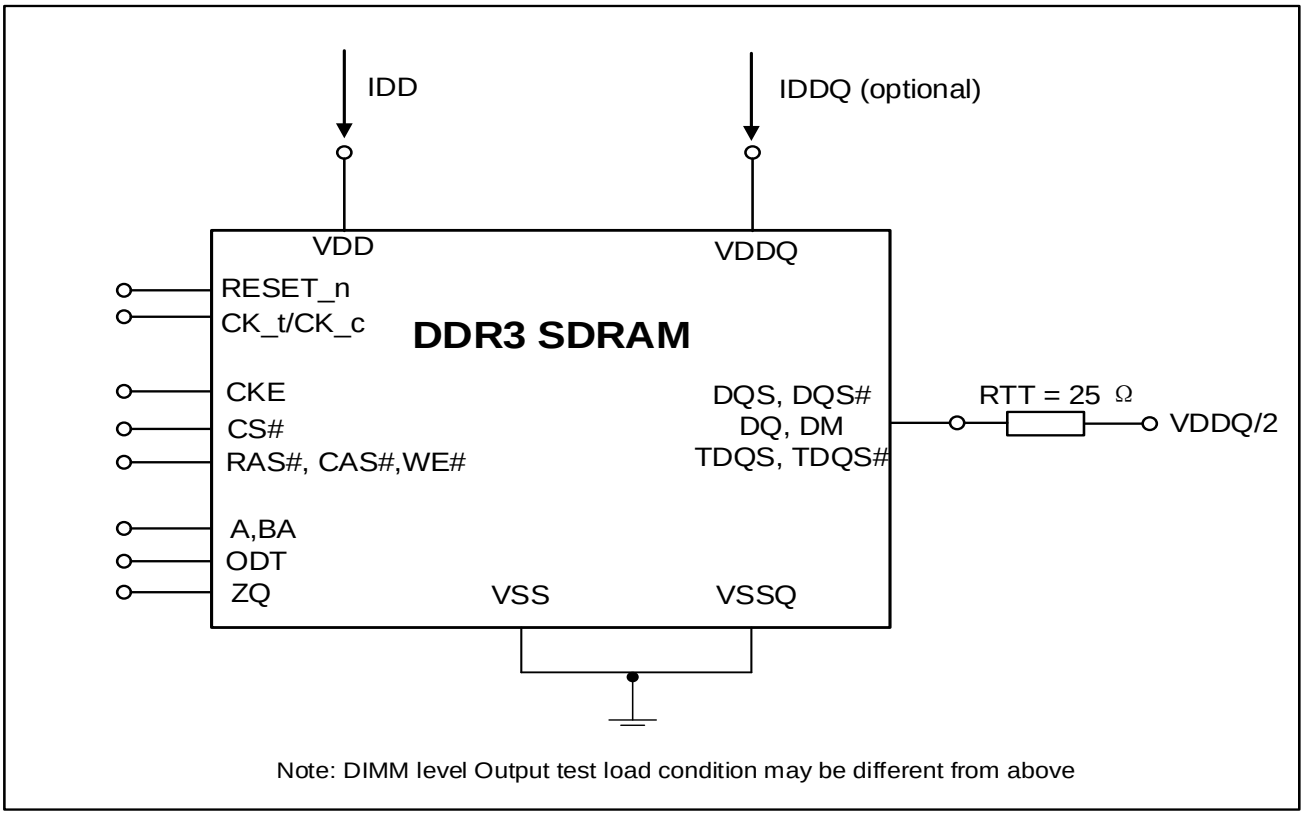


Figure 9-1. Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements

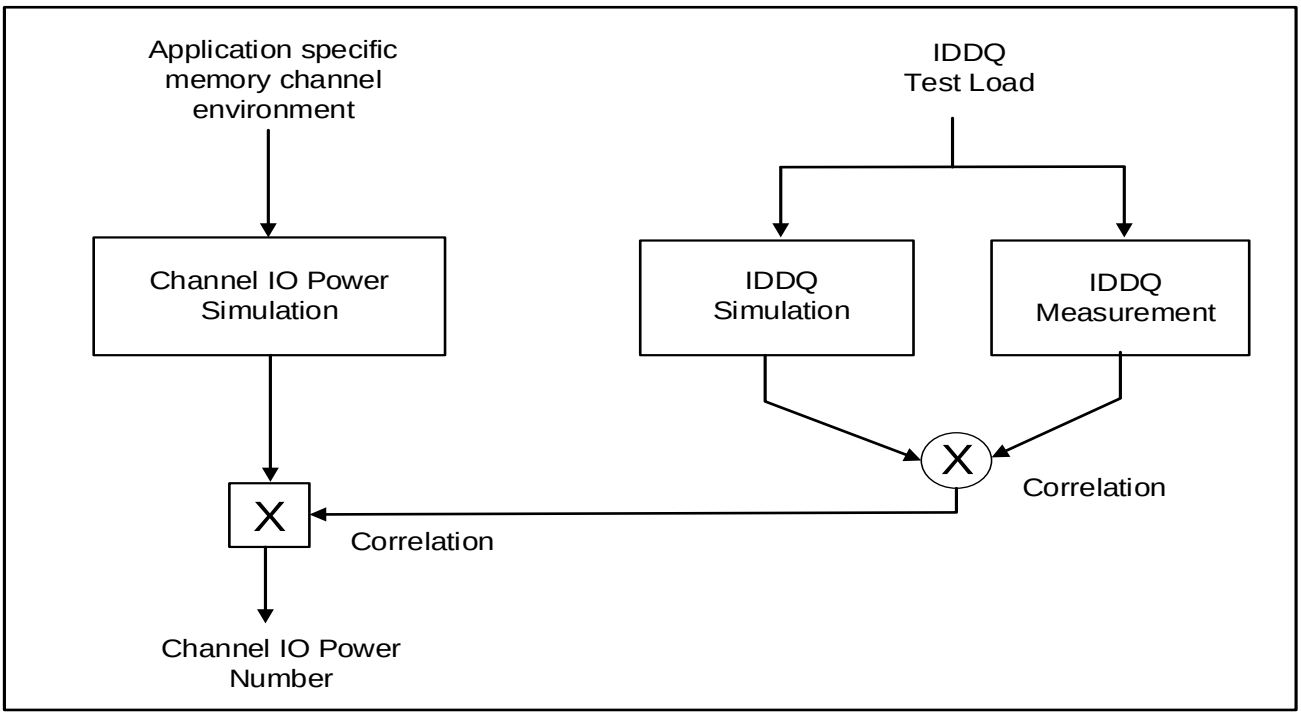


Figure 9-2. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 9-1. Timing used for IDD and IDDQ Measured-Loop Patterns for 1333/1600

Symbol		DDR3L-1333				DDR3L-1600				Unit
		7-7-7	8-8-8	9-9-9	10-10-10	8-8-8	9-9-9	10-10-10	11-11-11	
tCK		1.5				1.25				ns
CL		7	8	9	10	8	9	10	11	nCK
nRCD		7	8	9	10	8	9	10	11	nCK
nRC		31	32	33	34	36	37	38	39	nCK
nRAS		24				28				nCK
nRP		7	8	9	10	8	9	10	11	nCK
nFAW	1KB page size	20				24				nCK
	2KB page size	30				32				nCK
nRRD	1KB page size	4				5				nCK
	2KB page size	5				6				nCK
nRFC 512 Mb		60				72				nCK
nRFC 1 Gb		74				88				nCK
nRFC 2 Gb		107				128				nCK
nRFC 4 Gb		174				208				nCK
nRFC 8 Gb		234				280				nCK

Table 9-2. Timing used for IDD and IDDQ Measured-Loop Patterns for 1866/2133

Symbol		DDR3L-1866				DDR3L-2133				Unit
		10-10-10	11-11-11	12-12-12	13-13-13	11-11-11	12-12-12	13-13-13	14-14-14	
tCK		1.071				0.938				ns
CL		10	11	12	13	11	12	13	14	nCK
nRCD		10	11	12	13	11	12	13	14	nCK
nRC		42	43	44	45	47	48	49	50	nCK
nRAS		32				36				nCK
nRP		10	11	12	13	11	12	13	14	nCK
nFAW	1KB page size	26				27				nCK
	2KB page size	33				38				nCK
nRRD	1KB page size	5				6				nCK
	2KB page size	6				7				nCK
nRFC 512 Mb		85				97				nCK
nRFC 1 Gb		103				118				nCK
nRFC 2 Gb		150				172				nCK
nRFC 4 Gb		243				279				nCK
nRFC 8 Gb		328				375				nCK

Table 9-3. Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** see Table 9-2; **BL:** 8(1); **AL:** 0; **CS#:** High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-4; **Data IO:** MID-LEVEL; **DM**: stable at 0; **Bank Activity**: Cycling with one bank active at a time: 0,0,1,1,2,2, ... (see Table 9-4); **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal**: stable at 0; **Pattern Details**:see Table 9-4
IDD1	**Operating One Bank Active-Precharge Current** **CKE:** High; **External clock:** On**;** **tCK, nRC, nRAS, nRCD, CL:** see Table 9-1; **BL:**8(1,7); **AL:**0**;** **CS#:** High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling according toTable 9-5; **DM:** stable at 0; **Bank Activity:** Cycling with one bank activeat a time: 0,0,1,1,2,2, … (see Table 9-5); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 9-5
IDD2N	**Precharge Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-6 **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 9-6
IDD2NT	**Precharge Standby ODT Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-7; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** toggling according to Table 9-7; **Pattern Details:** Table 9-7;
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current

Symbol	Description
IDD2P0	**Precharge Power-Down Current Slow Exit** **CKE:** Low; **External clock:** On; **tCK, CL;** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0 **Pecharge Power Down Mode:** Slow Exit(3)
IPP2P1	**Precharge Power-Down Current Fast Exit** **CKE:** Low; **External clock:** On; **tCK, CL;** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0 **Pecharge Power Down Mode:** Fast Exit(3)
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-6; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 9-6

Symbol	Description
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-6; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** stable at 0
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1,7); **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-8; **Data IO:** seamless read data burst with differentdata between one burst and the next one according to Table 9-8; **DM:** stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2, ... (see Table 9-8); **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 9-8
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-9; **Data IO:** seamless read data burst with differentdata between one burst and the next one according to Table 9-9; **DM:** stable at 0; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2, ... (see Table 9-9); **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** stable at HIGH; **Pattern Details:** seeTable 9-9

Symbol	Description
IDD5B	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL nRFC:** see Table 9-1; **BL:** 8(1); **AL:** 0; **CS#**: High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-10; **Data IO:** MID-LEVEL**;** **DM:** stable at 0; **Bank Activity:** REF command every nRFC (see Table 9-10); **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details**: see Table 9-10
IDD6	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **Auto Self-Refresh (ASR)**: Disabled(4); **Self-Refresh Temperature Range (SRT)**: Normal(5); **CKE**: Low; **External clock**: Off; **CK and CK#**: LOW; **CL**: see Table 9-1; **BL**:8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL**;** **DM:** stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL
IDD6ET	**Self-Refresh Current: Extended Temperature Range** ***T*CASE:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Disabled(4); **Self-Refresh Temperature Range (SRT)**: Extended(5); **CKE**: Low; **External clock**: Off; **CK and CK#**: LOW; **CL**: see Table 9-1; **BL**:8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL**;** **DM:** stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL

Symbol	Description
IDD6TC	**Auto Self-RefreshCurrent (optional)**[6] ***T*CASE:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Enabled[4]; **Self-Refresh Temperature Range (SRT)**: Normal[5]; **CKE**: Low; **External clock**: Off; **CK and CK#**: LOW; **CL**: see Table 9-1; **BL**:8[1]; **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT**: Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** see Table 9-1; **BL:** 8[1]; **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling according to Table 9-11; **Data IO:** Read data bursts with different data between one burst and the next one according to Table 9-11; **DM:** stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 9-11; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 9-11.
IDD8 (Optional)	**RESET Low Current** **RESET:** Low; **External clock:** Off; **CK and CK#:** Low; **CKE:** FLOATING; **CS#, Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.

Note:

1. Burst Length: BL8 fixedby MRS: set MR0 A[1,0] =00B
2. Output Buffer Enable: set MR1 A[12] =0B; set MR1 A[5,1]=01B; RTT_Nom enable: set MR1 A[9,6,2]=011B; RTT_Wr enable: set MR2 A[10,9]=10B
3. Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 =0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
7. Read Burst Type: Nibble Sequential, set MR0 A[3]=0B

Table 9-4. IDD0 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D_#,D_#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1…4 unit nRAS -1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			…	repeat pattern 1…4 unit nRC -1, truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3,4	D_#,D_#	1	1	1	1	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 unit 1* nRC + nRAS -1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			…	repeat nRC + 1…4 unit 2* nRC -1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 9-5. IDD1 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D_#,D_#	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1…4 unit nRCD -1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			…	repeat pattern 1…4 unit nRAS -1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			…	repeat pattern 1…4 unit nRC -1, truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3,4	D_#,D_#	1	1	1	1	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 unit nRC + nRCD -1, truncate if necessary												
			1*nRC + nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
				repeat pattern nRC + 1…4 unit nRC + nRAS -1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			…	repeat pattern nRC + 1…4 unit 2* nRC -1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:

1. DM must be driven LOW all thetime. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9-6. IDD2N and IDD3N Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D#	1	1	1	1	0	0	0	0	0	F	0	-
			3	D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-27	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 9-7. IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D#	1	1	1	1	0	0	0	0	0	F	0	-
			3	D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 9-8. IDD4R and IDDQ4R Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	
			6,7	D#, D#	1	1	1	1	0	0	00	0	0	F	0	
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9-9. IDD4W Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	
			6,7	D#, D#	1	1	1	1	1	0	00	0	0	F	0	
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to WR Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by WriteCommand. Outside burst operation, DQ signals are MID-LEVEL.

Table 9-10. IDD5B Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
		1	1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			5…8	repeat cycles 1…4, but BA[2:0] = 1												
			9…12	repeat cycles 1…4, but BA[2:0] = 2												
			13…16	repeat cycles 1…4, but BA[2:0] = 3												
			17…20	repeat cycles 1…4, but BA[2:0] = 4												
			21…24	repeat cycles 1…4, but BA[2:0] = 5												
			25…28	repeat cycles 1…4, but BA[2:0] = 6												
			29…32	repeat cycles 1…4, but BA[2:0] = 7												
		2	33…nRFC-1	repeat Sub-Loop 1, unit nRFC -1. Truncate, if necessary.												

Note:

1. DM must be driven Low all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 9-11. IDD7 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			…	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			…	repeat above D Command until 2 * nRRD -1												
		2	2* nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3* nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4* nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW + nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW + 2* nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW + 3* nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW + 4* nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2 * nFAW - 1, if necessary												
		10	2* nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
			2* nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2* nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2 * nFAW + nRRD - 1												
		11	2*nFAW + nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW + nRRD +1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW + nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				repeat above D Command until 2 * nFAW + 2 * nRRD -1												
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 10, butBA[2:0] = 2												
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 11, butBA[2:0] = 3												
		14	2*nFAW + 4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3 * nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, butBA[2:0] = 4												
		16	3*nFAW + nRRD	repeat Sub-Loop 11, butBA[2:0] = 5												
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 10, butBA[2:0] = 6												
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 11, butBA[2:0] = 7												
		19	3*nFAW + 4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4 * nFAW - 1, if necessary												

Note:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

9.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 9-12. I_{DD} Specifications (1.35 V)

Speed Grade Bin	DDR3L-1866	DDR3L-2133	Unit	Notes
Symbol	Max.	Max.		
I_{DD0}	88	92	mA	x16
I_{DD1}	132	138	mA	x16
$I_{DD2P(0)}$ slow exit	28	30	mA	x16
$I_{DD2P(1)}$ fast exit	32	34	mA	x16
I_{DD2N}	52	56	mA	x16
I_{DD2NT}	55	58	mA	x16
I_{DD2Q}	50	54	mA	x16
I_{DD3P}(fast exit)	52	55	mA	x16
I_{DD3N}	72	76	mA	x16
I_{DD4R}	268	297	mA	x16
I_{DD4W}	256	280	mA	x16
I_{DD5B}	348	342	mA	x16
I_{DD6}	16	16	mA	x16
I_{DD7}	329	340	mA	x16
I_{DD8}	14	14	mA	x16

Note:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3L SDRAM devices support the following options or requirementsreferred to in this material.
2. Some data retains the possibility of future updates.

Table 9-13. I_{DD} Specifications (1.5 V)

Speed Grade Bin	DDR3L-1866	DDR3L-2133	Unit	Notes
Symbol	Max.	Max.		
I_{DD0}	90	94	mA	x16
I_{DD0}	135	140	mA	x16
$I_{DD2P(0)}$ slow exit	28	31	mA	x16
$I_{DD2P(1)}$ fast exit	32	35	mA	x16
I_{DD2N}	54	58	mA	x16
I_{DD2NT}	57	60	mA	x16
I_{DD2Q}	52	55	mA	x16
I_{DD3P}(fast exit)	52	57	mA	x16
I_{DD3N}	73	78	mA	x16
I_{DD4R}	271	301	mA	x16
I_{DD4W}	260	284	mA	x16
I_{DD5B}	351	345	mA	x16
I_{DD6}	16	16	mA	x16
I_{DD7}	335	347	mA	x16
I_{DD8}	14	14	mA	x16

Note:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirementsreferred to in this material.
2. Some data retains the possibility of future updates.

10 INPUT/OUTPUT CAPACITANCE

10.1 Input/Output Capacitance

Table 10-1. DDR3L/DDR3-800/1066/1333/1600 Input/Output Capacitance

Symbol	Parameter		800		1066		1333		1600		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM,DQS, DQS#, TDQS, TDQS#)	DDR3 (1.5 V)	1.4	3.0	1.4	2.7	1.4	2.5	1.4	2.3	pF	1,2,3
		DDR3L (1.35 V)	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2		
C_{CK}	Input capacitance, CK and CK#		0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta DQS and DQS#		0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance, (CTRL, ADD,CMD input-only pins)	DDR3 (1.5 V)	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	2,3,6
		DDR3L (1.35 V)	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2		
C_{DI_CTRL}	Input capacitance delta, (All CTRLinput-only pins)		-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta, (All ADD/CMD input-only pins)		-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
C_{DIO}	Input/output capacitance delta, DQ,DM, DQS, DQS#, TDQS, TDQS#		-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	-	3	-	3	pF	2,3,12

Note:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance ismeasured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VEC-TOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT

as necessary). VDD=VDDQ=1.35V, VBIAS=VDD/2 and on-die termination off.

3. This parameter applies tomonolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#
5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS#)
6. C_I applies to ODT, CS#, CKE, A0-A14, BA0-BA2, RAS#, CAS#, WE#。
7. C_{DI_CTRL} applies to ODT, CS# and CKE
8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CLK)+C_I(CLK#))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A14, BA0-BA2, RAS#, CAS# and WE#。
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(CLK#))
11. C_{DIO}=C_{IO}(DQ, DM) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

Table 10-2. DDR3L/DDR3-1866/2133 Input/Output Capacitance

Symbol	Parameter		1866		2133		Unit	Note
			Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM,DQS, DQS#, TDQS, TDQS#)	DDR3 (1.5 V)	1.4	2.2	1.4	2.1	pF	1,2,3
		DDR3L (1.35 V)	1.4	2.1	-	-		
C_{CK}	Input capacitance, CK and CK#		0.8	1.3	0.8	1.3	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta DQS and DQS#		0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance, (CTRL, ADD,CMD input-only pins)	DDR3 (1.5 V)	0.75	1.2	0.75	1.2	pF	2,3,6
		DDR3L (1.35 V)	0.75	1.2	-	-		
C_{DI_CTRL}	Input capacitance delta, (All CTRLinput-only pins)		-0.4	0.2	-0.4	0.2	pF	2,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta, (All ADD/CMD input-only pins)		-0.4	0.4	-0.4	0.4	pF	2,3,9,10
C_{DIO}	Input/output capacitance delta, DQ,DM, DQS, DQS#, TDQS, TDQS#		-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	pF	2,3,12

Note:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance ismeasured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VEC-TOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.35V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies tomonolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#
5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS#)
6. C_I applies to ODT, CS#, CKE, A0-A14, BA0-BA2, RAS#, CAS#, WE#。
7. C_{DI_CTRL} applies to ODT, CS# and CKE
8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CLK)+C_I(CLK#))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A14, BA0-BA2, RAS#, CAS# and WE#。
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(CLK#))
11. C_{DIO}=C_{IO}(DQ, DM) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

11 ELECTRONICAL CHARACTERISTICS AND TIMING FOR DDR3L-800 TO DDR3L-2133

11.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/maxvalues may result in malfunction of the DDR3L SDRAM device.

11.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where eachclock period is calculated fromrising edge to rising edge.

tCK(avg)=(j=1□N□tCKj) / N□ N=200

11.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edgeto the next consecutiverising edge. tCK(abs) is not subject to production test.

11.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

tCH(avg)=(j=1□N□tCHj) / (N×tCK(avg))□ N=200

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCL(avg)=(j=1□N□tCLj) / (N×tCK(avg))□ N=200

11.1.4 Definition for tJIT(per) and tJIT (per, lck)

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCK_i- tCK(avg) where i = 1 to 200}.

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per, lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT (per, lck) are not subject to production test.

11.1.5 Definition for tJIT(cc) and tJIT (cc, lck)

tJIT(cc) is defined as the absolute differencein clock period between two consecutive clock cycles.

tJIT(cc) = Max of | {tCK_{i+1}- tCK_i} |.

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT (cc, lck) are not subject to production test.

11.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is notsubject to production test.

11.2 Refresh parameters by device density

Table 11-1. Refresh parameters by device density

Parameter	Symbol		2Gb	Units	Notes
REF command to ACT or REF command time	tRFC		160	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	µs	
		85 °C < T_{CASE} ≤ 95 °C	3.9	µs	1

Note:

1. Users should refer to the DRAM supplier datasheet and/or the DIMM SPD to determine if DDR3L SDRAM devices support the following options or requirements referred to in this material.

11.3 Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

Table 11-2. DDR3L/DDR3-800 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-800D		DDR3L/DDR3-800E		Unit	Notes
CL-nRCD-nRP			5-5-5		6-6-6			
Parameter		Symbol	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	12.5	20	15	20	ns	
ACT to internal Read or write delay time		t_{RCD}	12.5	-	15	-	ns	
PRE command period		t_{RP}	12.5	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	50	-	52.5	-	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	3.0	3.3	ns	1,2,3,4,12,13
CL =6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1,2,3
Supported CL Settings			5,6		5,6		n_{CK}	13
Supported CWL Settings			5		5		n_{CK}	

Table 11-3. DDR3L/DDR3-1066 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-1066E		DDR3L/DDR3-1066F		DDR3L/DDR3-1066G		Unit	Notes
CL-nRCD-nRP			6-6-6		7-7-7		8-8-8			
Parameter		Symbol	Min	Max	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal Read or write delay time		t_{RCD}	11.25	-	13.125	-	15	-	ns	
PRE command period		t_{RP}	11.25	-	13.125	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	48.75	-	50.625	-	52.5	-	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	3.0	3.3	3.0	3.3	ns	1,2,3,4,6,12,13
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4
CL =7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3
Supported CL Settings			5,6,7,8		5,6,7,8		5,6,8		n_{CK}	13
Supported CWL Settings			5,6		5,6		5,6		n_{CK}	

Table 11-4. DDR3L/DDR3-1333 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-1333F (optional)		DDR3L/DDR3-1333G		DDR3L/DDR3-1333H		DDR3L/DDR3-1333J (optional)		Unit	Notes
CL-nRCD-nRP			7-7-7		8-8-8		9-9-9		10-10-10			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	10.5	20	12	20	13.5 (13.125) [5,11]	20	15	20	ns	
ACT to internal Read or write delay time		t_{RCD}	10.5	-	12	-	13.5 (13.125) [5,11]	-	15	-	ns	
PRE command period		t_{RP}	10.5	-	12	-	13.5 (13.125) [5,11]	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	46.5	-	48	-	49.5 (49.125) [5,11]	-	51	-	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	3.0	3.3	3.0	3.3	ns	1,2,3,4, 7,12,13
	CWL = 6,7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4, 7
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL =7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875 (Optional)[5,11]	< 2.5	Reserved		ns	1,2,3,4, 7
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	Reserved		ns	1,2,3,4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5,6,7,8,9,(10)		5,6,7,8,9,(10)		5,6,8,(7),9,(10)		5,6,8,10		n_{CK}	
Supported CWL Settings			5,6,7		5,6,7		5,6,7		5,6,7		n_{CK}	

Table 11-5. DDR3L/DDR3-1600 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-1600G (optional)		DDR3L/DDR3-1600H		DDR3L/DDR3-1600J		DDR3L/DDR3-1600K		Unit	Notes
CL-nRCD-nRP			8-8-8		9-9-9		10-10-10		11-11-11			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	10	20	11.25	20	12.5	20	13.75 (13.125) [5,11]	20	ns	
ACT to internal Read or write delay time		t_{RCD}	10	-	11.25	-	12.5	-	13.75 (13.125) [5,11]	-	ns	
PRE command period		t_{RP}	10	-	11.25	-	12.5	-	13.75 (13.125) [5,11]	-	ns	
ACT to ACT or REF command period		t_{RC}	45	-	46.25	-	47.5	-	48.75 (48.125) [5,11]	-	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	3.0	3.3	ns	1,2,3,4, 8,12,13
	CWL = 6,7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4, 8
	CWL = 7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL =7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875 (Optional)[5,11]	< 2.5	ns	1,2,3,4, 8
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		Reserved		Reserved		ns	1,2,3,4, 8
	CWL = 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	Reserved		Reserved		ns	1,2,3,4, 8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5 (Optional)[5,11]	< 1.875	ns	1,2,3,4, 8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved			1,2,3,4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5,6,7,8,9,10,(11)		5,6,7,8,9,10,(11)		5,6,7,8,9,10,(11)		5,6,(7),8,(9),10,11		n_{CK}	
Supported CWL Settings			5,6,7,8		5,6,7,8		5,6,7,8		5,6,7,8		n_{CK}	

Table 11-6. DDR3L/DDR3-1866 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-1866J (optional)		DDR3L/DDR3-1866K		DDR3L/DDR3-1866L		DDR3L/DDR3-1866M (optional)		Unit	Notes
CL-nRCD-nRP			10-10-10		11-11-11		12-12-12		13-13-13			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	10.7	20	11.77	20	12.84	20	13.91 (13.125)[5,14]	20	ns	
ACT to internal Read or write delay time		t_{RCD}	10.7	-	11.77	-	12.84	-	13.91 (13.125)[5,14]	-	ns	
PRE command period		t_{RP}	10.7	-	11.77	-	12.84	-	13.91 (13.125)[5,14]	-	ns	
ACT to PRE command period		t_{RAS}	34	9 * tREFI	34	9 * tREFI	34	9 * tREFI	34	9 * tREFI	ns	
ACT to ACT or REF command period		t_{RC}	44.7	-	45.77	-	46.84	-	47.91 (47.125)[5,14]	-	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,9
	CWL = 6,7,8,9	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,9
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL =7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875 (Optional)[5,14]	< 2.5	ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,9
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	Reserved		Reserved		ns	1,2,3,4,9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5 (Optional)[5,14]	< 1.875	ns	1,2,3,4,9
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		Reserved			1,2,3,4,9
	CWL = 9		Reserved		Reserved		Reserved		Reserved			4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,9
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved		ns	1,2,3,4,9
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25 (Optional)[5,14]	< 1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	Reserved		Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5,6,7,8,9,10, 11,12,(13)		5,6,7,8,9,10, 11,12,(13)		5,6,7,8,9,10, 11,12,(13)		6,8,10,13 (7),(9),(11)		n_{CK}	
Supported CWL Settings			5,6,7,8,9		5,6,7,8,9		5,6,7,8,9		5,6,7,8,9		n_{CK}	

Table 11-7. DDR3L/DDR3-2133 Speed Bins and Operating Conditions

Speed Bin			DDR3L/DDR3-2133G (optional)		DDR3L/DDR3-2133H		DDR3L/DDR3-2133J		DDR3L/DDR3-2133K		Unit	Notes
CL-nRCD-nRP			11-11-11		12-12-12		13-13-13		14-14-14			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Internal Read command to first data		t_{AA}	10.285	20	11.22	20	12.155	20	13.09	20	ns	
ACT to internal Read or write delay time		t_{RCD}	10.285	-	11.22	-	12.155	-	13.09	-	ns	
PRE command period		t_{RP}	10.285	-	11.22	-	12.155	-	13.09	-	ns	
ACT to PRE command period		t_{RAS}	33	9 * tREFI	33	9 * tREFI	33	9 * tREFI	33	9 * tREFI	ns	
ACT to ACT or REF command period		t_{RC}	43.285	-	44.22	-	45.155	-	46.09	-	ns	
CL =5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	Reserved		ns	1,2,3,4,10
	CWL = 6,7,8,9,10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,10
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,10
	CWL = 7,8,9,10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL =7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,10
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		Reserved		Reserved		ns	1,2,3,4,10
	CWL = 8,9,10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,10
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	Reserved		Reserved		ns	1,2,3,4,10
	CWL = 8,9,10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,4,10
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved		ns	1,2,3,4,10
	CWL = 9,10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,10
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1,2,3,4,10
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	Reserved		Reserved		Reserved		ns	1,2,3,4,10
	CWL = 10	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3,10
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	Reserved		Reserved		ns	1,2,3,4,10
	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	Reserved		ns	1,2,3,4,10
	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	0.938	< 1.07	Reserved		Reserved		ns	1,2,3,4

Speed Bin			DDR3L/DDR3-2133G (optional)		DDR3L/DDR3-2133H		DDR3L/DDR3-2133J		DDR3L/DDR3-2133K		Unit	Notes
CL-nRCD-nRP			11-11-11		12-12-12		13-13-13		14-14-14			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	1.07	< 1.25	ns	1,2,3,10
	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	0.938	< 1.07	0.938	< 1.07	Reserved		ns	1,2,3,4
CL = 14	CWL = 5,6,7,8,9	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	0.938	< 1.07	0.938	< 1.07	0.938	< 1.07	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5,6,7,8,9,10, 11,12,13,(14)		5,6,7,8,9,10, 11,12,13,(14)		5,6,7,8,9,10, 11,12,13,(14)		5,6,7,8,9,10, 11,12,13,14		n_{CK}	
Supported CWL Settings			5,6,7,8,9,10		5,6,7,8,9,10		5,6,7,8,9,10		5,6,7,8,9,10		n_{CK}	

11.3.1 Speed Bin Table Note

Absolute Specifications {T_{OPER}; V_{DDQ}= V_{DD}= 1.283V to 1.45V & 1.5V(1.425V to 1.575V)};

Note:

1. The CL setting and CWL setting result in tCK(AVG). MIN and tCK(AVG). MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL-all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25,1.07, or 0.938 ns) when calculating CL [nCK] = tAA[ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.5 ns or 1.25 ns or 1.07 ns or0.938 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3L/DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR3L/DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR3L/DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR3L/DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
10. Any DDR3L/DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
11. For devices supporting optional down binningto CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3L-1333H devices supporting down binning to DDR3L-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte

20). DDR3L-1600K devices supporting down binning to DDR3L-1333H or DDR3L-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte20) is programmed to13.125ns, tRCmin (Byte 21,23) also should be programmed accodingly. For example, 49.125 ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3L-1333H and 48.125ns (tRASmin + tRPmin =35 ns + 13.125 ns) for DDR3L-1600K.

12. DDR3L-800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
13. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
14. For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3L/DDR3-1866M devices supporting down binning to DDR3L/DDR3-1600K or DDR3L/DDR3-1333H or 1066F should program 13.125 ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRPmin (byte20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34 ns+ 13.125 ns)

12 ELECTRICAL CHARACTERISTICS AND AC TIMING

12.1 Timing Parameters for DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600

Table 12-1. Timing Parameters by Speed Bin

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	8	-	ns	6
Average Clock Period	tCK (avg)	See “Standard Speed Bins								ps	
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	
Absolute Clock Period	tCK (abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL (abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT (per)	-100	100	-90	90	-80	80	-70	70	ps	
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-90	90	-80	80	-70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	200		180		160		140		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	180		160		140		120		ps	
Duty Cycle Jittter	tJIT (duty)	-	-	-	-	-	-	-	-		
Cumulative error across 2 cycles	tERR (2per)	-147	147	-132	132	-118	118	-103	103	ps	
Cumulative error across 3 cycles	tERR (3per)	-175	175	-157	157	-140	140	-122	122	ps	
Cumulative error across 4 cycles	tERR (4per)	-194	194	-175	175	-155	155	-136	136	ps	
Cumulative error across 5 cycles	tERR (5per)	-209	209	-188	188	-168	168	-147	147	ps	
Cumulative error across 6 cycles	tERR (6per)	-222	222	-200	200	-177	177	-155	155	ps	
Cumulative error across 7 cycles	tERR (7per)	-232	232	-209	209	-186	186	-163	163	ps	
Cumulative error across 8 cycles	tERR (8per)	-241	241	-217	217	-193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR (9per)	-249	249	-224	224	-200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR (10per)	-257	257	-231	231	-205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR (11per)	263	263	-237	237	-210	210	-184	184	ps	

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 12 cycles	tERR (12per)	-269	269	-242	242	-215	215	-188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR (nper)	tERR (nper)min = ((1 + 0.68ln(n)) * tJIT (per)_total min)								ps	24
		tERR (nper)max = ((1 + 0.68ln(n)) * tJIT (per)_total max)									
Data Timing											
DQS,DQS# to DQ skew, per group, per acces	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK (avg)	13, g
DQ low impedance time from CK, CK#	tLZ (DQ)	-800	400	-600	300	-500	250	-450	225	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ (DQ)	-	400	-	300	-	250	-	225	ps	13,14,f
Data setup time from DQS, DQS# referenced to VIH(ac) / VIL(ac) levels	tDS(base) AC175	75		25		-		-		ps	d,17
	tDS(base) AC150	125		75		30		10		ps	d,17
Data hold time to DQS, DQS# referenced to VIH(ac) / VIL(ac) levels	tDH(base) DC100	150		100		65		45		ps	d,17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	ps	28
Data Strobe Timing											
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK (avg)	13,19,g
DQS, DQS# differential READ Preamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK (avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	0.40	-	0.40	-	tCK (avg)	13,g
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	0.40	-	0.40	-	tCK (avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK (avg)	1
DQS, DQS# differential WRITE Preamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK (avg)	1
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-400	400	-300	300	-255	255	-225	225	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-800	400	-600	300	-500	250	-450	225	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	ps	13,14,f
DQS and DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK (avg)	29,31
DQS and DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK (avg)	30,31

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	tCK (avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.18	-	tCK (avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.18	-	tCK (avg)	c,32
Command and Address Timing											
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	Max (12nCK, 15 ns)	-	Max (12nCK, 15 ns)	-	Max (12nCK, 15 ns)	-	Max (12nCK, 15 ns)	-		
ACT to internal read or write delay time	tRCD	See Table 11-2		See Table 11-3		see Table 11-4		See Table 11-5			e
PRE command period	tRP	See Table 11-2		See Table 11-3		see Table 11-4		See Table 11-5			e
ACT to ACT or REF command period	tRC	See Table 11-2		See Table 11-3		see Table 11-4		See Table 11-5			e
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + round up (tRP / tCK(avg))								nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See Table 11-2		See Table 11-3		see Table 11-4		See Table 11-5			e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	Max (4nCK, 10 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 6 ns)	-	Max (4nCK, 6 ns)	-		e
ACTIVE to ACTIVE command period for 2KB page siz	tRRD	Max (4nCK, 10 ns)	-	Max (4nCK, 10 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	ns	e

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC100	200		125		65		45		ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	350		275		190		170		ps	b,16,27
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100	275		200		140		120		ps	b,16
Control and Address Input pulse width for each input	tIPW	900	-	780	-	620	-	560	-	ps	28
Calibration Timing											
Power-up and RESET calibration time	tZQinit	Max (512nCK, 640 ns)	-	Max (512nCK, 640 ns)	-	Max (512nCK, 640 ns)	-	Max (512nCK, 640 ns)	-		
Normal operation Full calibration time	tZQoper	Max (256nCK, 320 ns)	-	Max (256nCK, 320 ns)	-	Max (256nCK, 320 ns)	-	Max (256nCK, 320 ns)	-		
Normal operation short calibration Short calibration time	tZQCS	Max (64nCK, 80 ns)	-	Max (64nCK, 80 ns)	-	Max (64nCK, 80 ns)	-	Max (64nCK, 80 ns)	-		23
Reset Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-		
Self Refresh Timing											
Exit Self Refresh to commands not requiring a locked DLL	tXS	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Power Down Timing											
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (3nCK, 7.5 ns)	-	Max (3nCK, 7.5 ns)	-	Max (3nCK, 6ns)	-	Max (3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	Max (10nCK, 24ns)	-	Max (10nCK, 24ns)	-	Max (10nCK, 24ns)	-	Max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	Max (3nCK, 7.5 ns)	-	Max (3nCK, 5.625 ns)	-	Max (3nCK, 5.625 ns)	-	Max (3nCK, 5ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	nCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	nCK	
ODT Timing											
ODT turn on Latency	ODTLon	WL -2 = CWL + AL - 2								nCK	
ODT turn off Latency	ODTLoff	WL -2 = CWL + AL - 2								nCK	

Speed		DDR3L/DDR3-800		DDR3L/DDR3-1066		DDR3L/DDR3-1333		DDR3L/DDR3-1600		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	ps	7, f
RTT_Nom and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing											
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	tWLS	325	-	245	-	195	-	165	-	ps	
Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK#_crossing	tWLH	325	-	245	-	195	-	165	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	

12.2 Timing Parameters for DDR3L-1866 and DDR3L-2133 Speed Bins

Table 12-2. Timing Parameters by Speed Bin

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	ns	6
Average Clock Period	tCK (avg)	See “Standard Speed Bins				ns	
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	tCK (avg)	
Absolute Clock Period	tCK (abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL (abs)	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT (per)	-60	60	-50	50	ps	
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-50	50	-40	40	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	120		100		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	100		80		ps	
Duty Cycle Jittter	tJIT (duty)	-	-	-	-		
Cumulative error across 2 cycles	tERR (2per)	-88	88	-74	74	ps	
Cumulative error across 3 cycles	tERR (3per)	-105	105	-87	87	ps	
Cumulative error across 4 cycles	tERR (4per)	-117	117	-97	97	ps	
Cumulative error across 5 cycles	tERR (5per)	-126	126	-105	105	ps	
Cumulative error across 6 cycles	tERR (6per)	-133	133	-111	111	ps	
Cumulative error across 7 cycles	tERR (7per)	-139	139	-116	116	ps	
Cumulative error across 8 cycles	tERR (8per)	-145	145	-121	121	ps	
Cumulative error across 9 cycles	tERR (9per)	-150	150	-125	125	ps	
Cumulative error across 10 cycles	tERR (10per)	-154	154	-128	128	ps	
Cumulative error across 11 cycles	tERR (11per)	-158	158	-132	132	ps	
Cumulative error across 12 cycles	tERR (12per)	-161	161	-134	134	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR (nper)	tERR (nper)min = ((1 + 0.68ln(n)) * tJIT (per)_total min) tERR (nper)max = ((1 + 0.68ln(n)) * tJIT (per)_total max)				ps	24
Data Timing							
DQS,DQS# to DQ skew, per group, per acces	tDQSQ	-	85	-	75	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK (avg)	13, g
DQ low impedance time from CK, CK#	tLZ (DQ)	-390	195	-360	180	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ (DQ)	-	195	-	180	ps	13,14,f
Data setup time from DQS, DQS# referenced to VIH(ac) / VIL(ac) levels	tDS(base) AC150	-		-		ps	d,17
	tDS(base) AC135	68		53		ps	d,17
Data hold time to DQS, DQS# referenced to VIH(ac) / VIL(ac) levels	tDH(base) DC100	-		-		ps	d,17
DQ and DM Input pulse width for each input	tDIPW	320	-	280	-	ps	28
Data Strobe Timing							
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK (avg)	13,19,g

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS, DQS# differential READ Preamble	tRPST	0.3	Note 11	0.3	Note 11	tCK (avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.4	-	0.38	-	tCK (avg)	13,g
DQS, DQS# differential output low time	tQSL	0.4	-	0.38	-	tCK (avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK (avg)	1
DQS, DQS# differential WRITE Preamble	tWPST	0.3	-	0.3	-	tCK (avg)	1
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-195	195	-180	180	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-390	195	-360	180	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	195	-	180	ps	13,14,f
DQS and DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK (avg)	29,31
DQS and DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK (avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	tCK (avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	tCK (avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	tCK (avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	Max (12nCK, 15 ns)	-	Max (12nCK, 15 ns)	-		
ACT to internal read or write delay time	tRCD	See Table 11-6		See Table 11-3			e
PRE command period	tRP	See Table 11-6		See Table 11-3			e
ACT to ACT or REF command period	tRC	See Table 11-6		See Table 11-3			e
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See Table 11-6		See Table 11-3			e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	Max (4nCK, 5.0 ns)	-	Max (4nCK, 5.0 ns)	-		e
ACTIVE to ACTIVE command period for 2KB page siz	tRRD	Max (4nCK, 6.0 ns)	-	Max (4nCK, 6.0 ns)	-		e

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Four activate window for 1KB page size	tFAW	27	-	25	-	ns	e
Four activate window for 2KB page size	tFAW	35	-	35	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC100	-		-		ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	150		135		ps	b,16,27
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100	100		95		ps	b,16
Control and Address Input pulse width for each input	tIPW	535	-	470	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	Max (512nCK, 640 ns)	-	Max (512nCK, 640 ns)	-		
Normal operation Full calibration time	tZQoper	Max (256nCK, 320 ns)	-	Max (256nCK, 320 ns)	-		
Normal operation short calibration Short calibration time	tZQCS	Max (64nCK, 80 ns)	-	Max (64nCK, 80 ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-		
Self Refresh Timing							
Exit Self Refresh to commands not requiring a locked DLL	tXS	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		
Power Down Timing							
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (3nCK, 6 ns)	-	Max (3nCK, 6 ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	Max (10nCK, 24ns)	-	Max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	Max (3nCK, 5 ns)	-	Max (3nCK, 5 ns)	-		
Command pass disable delay	tCPDED	2	-	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI		15

Speed		DDR3L/DDR3-1866		DDR3L/DDR3-2133		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Timing of ACT command to Power Down entry	tACTPDEN	1	-	2	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	2	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR / tCK(avg))	-	WL + 4 + (tWR / tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	2	-	nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-		
ODT Timing							
ODT turn on Latency	ODTLon	WL -2 = CWL + AL - 2				nCK	
ODT turn off Latency	ODTLoff	WL -2 = CWL + AL - 2				nCK	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-195	195	-180	180	ps	7, f
RTT_Nom and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS/DQS# crossing	tWLS	140	-	125	-	ps	
Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK# crossing	tWLH	140	-	125	-	ps	
Write leveling output delay	tWLO	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

12.3 Jitter Notes

Note:

a. Unit ‘tCK(avg)’ represents the actual tCK(avg) of the input clock under operation. Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per).min.

b. These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), asthe setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

c. These parameters are measured from a data strobe signal (DQS(L/U), DQS (L/U) #) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

d. These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U) #) crossing.

e. For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU {tPARAM [ns] / tCK(avg) [ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU {tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3L/DDR3-800 6-6-6, of which tRP =15ns, the device will support tnRP = RU {tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

f. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3L/DDR3-800 SDRAM has tERR(mper), act, min = - 172 ps and tERR(mper), act, max = + 193 ps, then tDQSCK, min(derated) = tDQSCK, min -tERR(mper), act, max = - 400 ps - 193 ps = - 593 ps and tDQSCK, max(derated) = tDQSCK, max -tERR(mper), act, min = 400 ps + 172ps = + 572 ps. Similarly, tLZ(DQ) for DDR3L-800 derates totLZ(DQ), min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ), max(derated)= 400 ps + 172 ps = + 572 ps. (Caution onthe min/max usage!)
Note that tERR(mper), act, min is the minimum measured value of tERR(nper) where 2 <= n <=12, and tERR(mper), act, max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

g. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per), act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3L/DDR3-800 SDRAM has tCK(avg), act = 2500 ps, tJIT(per), act, min = - 72 ps and tJIT(per), act, max = + 93 ps, then tRPRE, min(derated) =tRPRE, min + tJIT(per), act, min = 0.9 x tCK(avg), act + tJIT(per), act, min = 0.9 x 2500 ps - 72 ps =+ 2178 ps. Similarly, tQH, min(derated) = tQH, min + tJIT(per), act, min = 0.38 x tCK(avg), act +tJIT(per), act, min = 0.38 x 2500 ps - 72 ps= + 878 ps. (Caution onthe min/max usage!)

12.4 Timing Parameter Notes

Note:

1. Actual value dependant upon measurement level definitions See “Method for calculating tWPRE transitions and endpoints” and “Method for calculating tWPST transitions and endpoints”.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-upto next higher integer value.

6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON.
8. For definition of RTT turn-off time tAOF.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship”.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for R_{ON34}.
14. tREFI depends on TOPER.
15. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) =VRefCA(DC). See 11.5 “Address / Command Setup, Hold and Derating”.
16. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 12.6 “Data Setup, Hold and Slew Rate Derating”.
17. Start of internal write transaction is defined as follows:
    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
18. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
19. CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
20. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
21. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
22. One ZQCS command can effectively correct aminimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

    $$ZQCorrection \geq TSens \times Tdriftrate + (VSens \times Vdriftrate)$$

    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

    For example, if TSens = 1.5% /℃, VSens = 0.15% / mV, Tdriftrate = 1℃ / sec and Vdriftrate= 15 mV / sec, then the interval between ZQCS commands is calculated as:

    $$0.5 \geq 1.5 \times 1 + (0.15 \times 15) = 0.133 \approx 128ms$$
23. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
24. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

25. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
26. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
27. Pulse width of an input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
28. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
29. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
30. tDQSH, act + tDQSL, act = 1 tCK, act; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
31. tDSH, act + tDSS, act = 1 tCK, act; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

12.5 Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the datasheet tIS(base) and tIH(base) value (see Table 12-3) to the △tIS and △tIH derating value (see Table 12-5) respectively. Example: tIS (total setup time) = tIS(base) + △tIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 12-1). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 12-2).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 12-1). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 12-3).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 12-12).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 12-5, the derating values may obtained by linear interpolation.

These values are typically not subject to productiontest. They are verified by design and characterization.

Table 12-3. ADD/CMD Setup and Hold Base-Values for 1V/ns (1.35 V)

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	DDR3L-2133	Units
tIS(base, AC160)	$V_{IH/L(AC)}$	215	140	80	60	-	-	ps
tIS(base, AC135)	$V_{IH/L(AC)}$	365	290	205	185	65	60	ps
tIS(base, AC125)	$V_{IH/L(AC)}$	-	-	-	-	150	135	ps
tIH(base, DC90)	$V_{IH/L(DC)}$	285	210	150	130	110	95	ps

Note:

1. (ac/dc referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate).
2. The tIS(base) AC135 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 125 ps for DDR3L-800/1066 or 100ps for DDR3L-1333/1600 of derating to accommodate for the lower alternate threshold of 135 mV and another 25 ps to account for the earlier reference point [(160 mv - 135 mV) / 1 V/ns].
3. The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75 ps for DDR3L-1866 and 65ps for DDR3L-2133 to accommodate for the lower alternate threshold of 125 mV and another 10 ps to account for the earlier reference point [(135 mv - 125 mV) /1 V/ns].

Table 12-4. ADD/CMD Setup and Hold Base-Values for 1V/ns (1.5 V)

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
tIS(base, AC175)	$V_{IH/L(AC)}$	200	125	65	45	-	-	ps
tIS(base, AC150)	$V_{IH/L(AC)}$	350	275	190	170	-	-	ps
tIS(base, AC135)	$V_{IH/L(AC)}$	-	-	-	-	65	60	ps
tIS(base, AC125)	$V_{IH/L(AC)}$	-	-	-	-	150	135	ps
tIH(base, DC90)	$V_{IH/L(DC)}$	275	200	140	120	100	95	ps

Note:

1. (ac/dc referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)

Table 12-5. Derating value DDR3L-800/1066/1333/1600 tIS/tIH – AC/DC based AC160 Threshold (1.35 V)

△tIS,△tIH derating in [ps] AC/DC based AC160 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-160mV																
		CK, CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

Table 12-6. Derating value DDR3L-800/1066/1333/1600 tIS/tIH – AC/DC based Alternate AC135 Threshold (1.35 V)

△tIS,△tIH derating in [ps] AC/DC based Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV																
		CK, CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

Table 12-7. Derating value DDR3L-1866/2133 tIS/tIH – AC/DC based Alternate AC125 Threshold (1.35 V)

△tIS,△tIH derating in [ps] AC/DC based Alternate AC125 Threshold -> VIH(ac)=VREF(dc)+125mV, VIL(ac)=VREF(dc)-125mV																	
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

Table 12-8. Derating value DDR3-800/1066/1333/1600 tIS/tIH – AC/DC based AC175 Threshold (1.5 V)

△tIS,△tIH derating in [ps] AC/DC based AC175 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV																	
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 12-9. Derating value DDR3-800/1066/1333/1600 tIS/tIH – AC/DC based AC150 Threshold (1.5 V)

△tIS,△tIH derating in [ps] AC/DC based Alternate AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																
		CK, CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 12-10. Derating value DDR3-1866/2133 tIS/tIH – AC/DC based AC135 Threshold (1.5 V)

△tIS,△tIH derating in [ps] AC/DC based Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV																
		CK, CK# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Table 12-11. Derating value DDR3-1866/2133 tIS/tIH – AC/DC based AC125 Threshold (1.5 V)

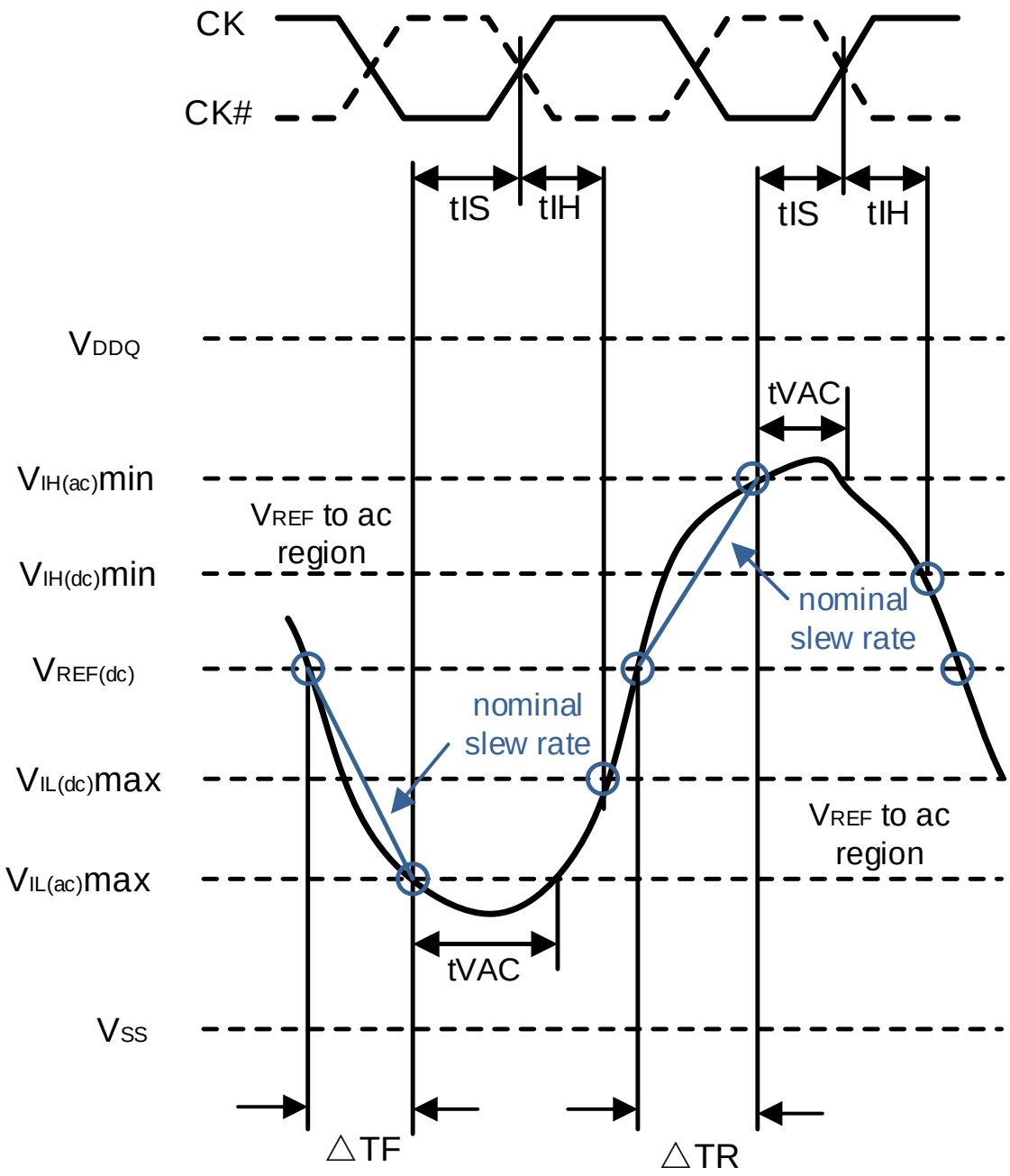
△tIS,△tIH derating in [ps] AC/DC based Alternate AC125 Threshold -> VIH(ac)=VREF(dc)+125mV, VIL(ac)=VREF(dc)-125mV																	
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ADD Slew Rate V/ns	2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

Table 12-12. Required minimum time t_{VAC} above VIH(ac) {below VIL(ac)} for valid ADD/CMD transition (1.35 V)

Slew Rate [V/ns]	DDR3				DDR3L			
	t800/1066/1333/1600		1866/2133		800/1066/1333/1600		1866/2133	
	175mV [ps]	150mV [ps]	135mV [ps]	125mV [ps]	160mV [ps]	135mV [ps]	135mV [ps]	125mV [ps]
>2.0	75	175	168	173	200	213	200	205
2.0	57	170	168	173	200	213	200	205
1.5	50	167	145	152	173	190	178	184
1.0	38	130	100	110	120	145	133	143
0.9	34	113	85	96	102	130	118	129
0.8	29	93	66	79	80	111	99	111
0.7	22	66	42	56	51	87	75	89
0.6	Note	30	10	27	13	55	43	59
0.5	Note	Note	Note	Note	Note	10	Note	18
<0.5	Note	Note	Note	Note	Note	10	Note	18

Note:

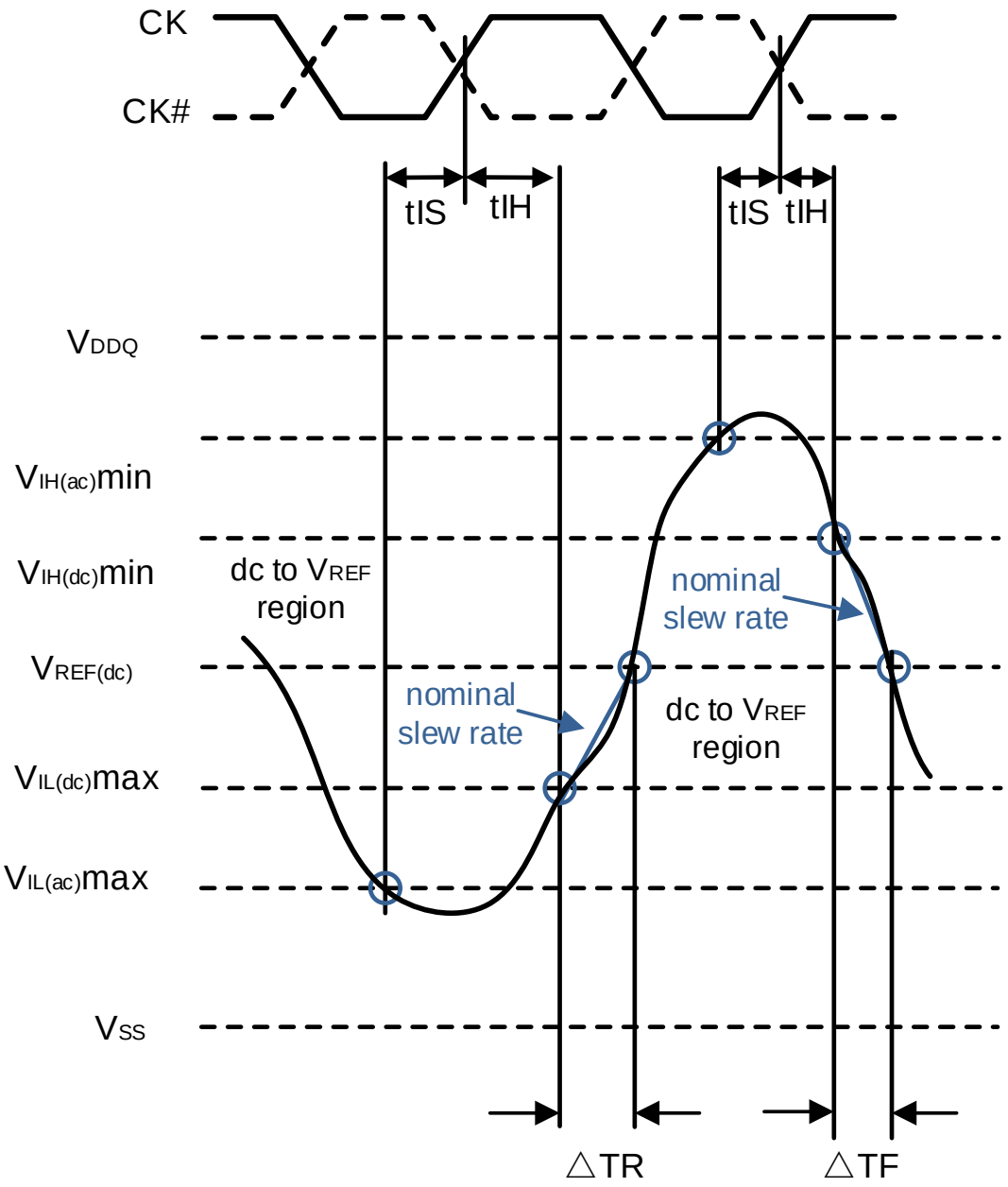
1. Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(dc) - V_{IL(ac)}(max)}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(ac)(min) - V_{REF}(dc)}{\Delta TR}$$

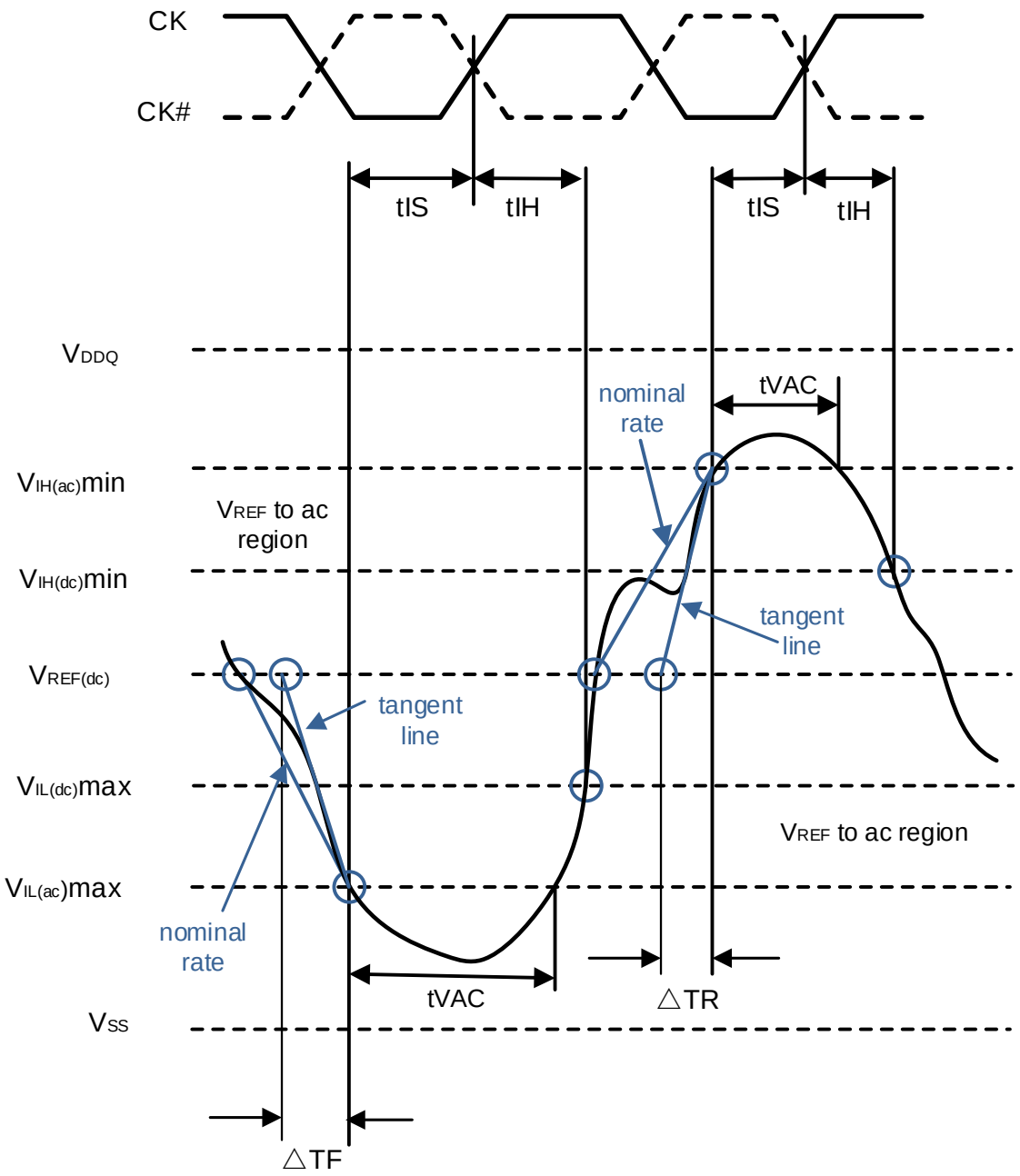
Figure 12-1. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = V_{REF\,dc} - V_{IL(dc)max}/\Delta TR$$

$$\text{Hold Slew Rate Falling Signal} = V_{IH\,dc\,min} - V_{REF\,dc}/\Delta TF$$

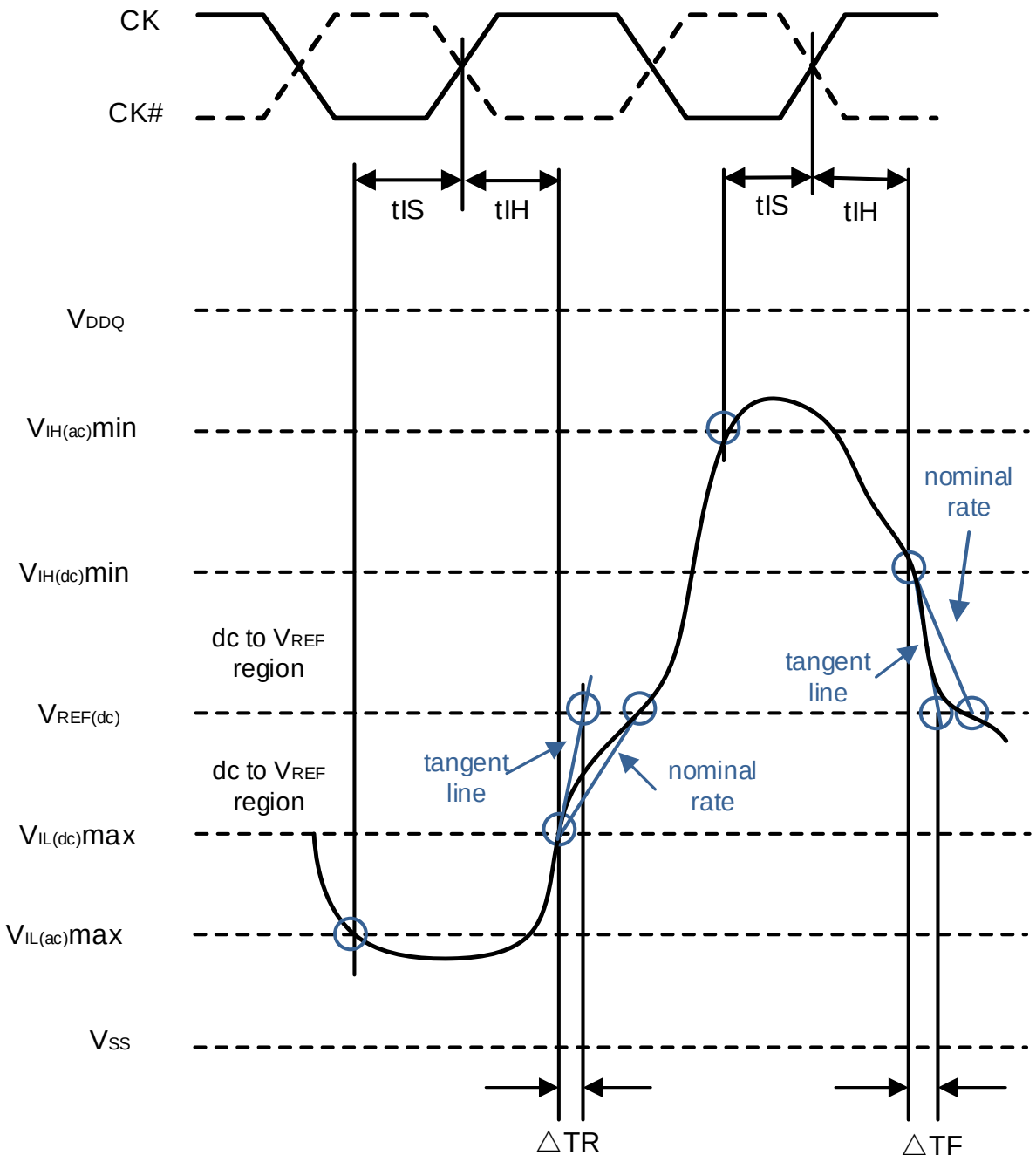
Figure 12-2. Illustration of nominal slew rate for hold time t_{IH} (for ADD/CMD with respect to clock).



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH\,ac}\text{min} - V_{REF\,dc}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF\,dc} - V_{IL\,ac}\text{max}]}{\Delta TF}$$

Figure 12-3. Illustration of tangent line for setup time t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{REF\,dc} - V_{IL\,dc}\,\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{IH\,dc}\,\text{min} - V_{REF\,dc}]}{\Delta TF}$$

Figure 12-4. Illustration of tangent line for hold time t_{IH} (for ADD/CMD with respect to clock).

12.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the △tDS and △tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + △tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is definedas the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see Figure 12-5). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 12-7).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 12-6). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rateline anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 12-8).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC}.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

12.6.1 Data Setup, Hold and Slew Rate Derating of DDR3-1866/2133

tDS(base) and tDH(base) of DDR3-1866/2133 are referenced for 2V/ns DQ-slew-rate and 4V/ns DQS slew-rate. Derating values △tDS and △tDH with DQ base slew rate 2V/ns shall be used to calculate total tDS and tDH of DDR3-1866/2133.

This means that for Data input signal above 1600Mbps the reference slew rate for setup/hold specification shall be set to 2V/ns. When DDR3-1866/2133 devices are used at or below 1600Mbps they shall meet an associated data setup/hold specification (including reference slew rate, levels and derating table) of the speed grade associated with that data rate.

For example, a 2133 device operating at 1600Mbps shall require tDS(AC150) = 10ps and tDH(DC100) = 45ps at 1V/ns (and the respective derating table.)

(Note that the AC levels of 135mV also do not apply if the device is not operated at highest data rate.)

Table 12-13. Data Setup and Hold Base-Values (1.35 V)

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Note
tDS(base, AC160)	$V_{IH/L(ac)}$ SR=1V/ns	90	40	-	-	-	ps	1
tDS(base, AC135)	$V_{IH/L(ac)}$ SR=1V/ns	140	90	45	25	-	ps	1
tDS(base, AC130)	$V_{IH/L(ac)}$ SR=2V/ns	-	-	-	-	70	ps	2
tDH(base, DC90)	$V_{IH/L(dc)}$ SR=2V/ns	-	-	-	-	75	ps	2
tDH(base, DC90)	$V_{IH/L(dc)}$ SR=1V/ns	160	110	75	55	-	ps	1

Note:

1. (ac/dc referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate)
2. (ac/dc referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate)
3. Optional in DDR3L SDRAM

Table 12-14. Data Setup and Hold Base-Values (1.5 V)

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
tDS(base, AC175)	$V_{IH/L(ac)}$ SR=1V/ns	75	25	-	-	-	-	ps
tDS(base, AC150)	$V_{IH/L(ac)}$ SR=1V/ns	125	75	30	10	-	-	ps
tDS(base, AC135)	$V_{IH/L(ac)}$ SR=1V/ns	165	115	60	40	-	-	ps
tDS(base, AC135)	$V_{IH/L(ac)}$ SR=2V/ns	-	-	-	-	68	53	ps
tDH(base, DC100)	$V_{IH/L(dc)}$ SR=1V/ns	150	100	65	45	-	-	ps
tDH(base, DC100)	$V_{IH/L(dc)}$ SR=2V/ns	-	-	-	-	70	55	ps

Note:

1. (ac/dc referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate)

Table 12-15. Derating values for DDR3L-800/1066 tDS/tDH – (AC160) (1.35 V)

AC160 Threshold-> VIH(ac)=VREF(dc)+160mV, VIL(ac)=VREF(dc)-160mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

Note:

1. Cell contents which is '- 'are defined as 'not supported'

Table 12-16.Derating values for DDR3L-800/1066/1333/1600 tDS/tDH – (AC135) (1.35 V)

AC135 Threshold-> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	34	53	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

Note:

1. Cell contents which is '- 'are defined as 'not supported'

Table 12-17. Derating values for DDR3L-1866 tDS/tDH – (AC130) (1.35 V)

AC130 Threshold-> VIH(ac)=VREF(dc)+130mV, VIL(ac)=VREF(dc)-130mV																									
DDR3L		DQS, DQS# Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	4.0	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

Note:

1. Cell contents which is '- 'are defined as 'not supported'

Table 12-18. Derating values for DDR3-800/1066 tDS/tDH – (AC175) (1.5 V)

AC175 Threshold-> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

Table 12-19. Derating values for DDR3-800/1066/1333/1600 tDS/tDH – (AC150) (1.5V)

AC150 Threshold-> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

Table 12-20. Derating values for DDR3-800/1066/1333/1600 tDS/tDH – (AC135) (1.5V)

AC150 Threshold-> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	2.0	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	35	53	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

Table 12-21. Derating values for DDR3-1866/2133 tDS/tDH – (AC135) (1.5V)

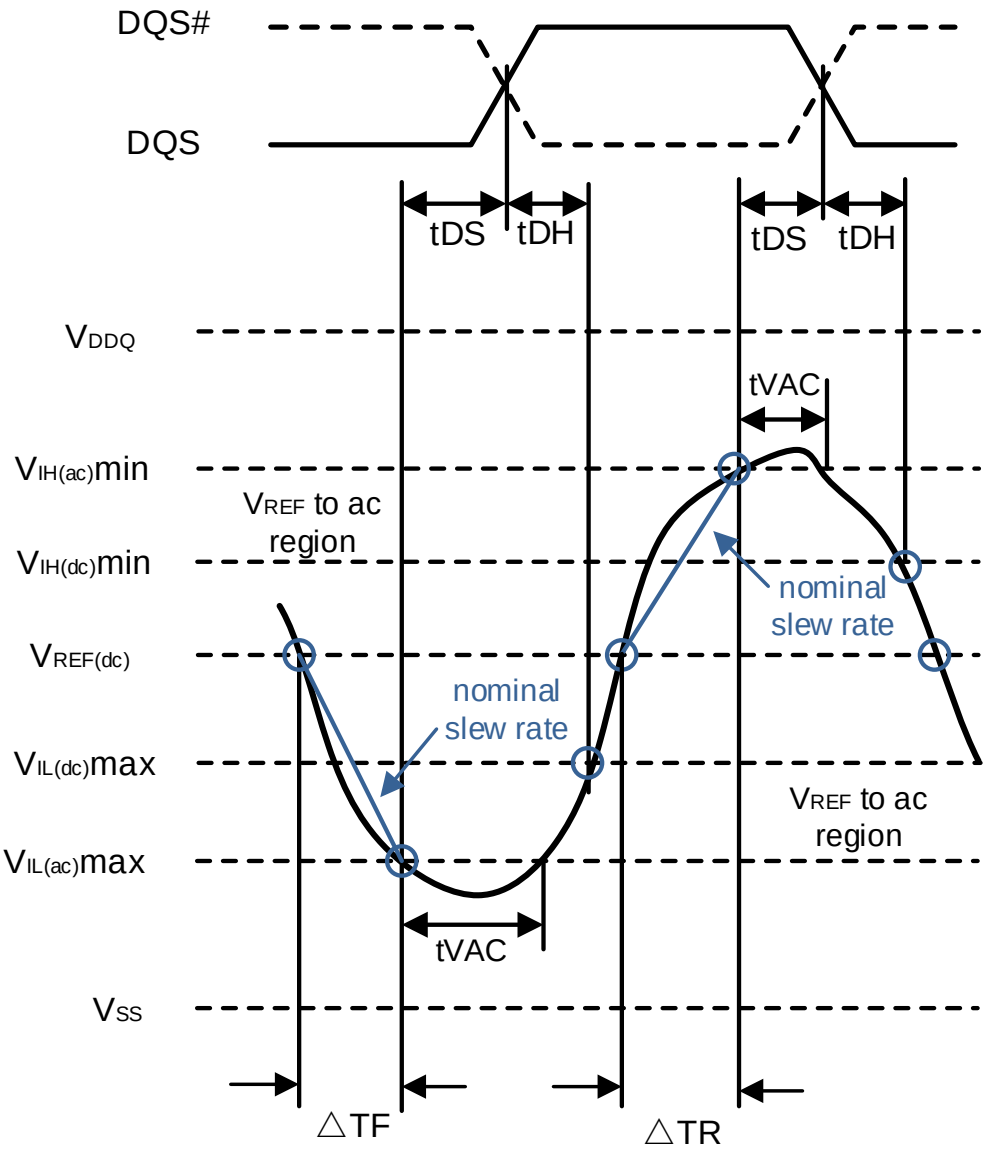
AC135Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)= VREF(dc)-135mV DC100Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)= VREF(dc)-100mV																									
		DQS, DQS# Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew Rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30			-	-
	0.8	-	-	-	-	-	-	-	-	-	-			-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-36	-76	-30	-60

Table 12-22. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid DQ transition

Slew Rate [V/ns]	DDR3 (1.5 V)					DDR3L (1.35 V)			
	800/1066	800/1066/1333/1600	800/1066/1333/1600	1866	2133	800/1066	800/1066/1333/1600	1866	2133
	AC175	AC150	AC135			AC160	AC135	AC130	AC130
>2.0	75	105	113	93	73	165	113	95	73
2.0	57	105	113	93	73	165	113	95	73
1.5	50	80	90	70	50	138	90	73	50
1.0	38	30	45	25	5	85	45	30	5
0.9	34	13	30	Note	Note	67	30	16	Note
0.8	29	Note	11	Note	Note	45	11	Note	Note
0.7	Note	Note	Note	-	-	16	Note	-	-
0.6	Note	Note	Note	-	-	Note	Note	-	-
0.5	Note	Note	Note	-	-	Note	Note	-	-
<0.5	Note	Note	Note	-	-	Note	Note	-	-

Note:

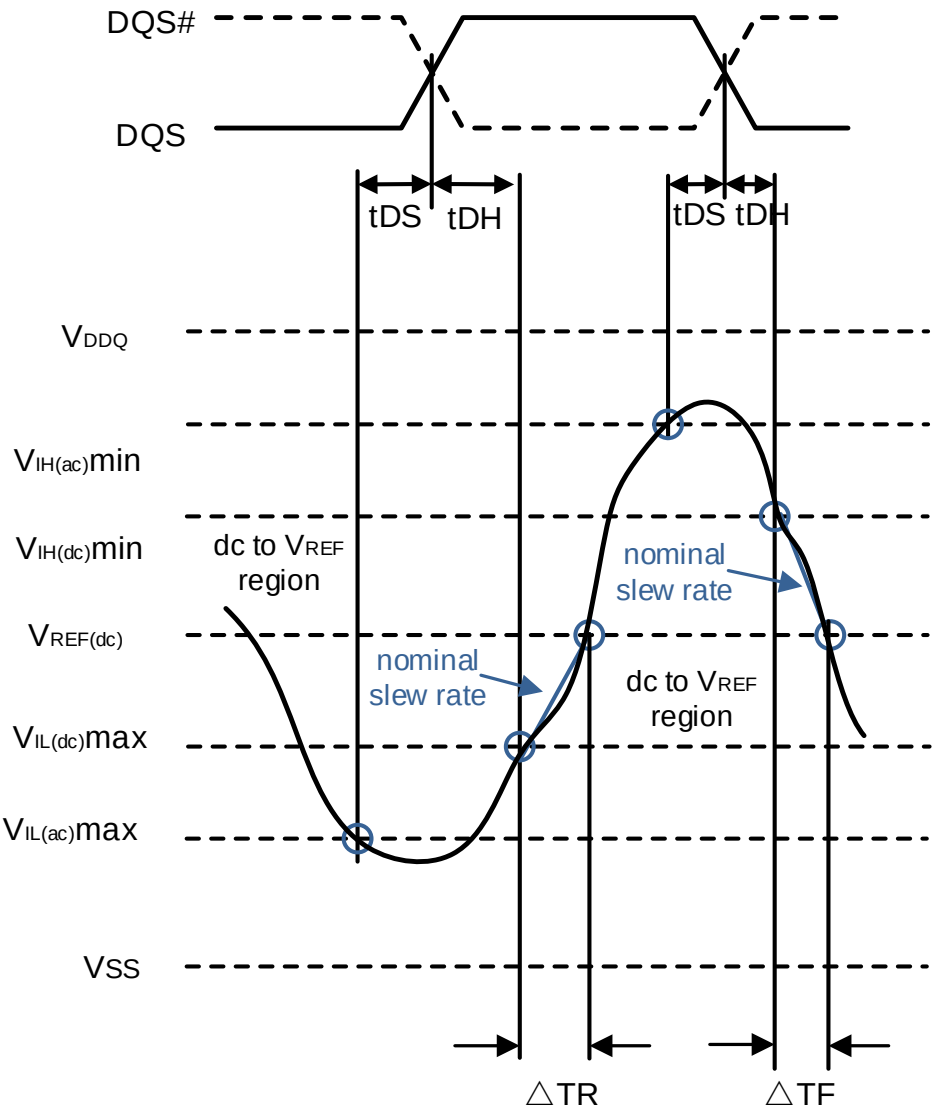
1. Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF\,dc} - V_{IL\,ac}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH\,ac} - V_{REF\,dc}}{\Delta TR}$$

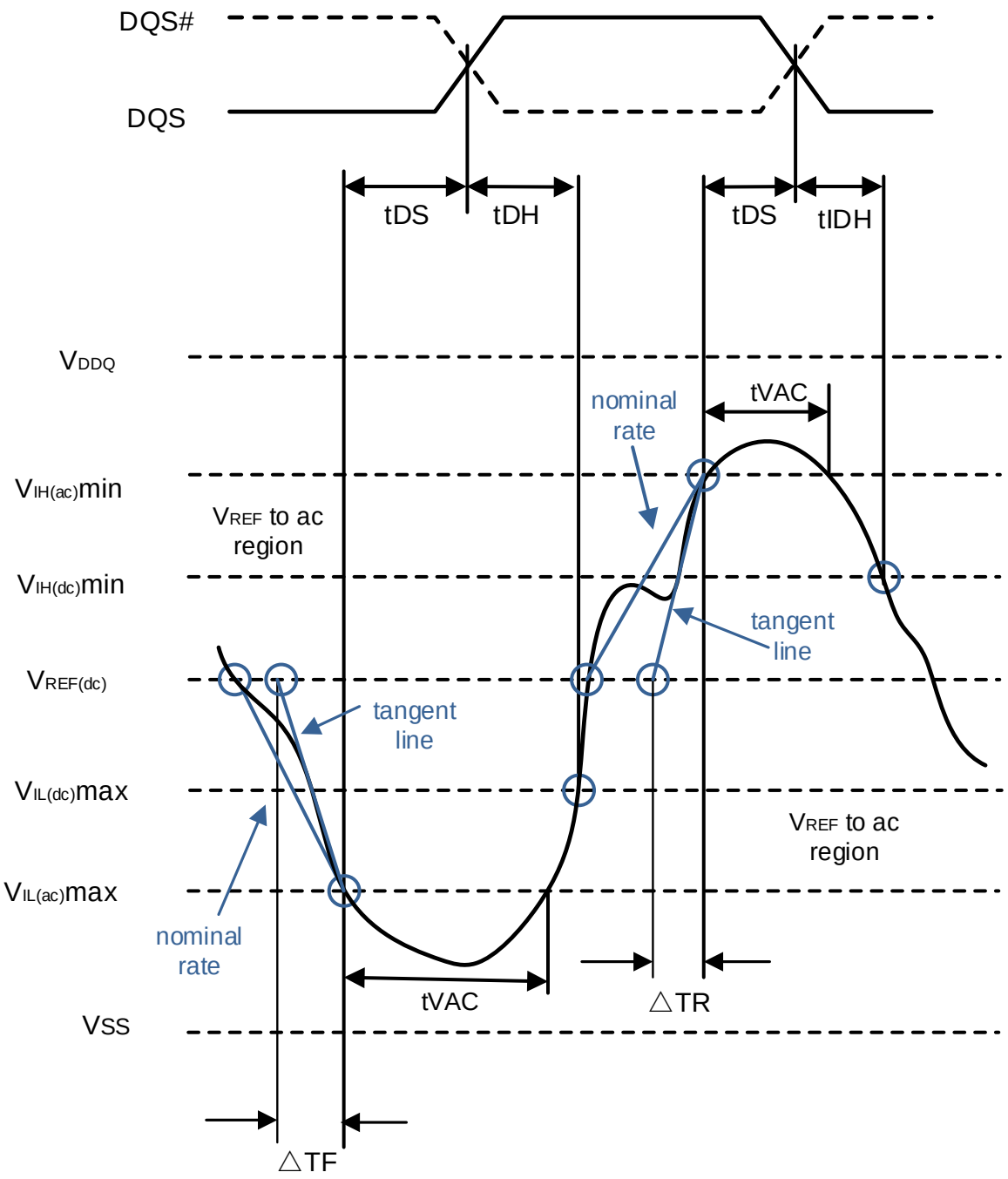
Figure 12-5. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \text{V□REF dc□□} - \text{V□IL dc□□max□ΔTR□}$$

$$\text{Hold Slew Rate Falling Signal} = \text{V□IH dc□□min} - \text{V□REF dc□□□ΔTF□}$$

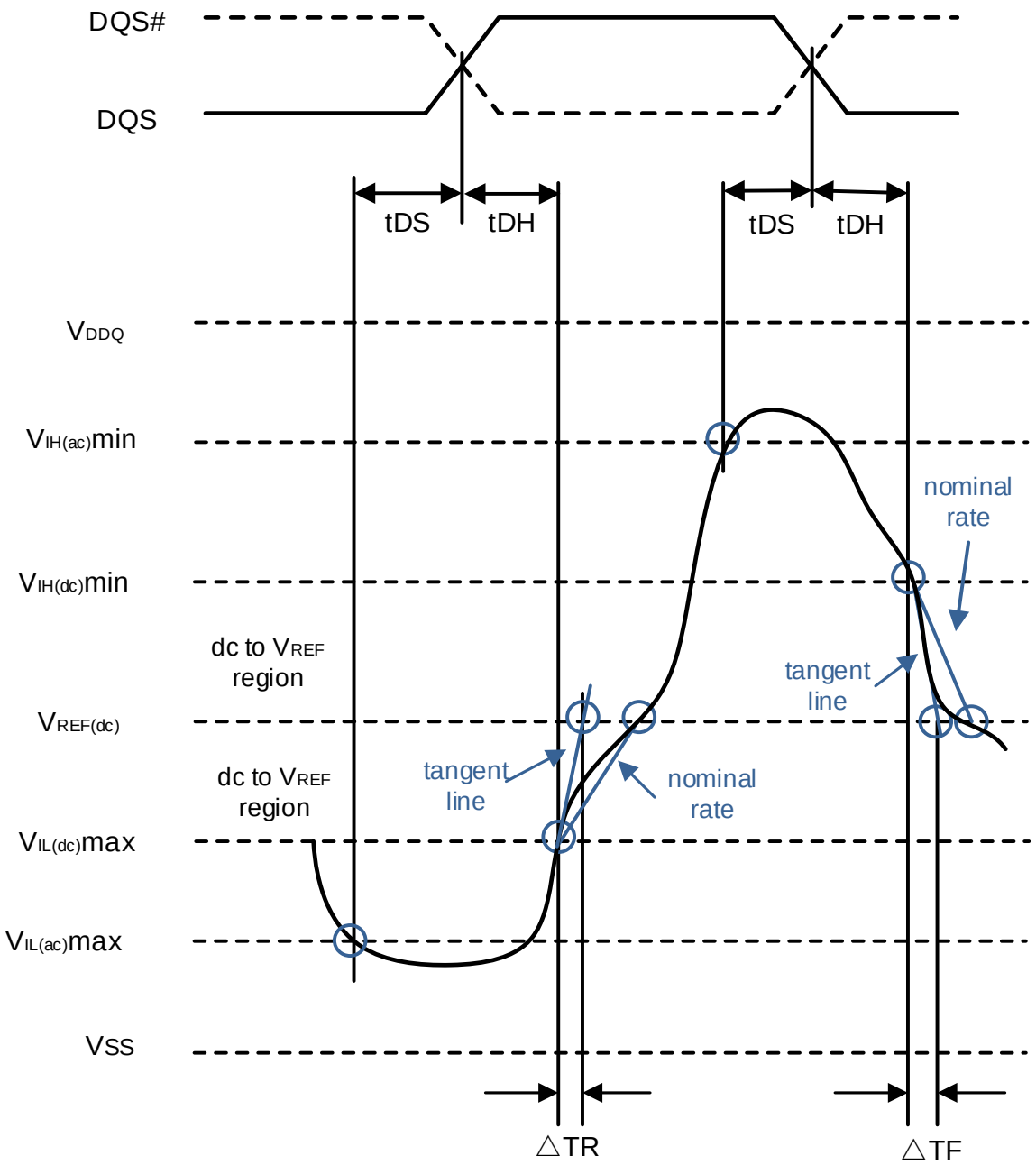
Figure 12-6. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe)



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH}(ac)\text{min} - V_{REF}(dc)]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF}(dc)\text{min} - V_{IL}(ac)\text{max}]}{\Delta TF}$$

Figure 12-7. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe)



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF\,dc} - V_{IL\,dc}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH\,dc}\text{min} - V_{REF\,dc}]}{\Delta TF}$$

Figure 12-8. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe)

13 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2022-5-24

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