USB Type-C Analog Audio Switch With Protection Function

FEATURES

- Power Supply V_{CC}: 2.7V to 5.5V
- USB High-Speed (480Mbps) Switch
  - SDD_{21} -3dB Bandwidth: 950MHz
  - 3Ω R_{ON} Typical
- Audio Switch
  - Negative Rail Capability: -3V to +3V
  - THD+N = -108dB; $1V_{RMS}$, f = 20Hz to 20KHz, 32Ω Load
  - 0.9Ω R_{ON} Typical
- High Voltage Protection
  - 20V DC Tolerance on Connector Side Pins
  - Over Voltage Protection: V_{TH} = 5V(Typ.)
- OMTP and CTIA Pinout Support
- Support Audio Sense Path
- 25-Ball WLCSP Package (2.24mm x 2.28mm)

GENERAL DESCRIPTIONS

The ASW5480 is a high performance USB Type-C port Multimedia switch which supports analog audio headsets. ASW5480 allows the sharing of a common USB Type-C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. ASW5480 also supports high voltage on SBU port and USB port on USB Type-C receptacle side.

APPLICATIONS

- Mobile Phone
- Tablet
- Notebook PC
- Media Player

BLOCK DIAGRAM

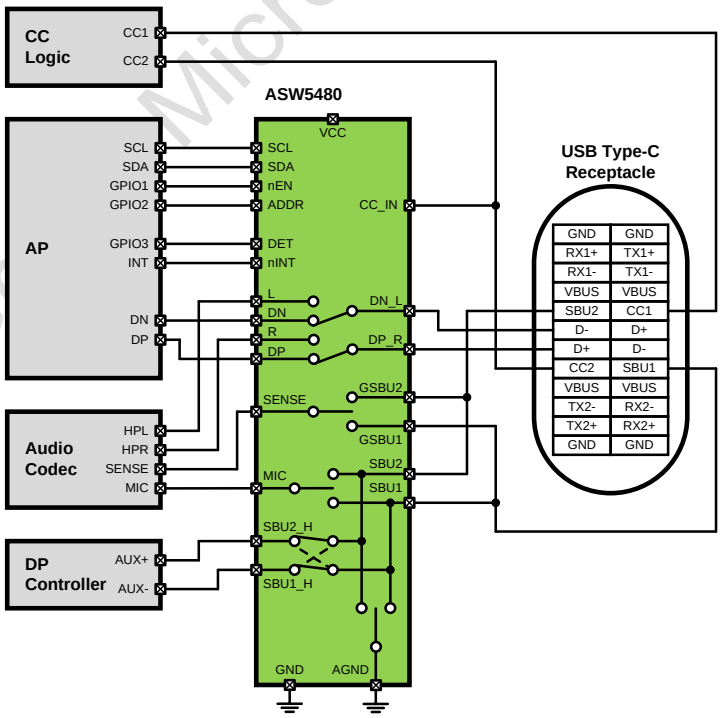


Figure 1, Block Diagram

Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	CHANGE DATE	CHANGE ITEMS
V01	2021/3	Initial version completed.
V02	2021/8	1. Update Resistance Detection flow. 2. Add DET pin notes in pape10.
V03	2022/7/5	The device ID was changed from 0x09 to 0x59.
V04	2023/05	Added humidity sensitivity level and Pin1 position description.
V05	2024/01	Update ESD HBM Model.

PIN DIAGRAM

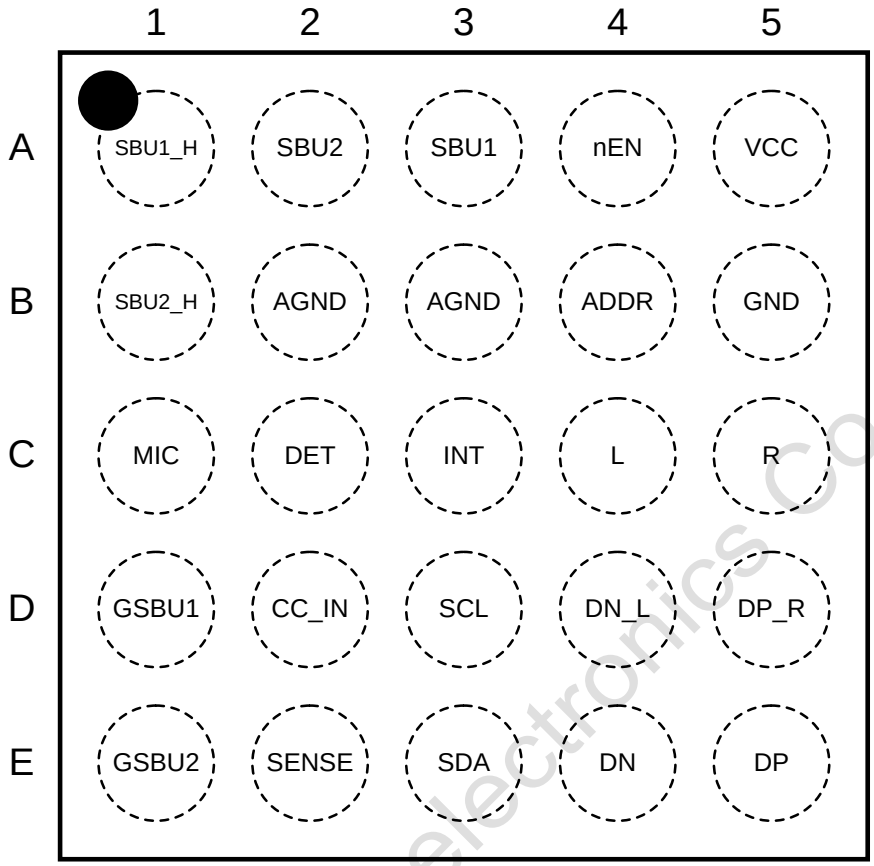


Figure 2, Pin Diagram (Top View)

PIN DESCRIPTIONS

No.	PIN No.	PIN NAME	TYPE	DESCRIPTIONS
1	A5	VCC	Power	Power Supply (2.7V to 5.5V)
2	B5	GND	Ground	Chip Ground
3	D5	DP_R	I/O	USB/Audio Common Connector
4	D4	DN_L	I/O	USB/Audio Common Connector
5	E5	DP	I/O	USB Data (Differential +)
6	E4	DN	I/O	USB Data (Differential -)
7	C5	R	I/O	Audio Right Channel
8	C4	L	I/O	Audio Left Channel
9	A3	SBU1	I/O	Sideband Use Wire 1
10	A2	SBU2	I/O	Sideband Use Wire 2
11	C1	MIC	I/O	Microphone Signal
12	B2	AGND	Ground	Audio Signal Ground
13	B3	AGND	Ground	Audio Signal Ground
14	E2	SENSE	I/O	Audio Ground Reference Output
15	C3	nINT	O	I^2C Interrupt Output, Active Low (Open Drain)
16	D2	CC_IN	I	Audio Accessory Attachment Detection Input
17	D1	GSBU1	I/O	Audio Sense Path 1 to Headset Jack GND
18	E1	GSBU2	I/O	Audio Sense Path 2 to Headset Jack GND
19	C2	DET	O	Push-Pull Output. When CC_IN > 1.5V, DET is Low and CC_IN < 1.2V, DET is High
20	D3	SCL	I	I^2C Clock
21	E3	SDA	I/O	I^2C Data
22	B1	SBU2_H	I/O	Host Side Sideband Use Wire 2
23	A1	SBU1_H	I/O	Host Side Sideband Use Wire 1
24	A4	nEN	I	Chip Enable, Active Low, Internal Pull-Down by 470kΩ
25	B4	ADDR	I	I^2C Slave Address Pin

Absolute Maximum Ratings

Stress exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Power Supply Voltage	-0.5	6.5	V
V_{CC_IN}	CC_IN to GND	-0.5	20	V
V_{SW_C}	DP_R to GND, DN_L to GND	-3.5	20	V
V_{SW_USB}	DP to GND, DN to GND	-0.5	6.5	V
V_{SW_AUDIO}	L to GND, R to GND	-3.5	6.5	V
$V_{SBU/GSBU}$	SBU1 to GND, SBU2 to GND, GSBU1 to GND, GSBU2 to GND	-0.5	20	V
V_{SBU_H}	SBU1_H to GND, SBU2_H to GND	-0.5	6.5	V
$V_{I/O}$	SENSE, MIC, DET, nINT to GND	-0.5	6.5	V
V_{CNTRL}	Control Input Voltage (SDA, SCL, nEN, ADDR)	-0.5	6.5	V
I_{SW_AUDIO}	Switch I/O Current, Audio Path	-250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path		100	mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2		50	mA
I_{SW_SBU}	Switch I/O Current, SBUx to SBUx_H		50	mA
I_{SW_SENSE}	Switch I/O Current, SENSE to GSBU1 or GSBU2		100	mA
I_{SW_AGND}	Switch I/O Current, AGND to SBU1 or SBU2		500	mA
I_{IK}	DC Input Diode Current	-50		mA
ESD	HBM Model (Connector Side and Power Pins: VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN)	3		KV
	HBM Model (Host Side Pins: the rest pins)	3		KV
	CDM Model	1		KV
T_A	Absolute Maximum Operating Temperature	-40	+85	°C
T_{STG}	Storage Temperature	-65	+150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

SYMBOL	PARAMETER	MIN	MAX	UNIT
POWER				
V_{CC}	Supply Voltage	2.7	5.5	V
USB SWITCH				
V_{SW_USB}	DP to GND, DN to GND, DP_R to GND, DN_L to GND	0	3.6	V
AUDIO SWITCH				
V_{SW_AUDIO}	DP_R to GND, DN_L to GND, L to GND, R to GND	-3.6	3.6	V
MIC SWITCH				
V_{SBU_MIC}	SBU1 to GND, SBU2 to GND, MIC to GND	0	3.6	V
SENSE SWITCH				
V_{GSBU_SENSE}	GSBU1 to GND, GSBU2 to GND, SENSE to GND	0	3.6	V
SBU to SBUx_H SWITCH				
V_{GSBU}	SBU1 to GND, SBU2 to GND, SBU1_H to GND, SBU2_H to GND	0	3.6	V
CC_IN PIN				
V_{CC_IN}	CC_IN to GND	0	5.5	V
CONTROL VOLTAGE (nEN, SDA, SCL)				
V_{IH}	Input Voltage High	1.3	V_{CC}	V
V_{IL}	Input Voltage Low		0.5	V
OPERATING TEMPERATURE				
T_A	Ambient Operating Temperature	-40	+85	°C

DC CHARACTERISTICS

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	POWER	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current	USB Switches on, SBUx to SBUx_H switches on	V_{CC} = 2.7 to 5.5V		39.5	65	μA
		Audio switches on, MIC switch on and Audio GND switch on			34.5	60	μA
I_{CCZ}	Quiescent Current	nEN = L, 04H'b7 = 0			1.2	5	μA
USB/AUDIO COMMON PINS: DP_R, DN_L							
I_{OZ}	Off Leakage Current of DP_R and DN_L	DN_L, DP_R = -3V to 3.6V	V_{CC} = 2.7 to 5.5V	-3.0	0.7	3.0	μA
I_{OFF}	Power-Off Leakage Current of DP_R and DN_L	DN_L, DP_R = 0V to 3.6V	Power Off	-3.0	0.7	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising Edge	V_{CC} = 2.7 to 5.5V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis				0.3		V
AUDIO SWITCH							
I_{ON}	On Leakage Current of Audio Switch	DN_L, DP_R = -3V to 3.0V, DP, DN, R, L = Floating	V_{CC} = 2.7 to 5.5V	-2.5	0.4	2.5	μA
I_{OFF}	Power-Off Leakage Current of L and R	L, R = 0V to 3V, DP_R, DN_L = Floating	Power Off	-1.0		1.0	μA
R_{ON_AUDIO}	Audio Switch On Resistance	I_{SW} = 100mA, V_{SW} = -3V to 3V	V_{CC} = 2.7 to 5.5V		0.9	2.1	Ω
R_{SHUNT}	Pull-Down Resistor on R/L Pin When Audio Switch is OFF	L = R = 3V		6	9.8	14	KΩ
USB SWITCH							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0V to 3.0V, DP, DN, R, L = Floating	V_{CC} = 2.7 to 5.5V	-3.0	0.5	3.0	μA
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V		-3.0	0.8	3.0	μA
I_{OFF}	Power-Off Leakage Current of DP and DN	DN, DP = 0V to 3.6V	Power OFF	-3.0		3.0	μA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8mA, V_{SW} = 0.4V	V_{CC} = 2.7 to 5.5V		2.6	5.2	Ω
SENSE SWITCH							
I_{ON}	Leakage Current of Sense Path	GSBUx = 0V to 1V, SENSE is floating	V_{CC} = 2.7 to 5.5V	-2.0	0.18	2.0	μA
R_{ON_SENSE}	SENSE Switch On Resistance	I_{SW} = 100mA, V_{SW} = 1V		0.2	0.7	1	Ω
I_{OZ}	Off Leakage Current of SENSE	SENSE = 0V to 1V		-2.0		2.0	μA
	Off Leakage Current of GSBUx	GSBUx = 0V to 1V		-2.0		2.0	μA
		GSBUx = 1V to 3.6V		-3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of SENSE	SENSE = 0V to 1V	Power Off	-2.0		2.0	μA
	Power-Off Leakage Current of GSBUx	GSBUx = 0V to 3.6V		-3.0		3.0	μA
V_{OV_TRIP}	Input OVP Lockout On GSBUx	Rising Edge	V_{CC} = 2.7 to 5.5V	4.5	4.9	5.3	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx				0.3		V
SBUx PINS							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0V to 3.6V	V_{CC} = 2.7 to 5.5V	-3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of SBUx	SBUx = 0V to 3.6V	Power OFF	-3.0		3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising Edge	V_{CC} = 2.7 to 5.5V	4.5	4.9	5.3	V
V_{OV_HYS}	Input OVP Hysteresis				0.3		V

DC CHARACTERISTICS (CONTINUED)

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	POWER	MIN	TYP	MAX	UNIT
MIC SWITCH							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0V to 3.6V, MIC is floating	V_{CC} = 2.7 to 5.5V	-3.0	0.38	3.0	µA
I_{OZ}	Off Leakage Current of MIC	MIC = 0V to 3.6V		-1.0		1.0	µA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0V to 3.6V	Power Off	-1.0		1.0	µA
R_{ON_MIC}	MIC Switch On Resistance	I_{SW} = 30mA, V_{SW} = 3.6V	V_{CC} = 2.7 to 5.5V	1.7	3.0	3.9	Ω
SBUx_H SWITCH							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0V to 3.6V, SBUx_H = Floating	V_{CC} = 2.7 to 5.5V	-3.0	0.14	3.0	µA
I_{OZ}	Off Leakage Current of SBUx_H	SBUx_H = 0V to 3.6V		-1.0		1.0	µA
I_{OFF}	Power-Off Leakage Current of SBUx_H	SBUx_H = 0V to 3.6V	Power Off	-1.0		1.0	µA
$R_{ON\_SBUx\_H}$	SBUx_H Switch On Resistance	I_{SW} = 30mA, V_{SW} = 0V to 3.6V	V_{CC} = 2.7 to 5.5V	1.5	2.7	3.5	Ω
AUDIO GROUND SWITCH (AGND to SBUx)							
R_{ON_AGND}	AGND Switch On Resistance	I_{SOURCE} = 100mA on SBUx	V_{CC} = 2.7 to 5.5V	30	57	90	mΩ
CC_IN PIN							
V_{TH_L}	Input Low Thershold		V_{CC} = 2.7 to 5.5V		1.2		V
V_{TH_H}	Input High Thershold				1.5		V
I_{IL}	Input Leakage of CC_IN	CC_IN = 0V to 5.5V				1.0	µA
nINT, DET PINS							
V_{OH}	Output High for DET	I_O = -2mA	V_{CC} = 2.7 to 5.5V	1.5	1.8	2.0	V
V_{OL}	Output Low for DET and nINT	I_O = 2mA				0.4	V
ADDR PIN							
V_{IH}	Input Voltage High		V_{CC} = 2.7 to 5.5V	0.9			V
V_{IL}	Input Voltage Low					0.7	V
I_{IL}	Input Leakage of ADDR	ADDR = 0V to V_{CC}		-1.0		1.0	µA
nEN PIN							
V_{IH}	Input Voltage High		V_{CC} = 2.7 to 5.5V	0.9			V
V_{IH}	Input Voltage Low					0.7	V
R_{PD}	Internal Pull-Down Resistor				470		KΩ
SDA, SCL PINS							
V_{IL_I2C}	Input Voltage Low					0.4	V
V_{IH_I2C}	Input Voltage High			1.2			V
I_{I2C}	Input Current of SDA and SCL Pins	SDA/SCL = 0V to 3.6V		-2.0		2.0	µA
V_{OL_SDA}	Output Voltage Low	I_{OL} = 2mA				0.3	V
I_{OL_SDA}	Output Current of Output Voltage Low	V_{OL_SDA} = 0.2V		10			mA

AC CHARACTERISTICS

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	POWER	MIN	TYP	MAX	UNIT
AUDIO SWITCH							
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L =1V, R_L = 32Ω	V_{CC} = 3.3V		40		µs
t_{rise}	Audio Switch Turn On Rising Time(1)				200		µs
t_{OFF}	Audio Switch Turn OFF Time				20		µs
X_{TALK}	Cross Talk (Adjacent)	f = 1KHz, R_L = 50Ω, V_{SW} = $1V_{RMS}$			-100		dB
BW	-3dB Bandwidth	R_L = 50Ω			600		MHz
O_{IRR}	Off Isolation	f = 1KHz, R_L = 50Ω, C_L = 0pF, V_{SW} = $1V_{RMS}$			-100		dB
THD+N	Total Harmonic Distortion + Noise Performance With A-Weighting Filter	f = 20Hz~20KHz, R_L = 600Ω, V_{SW} = $2V_{RMS}$			-110		dB
		f = 20Hz~20KHz, R_L = 32Ω, V_{SW} = $1V_{RMS}$			-108		dB
		f = 20Hz~20KHz, R_L = 16Ω, V_{SW} = $0.5V_{RMS}$			-104		dB
USB SWITCH							
t_{ON}	USB Switch Turn On Time	DP_R = DN_L =1.5V, R_L = 50Ω	V_{CC} = 3.3V		60		µs
t_{OFF}	USB Switch Turn Off Time				17		µs
BW	SDD_{21} -3dB Bandwidth	R_L = 50Ω			950		MHz
O_{IRR}	Off Isolation Between DP, DN and Common Node Pins	f = 1KHz, R_L = 50Ω, C_L = 0pF, V_{SW} = $1V_{RMS}$			-100		dB
t_{OVP}	DP_R and DN_L Pins OVP Response Time	V_{SW} = 3.5V to 5.5V			1	1.5	µs
MIC/AUDIO GROUND SWITCH							
t_{delay_MIC}	MIC Switch Turn On Delay Time	SBUx =1V, R_L = 50Ω	V_{CC} = 3.3V		40		µs
t_{rise_MIC}	MIC Switch Turn On Rising Time(1)				250		µs
t_{delay_AGND}	AGND Switch Turn On Time	SBUx pulled up to 0.5V by 16Ω, AGND connect to GND			100		µs
t_{rise_AGND}	AGND Switch Turn On Rising Time(1)				2200		µs
t_{OFF_MIC}	MIC Switch Turn OFF Time	SBUx =2.5V, R_L = 50Ω			12		µs
t_{OFF_AGND}	AGND Switch Turn OFF Time	SBUx: I_{SOURCE} = 10mA, Clamp to 2.5V			15		µs
BW	MIC Switch Bandwidth	R_L = 50Ω			60		MHz
SBUx_H SWITCH							
t_{ON}	SBUx_H Switch Turn On Time	SBUx_H =2.5V, R_L = 50Ω	V_{CC} = 3.3V		60		µs
t_{OFF}	SBUx_H Switch Turn Off Time				10		µs
BW	-3dB Bandwidth	R_L = 50Ω			60		MHz
t_{OVP}	SBUx Pins OVP Response Time	V_{SW} = 3.5V to 5.5V			0.5	1	µs
SENSE SWITCH							
t_{delay}	SENSE Switch Turn On Delay Time	GSBUx =1V, R_L = 50Ω	V_{CC} = 3.3V		50		µs
t_{rise}	SENSE Switch Turn On Rising Time(1)				200		µs
t_{OFF}	SENSE Switch Turn Off Time				12		µs
t_{OVP}	GSBUx Pins OVP Response Time	V_{SW} = 3.5V to 5.5V			0.7	1.5	µs
BW	-3dB Bandwidth	R_L = 50Ω			150		MHz

(1) Turn On Timing can be controlled by I2C register.

AC CHARACTERISTICS (CONTINUED)

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	POWER	MIN	TYP	MAX	UNIT
DET DELAY							
t_{delay_DET}	DET Response Delay Time	Transition from 0 to 1.8V	V_{CC} = 3.3V		1		µs
		Transition from 1.8 to 0V			3		µs

I²C SPECIFICATION (SCL, SDA)

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	FAST MODE		
		MIN	MAX	UNIT
f_{SCL}	I²C SCL Clock Frequency		400	KHz
$t_{HD;STA}$	Hold Time (repeated) START Condition	0.6		µs
t_{LOW}	Low Period of I²C SCL Clock	1.3		µs
t_{HIGH}	High Period of I²C SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time(2)	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(3)	100		ns
t_r	Rise Time of I²C SDA and I²C SCL Signals(3)	20 + 0.1C_b	300	ns
t_f	Fall Time of I²C SDA and I²C SCL Signals(3)	20 + 0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus-Free Time Between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

(2)Guaranteed by design, not production tested.

(3)A fast-mode I²C bus device can be used in a standard-mode I²C bus system, but the requirement $t_{SU;DAT}$ ≥ ±250ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C SCL signal. If such a device does stretch the LOW period of the I²C SCL signal, it must output the next data bit to the I²C SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the I²C SCL line is released.

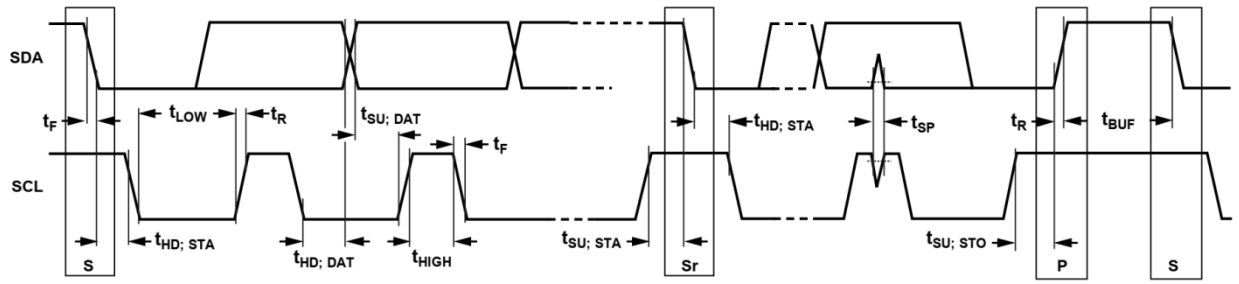


Figure 3, Definition of Timing for Full-Speed Mode Devices on the I²C Bus

CAPACITANCE

All typical values are at V_{CC} = 3.3V and T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	POWER	T_A = -40°C to 85°C			
				MIN	TYP	MAX	UNIT
$C_{ON\_USB/AUDIO}$	On Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias	V_{CC} = 3.3V		9		pF
$C_{OFF\_USB/AUDIO}$	Off Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			7.5		pF
C_{OFF_USB}	Off Capacitance (Non-Common Ports)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			3		pF
$C_{ON\_SENSE\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			55		pF
$C_{OFF\_SENSE\_SW}$	Off Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			88		pF
$C_{ON\_MIC\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			170		pF
$C_{OFF\_MIC\_SW}$	Off Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			10		pF
$C_{ON\_AGND\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			125		pF
$C_{ON\_SBUx\_H\_SW}$	On Capacitance (Common Port)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			160		pF
C_{CNTRL}	Control Input Pin Capacitance (nEN Pin)	f = 1MHz, 100mV_{PK-PK}, 100mV DC Bias			3		pF

APPLOCATION INFORMATION

Over-Voltage Protection

The ASW5480 features Over-Voltage Protection (OVP) on receptacle side pins that switch off the internal signal routing path if the input voltage exceeds the OVP threshold. If OVP is occurred, interrupt signal can be send by nINT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection

The ASW5480 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling(4). DET will be high when CC_IN is Low (CC_IN < 1.2V). When CC_IN is High (CC_IN > 1.5V), DET will be released to low.

	ASW5480 Disable	ASW5480 Enable
CC_IN < V_{TH_L} = 1.2V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5V	DET = 0	DET = 0

(4) DET pin is in Push/Pull Configuration as default . If you don't use this detection function , leave it floating.

MIC Switch Auto-Off Function

The function is active during control bit 0x12h bit[2] = 1. When CC_IN is high (CC_IN > 1.5V) and L, R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50μs first. Then it shows High-Z status under MIC switch is set on status.

Audio Ground Detection and Configuration

The function is active during control bit 0x12h bit[0] = 1 and R, L, AGND switches are set to be on status. For Type-C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

During detection and configuration, the L, R, SENSE, MIC and Audio ground switch will be off. After detection and configuration, L and R switches will turn on according to switch configuration and timing setting. MIC, SENSE and Audio ground will turn on according to detection results and timing control setting.

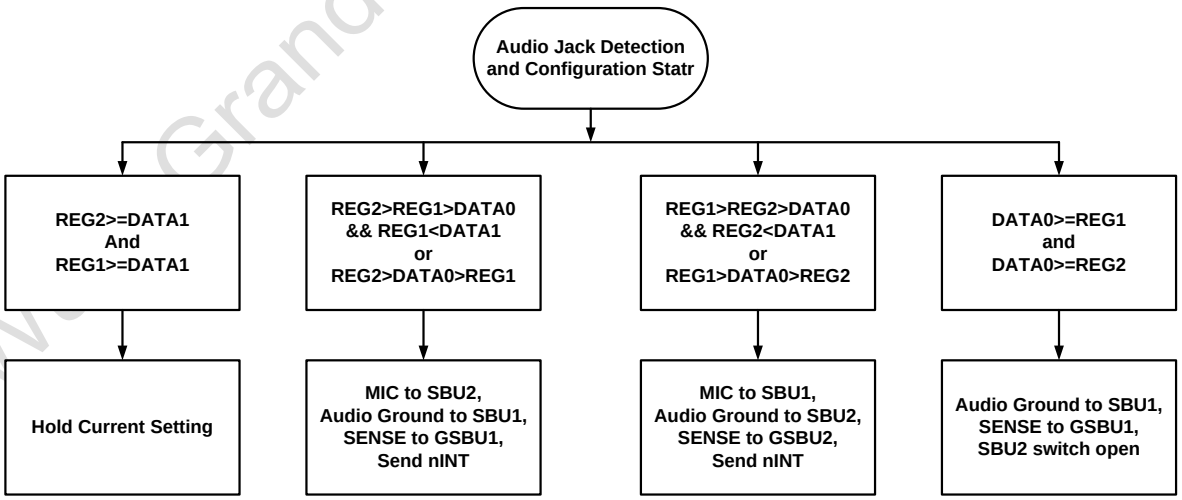


Figure 4, Audio Ground Detection and Configuration

Resistance Detection

The function is active during control bit 0x12h bit[1] = 1. It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register. The measurement could be from 1KΩ to 2.56MΩ which is controlled by internal register. The detection interval can be set at 100ms, 1s or 10s by register 0x16h.

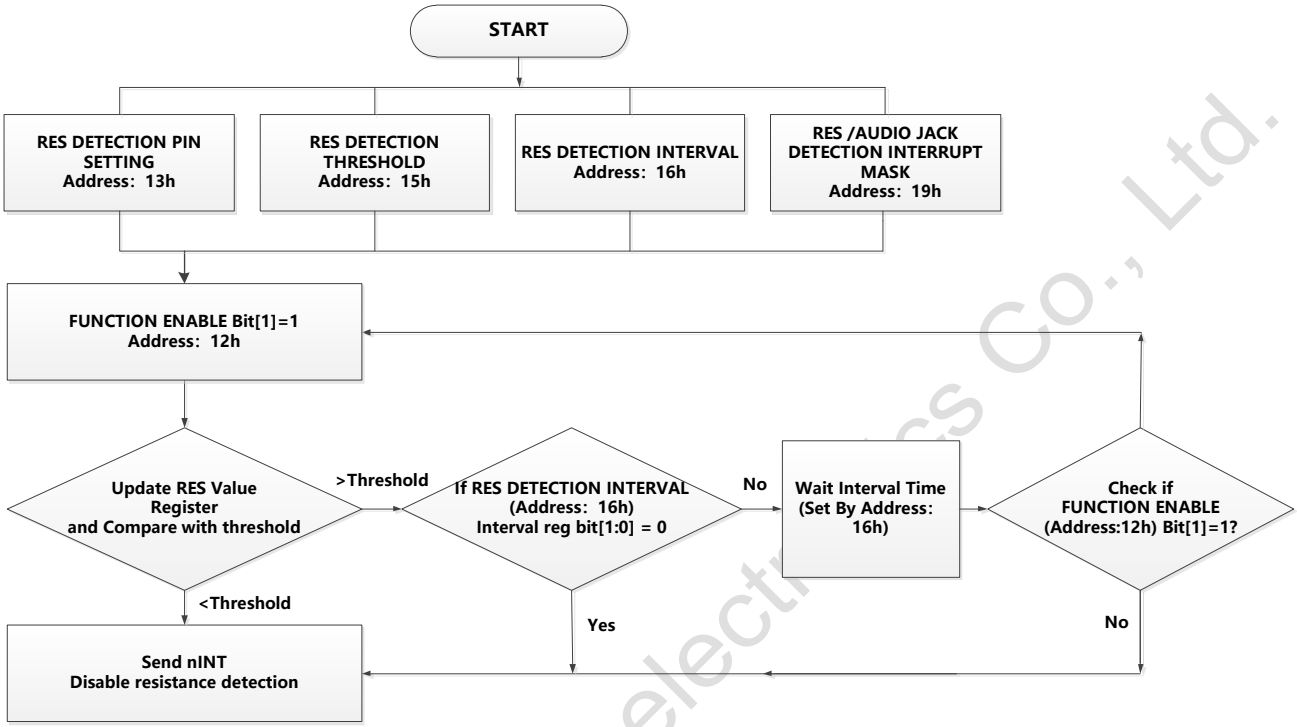


Figure 5, Resistance Detection

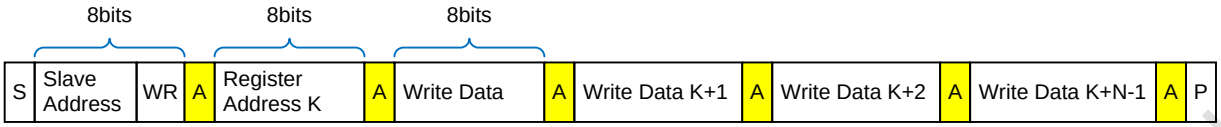
Manual Switch Control

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. it will provide manual control for device. During this configuration, ADDR and nINT pins will be set as logic control input.

Power	nEN	ADDR	nINT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ AGND Switch	SBU Bypass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	ON: DP_R to DP, DN_L to DN	OFF	OFF	ON: SBU1 to SBU1_H, SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	ON: DP_R to DP, DN_L to DN	OFF	OFF	ON: SBU1 to SBU2_H, SBU2 to SBU1_H
ON	L	1	0	ON: GSBU2 to SENSE	ON	OFF	ON: DP_R to R, DN_L to L	ON: SBU1 to MIC, SBU2 to AGND	OFF
ON	L	1	1	ON: GSBU1 to SENSE	ON	OFF	ON: DP_R to R, DN_L to L	ON: SBU2 to MIC, SBU1 to AGND	OFF

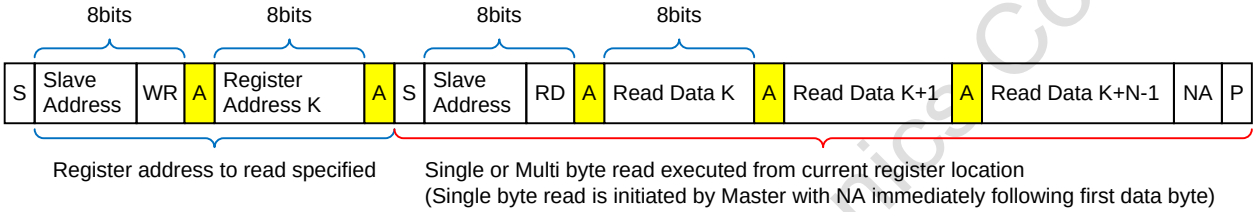
I2C INTERFACE

The ASW5480 includes a full I²C slave controller. The I2C slave fully complies with I²C specification version 2.1 requirements. This block is designed for fast mode, 400-KHz signals. Examples of an I²C write and read sequence are shown in below figures respectively.



NOTE: Single Byte Read is initiated by Master with P immediately following first data byte.

Figure 6, I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

	From Master to Slave	S	Start Condition	NA	Not Acknowledge (SDA High)	RD	Read = 1
	From Slave to Master	A	Acknowledge (SDA Low)	WR	Write = 0	P	Stop Condition

Figure 7, I²C Read Example

Table 1, I²C Slave Address

ADDR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDR = L	1	0	0	0	0	1	0	R/W
ADDR = H	1	0	0	0	0	1	1	R/W

REGISTER MAPS

ADDR	Register Name	Type	Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Device ID	R	0x59	0	1	0	1	1	0	0	1
01H	OVP Interrupt Mask	R/W	0x00	Reserved	Mask OVP Interrupt	Mask OVP /DP_R	Mask OVP /DN_L	Mask OVP /SBU1	Mask OVP /SBU2	Mask OVP /GSBU1	Mask OVP /GSBU2
02H	OVP Interrupt flag	R/C	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
03H	OVP Status	R	0x00	Reserved		OVP /DP_R	OVP /DN_L	OVP /SBU1	OVP /SBU2	OVP /GSBU1	OVP /GSBU2
04H	Switch settings Enable	R/W	0x98	Device Control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
05H	Switch Select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
06H	Switch Status0	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	Audio switch left channel turn on control	R/W	0x01	Audio Switch Left Channel Slow Control [7:0]							
09H	Audio switch right channel turn on control	R/W	0x01	Audio Switch Right Channel Slow Control [7:0]							
0AH	MIC switch turn on control	R/W	0x01	MIC Switch Right Channel Slow Control [7:0]							
0BH	Sense switch turn on control	R/W	0x01	SENSE Switch Right Channel Slow Control [7:0]							
0CH	Audio Ground Switch turn on control	R/W	0x01	Audio Ground Switch Right Channel Slow Control [7:0]							
0DH	Timing Delay between R switch enable and L switch enable	R/W	0x00	Timing Delay Between R Switch Enable and L Switch Enable Control [7:0]							
0EH	Timing Delay between MIC switch enable and L switch enable	R/W	0x00	Timing Delay Between MIC Switch Enable and L Switch Enable Control [7:0]							
0FH	Timing Delay between Sense switch enable and L switch enable	R/W	0x00	Timing Delay Between Sense Switch Enable and L Switch Enable Control [7:0]							
10H	Timing Delay between Audio Ground switch enable and L switch enable	R/W	0x00	Timing Delay Between Audio Ground Switch Enable and L Switch Enable Control [7:0]							
11H	Audio accessory status	R	0x02	Reserved						CC_IN	DET
12H	Function Enable	R/W	0x08	Reserved	DET I/O Control	RES	GPIO Control	Slow turn-on Control	MIC Auto Control	RES detection: auto clear	Audio jack detection: auto clear
13H	RES detection pin setting	R/W	0x00	Reserved					Detection pin select [2:0]		

REGISTER MAPS(CONTINUED)

ADDR	Register Name	Type	Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14H	RES detection value	R	0xFF	R detection value [7:0]							
15H	RES detection interrupt threshold	R/W	0x16	R detection interrupt resistance threshold [7:0]							
16H	RES detection interval	R/W	0x00	Reserved						Detection interval [1:0]	
17H	Audio jack status	RO	0x01	Reserved				4-pole, SBU2 MIC	4-pole, SBU1 MIC	3-pole	No audio
18H	Detection interrupt	R/C	0x00	Reserved					Audio detection done	RES detection occurred	RES detection done
19H	Detection interrupt Mask	R/W	0x00	Reserved					Audio detection done mask	RES detection occurred mask	RES detection done mask
1AH	Audio detection REG1	RO	0xFF	Audio detection value REG1 [7:0]							
1BH	Audio detection REG2	RO	0xFF	Audio detection value REG2 [7:0]							
1CH	MIC threshold DATA0	R/W	0x20	MIC Threshold value DATA0 [7:0]							
1DH	MIC threshold DATA1	R/W	0xFF	MIC Threshold value DATA1 [7:0]							
1EH	I2C reset	W/C	0x00	Reserved							I2C reset
1FH	Current source setting	R/W	0x07	Reserved				Current Source Setting [3:0]			

Table 2, DEVICE ID
(Register 0x00h, Reset Value: 0x59, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:6	Vendor ID	2	Vendor ID
5:3	Version ID	3	Device Version ID
2:0	Revision ID	3	Revision History ID

Table 3, OVP INTERRUPT MASK
(Register 0x01h, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7	Reserved	1	Do not use
6	OVP Interrupt mask control	1	OVP Interrupt function enable/disable 0: controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt

Table 4, OVP INTERRUPT FLAG
(Register 0x02h, Reset Value: 0x00, Type: Read Clear)

BITS	NAME	SIZE	DESCRIPTION
7:6	Reserved	2	Do not use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
2	SBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

Table 5, OVP STATUS
(Register 0x03h, Reset Value: 0x00, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:6	Reserved	2	Do not use
5	OVP on DP_R Pin	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L Pin	1	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 Pin	1	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 Pin	1	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 Pin	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 Pin	1	0: OVP event has not occurred 1: OVP event has occurred

Table 6, SWITCHING SETTING ENABLE
(Register 0x04h, Reset Value: 0x98, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7	Device Enable	1	0: Device Disable; L, R are pulled-down by 10kΩ and other switch nodes will be High-Z for positive input. 1: Device Enable.
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be High-Z for positive input; 1: Switch Enable.
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be High-Z for positive input; 1: Switch Enable.
4	DN_L to DN or L switches	1	0: Switch Disable; DN_L, DN will be High-Z for positive input and L is pulled-down by 10kΩ. 1: Switch Enable.
3	DP_R to DP or R switches	1	0: Switch Disable; DP_R, DP will be High-Z for positive input and R is pulled-down by 10kΩ. 1: Switch Enable.
2	Sense to GSBUx switches	1	0: Switch Disable; Sense, GSBU1 and GSBU2 will be High-Z for positive input. 1: Switch Enable.
1	MIC to SBUx switches	1	0: Switch Disable; MIC will be High-Z for positive input. 1: Switch Enable.
0	AGND to SBUx switches	1	0: Switch Disable; AGND will be High-Z for positive input. 1: Switch Enable.

Table 7, SWITCH SELECT
(Register 0x05h, Reset Value: 0x18, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7	Reserved	1	Do not use
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L or DN or L switches	1	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R or DP or R switches	1	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

Table 8, SWITCH STATUS0
(Register 0x06h, Reset Value: 0x05, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:6	Reserved	2	Do not use
5:4	Sense Switch Status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not Valid
3:2	DP_R Switch Status	2	00: DP_R switch is Open/Not Connected 01: DP_R connected to DP 10: DP_R connected to R 11: Not Valid
1:0	DN_L Switch Status	2	00: DN_L switch is Open/Not Connected 01: DN_L connected to DN 10: DN_L connected to L 11: Not Valid

Table 9, SWITCH STATUS1
(Register 0x07h, Reset Value: 0x00, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:6	Reserved	2	Do not use
5:3	SBU2 SwitchStatus	3	000: SBU2 switch is Open/Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
2:0	SBU1 SwitchStatus	3	000: SBU1 switch is Open/Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

Table 10, AUDIO SWITCH LEFT CHANNEL SLOW TURN-ON
(Register 0x08h, Reset Value: 0x01, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Switch turn on rising time setting	8	11111111: 25600μs … 00000001: 200μs 00000000: 100μs

Table 11, AUDIO SWITCH RIGHT CHANNEL SLOW TURN-ON
(Register 0x09h, Reset Value: 0x01, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Switch turn on rising time setting	8	11111111: 25600μs
			…
			00000001: 200μs
			00000000: 100μs

Table 12, MIC SWITCH SLOW TURN-ON
(Register 0x0Ah, Reset Value: 0x01, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Switch turn on rising time setting	8	11111111: 25700μs
			…
			00000010: 350μs
			00000001: 250μs
			00000000: Not Valid

Table 13, SENSE SWITCH SLOW TURN-ON
(Register 0x0Bh, Reset Value: 0x01, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Switch turn on rising time setting	8	11111111: 25600μs
			…
			00000001: 200μs
			00000000: 100μs

Table 14, AUDIO GROUND SWITCH SLOW TURN-ON
(Register 0x0Ch, Reset Value: 0x01, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Switch turn on rising time setting	8	11111111: 179000μs
			…
			00000001: 1400μs
			00000000: 700μs

Table 15, TIMING DELAY BETWEEN R SWITCH ENABLE AND L SWITCH ENABLE
(Register 0x0Dh, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Delay timing setting	8	11111111: 25500μs
			11111110: 25400μs
			…
			00000001: 100μs
			00000000: 0μs

Table 16, TIMING DELAY BETWEEN MIC SWITCH ENABLE AND L SWITCH ENABLE
(Register 0x0Eh, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Delay timing setting	8	11111111: 25500μs
			11111110: 25400μs
			…
			00000001: 100μs
			00000000: 0μs

Table 17, TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE
(Register 0x0Fh, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Delay timing setting	8	11111111: 25500μs
			11111110: 25400μs
			…
			00000001: 100μs
			00000000: 0μs

Table 18, TIMING DELAY BETWEEN AUDIO GROUND SWITCH ENABLE AND L SWITCH ENABLE
(Register 0x10h, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	Delay timing setting	8	11111111: 25500μs 11111110: 25400μs … 00000001: 100μs 00000000: 0μs

Table 19, AUDIO ACCESSORY STATUS
(Register 0x11h, Reset Value: 0x02, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:2	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2V 1: CC_IN > 1.5V
0	DET	1	0: DET output is Low 1: DET output is High

Table 20, FUNCTION ENABLE
(Register 0x12h, Reset Value: 0x08, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7	Reserved	1	Do not use
6	DET I/O Control	1	1: DET pin is in Open/Drain Configuration 0: DET pin is in Push/Pull Configuration
5	RES detection range setting	1	1: 10KΩ to 2560KΩ 0: 1KΩ to 256KΩ
4	GPIO control enable	1	1: Enable 0: Disable
3	Slow turn on control enable	1	1: Enable 0: Disable
2	MIC auto break out control enable	1	1: Enable 0: Disable
1	RES detection enable	1	1: Enable; will be changed to '0' after low resistance detection 0: Disable
0	Audio jack detection and configuration enable	1	1: Enable; will be changed to '0' after audio jack detection and configuration 0: Disable

Table 21, RES DETECTION PIN SETTING
(Register 0x13h, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:3	Reserved	5	Do not use
2:0	Pin Selection	3	000: CC_IN 001: DP_R 010: DN_L 011: SBU1 100: SBU2 101…111: Do not use

Note: if RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

Table 22, RES VALUE
(Register 0x14h, Reset Value: 0xFF, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:0	Detected resistance value	8	00000000: R < 1KΩ … 11111111: R > 300KΩ

Table 23, RES DETECTION THRESHOLD
(Register 0x15h, Reset Value: 0x16, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	RES detection threshold	8	Selection by 1KΩ per step if Register 12h[5] = 0 Selection by 10KΩ per step if Register 12h[5] = 1 Default Value = 22KΩ 00000000: 1KΩ/10KΩ … 11111111: 256KΩ/2560KΩ

Table 24, RES DETECTION INTERVAL
(Register 0x16h, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:2	Reserved	6	Do not use
1:0	RES detection interval	2	00: Single 01: 100ms 10: 1s 11: 10s

Table 25, AUDIO JACK STATUS
(Register 0x17h, Reset Value: 0x01, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:4	Reserved	4	Do not use
3	4pole	1	1: 4 pole SBU2 to MIC, SBU1 to Audio Ground 0: others
2	4pole	1	1: 4 pole SBU1 to MIC, SBU2 to Audio Ground 0: others
1	3pole	1	1: 3 pole 0: others
0	No Audio Accessory	1	1: No Audio Accessory 0: Audio Accessory Attached

Table 26, RES DETETCTION/AUDIO JACK DETECTION INTERRUPT FLAG
(Register 0x18h, Reset Value: 0x00, Type: Read Clear)

BITS	NAME	SIZE	DESCRIPTION
7:3	Reserved	5	Do not use
2	Audio jack detection and configuration	1	1: Audio jack detection and configuration has not occurred 0: Audio jack detection and configuration has occurred
1	Low resistance occurred	1	1: Low resistance has not occurred 0: Low resistance has occurred
0	Low resistance detection	1	1: Low resistance detection has not occurred 0: Low resistance detection has occurred

Table 27, RES DETETCTION /AUDIO JACK DETECTION INTERRUPT MASK
(Register 0x19h, Reset Value: 0x00, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:3	Reserved	5	Do not use
2	Audio jack detection and configuration	1	1: Mask Audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1	1: Low resistance has occurred interrupt
0	Low resistance detection	1	1:Low resistance detection has occurred interrupt

Table 28, AUDIO JACK DETECTION REG1 VALUE
(Register 0x1Ah, Reset Value: 0xFF, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:0	Audio jack detection value	8	Resistance between SBU1 to SBU2

Table 29, AUDIO JACK DETECTION REG2 VALUE
(Register 0x1Bh, Reset Value: 0xFF, Type: Read)

BITS	NAME	SIZE	DESCRIPTION
7:0	Audio jack detection value	8	Resistance between SBU2 to SBU1

Table 30, MIC DETECTION THRESHOLD DATA0
(Register 0x1Ch, Reset Value: 0x20, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	MIC detection threshold DATA0	8	MIC detection threshold DATA0 00100000: 300mV

Table 31, MIC DETECTION THRESHOLD DATA1
(Register 0x1Dh, Reset Value: 0xFF, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:0	MIC detection threshold DATA1	8	MIC detection threshold DATA1 11111111: 2400mV

Table 32, I2C RESET
(Register 0x1Eh, Reset Value: 0x00, Type: Write/Clear)

BITS	NAME	SIZE	DESCRIPTION
7:1	Reserved	7	Do not use
0	I2C Reset	1	0: default 1: I^2C reset

Table 33, CURRENT SOURCE SETTING
(Register 0x1Fh, Reset Value: 0x07, Type: Read/Write)

BITS	NAME	SIZE	DESCRIPTION
7:4	Reserved	4	Do not use
3:0	Current Source Setting	4	1111: 1500μA 0111: 700μA … 0001: 100μA 0000: Invalid

TEST CIRCUITS

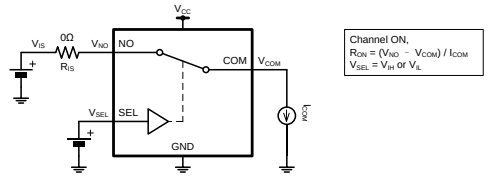


Figure 8, ON Resistance (R_{ON})

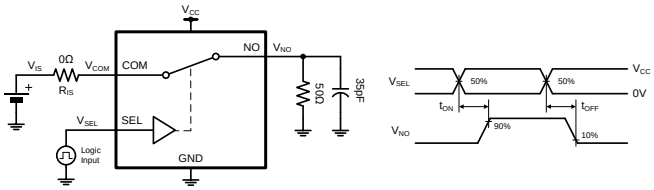


Figure 9, Turn-On and Turn-Off Time (t_{ON}/t_{OFF})

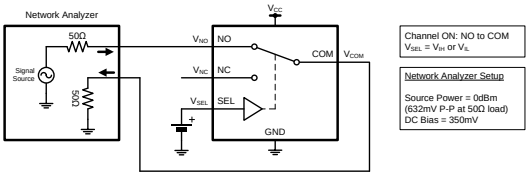


Figure 10, ON Channel -3dB Bandwidth (BW)

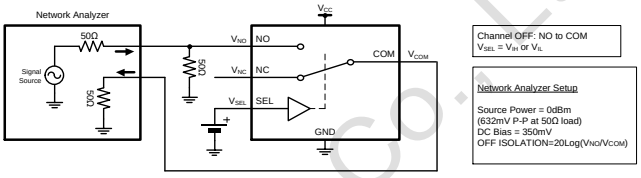


Figure 11, OFF Isolation (O_{ISO})

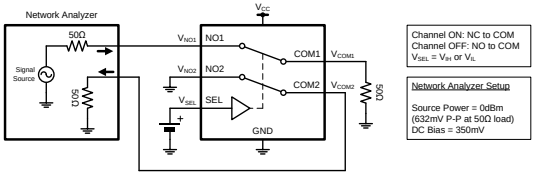


Figure 12, Chanel-to-Chanel Crosstalk (X_{TALK})

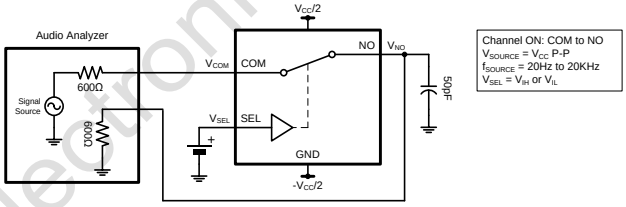
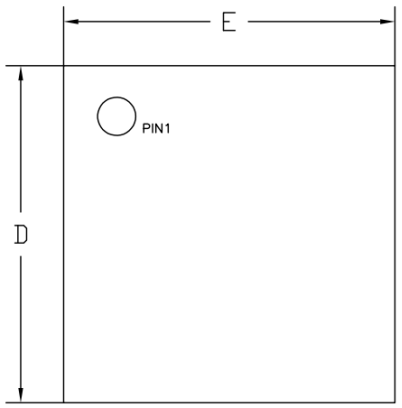
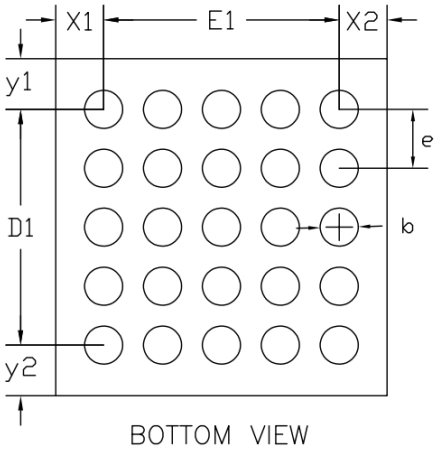


Figure 13, Total Harmonic Distortion (THD+N)

PACKAGE OUTLINE (CSP25-2.28x2.24)



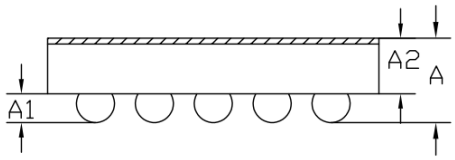
TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

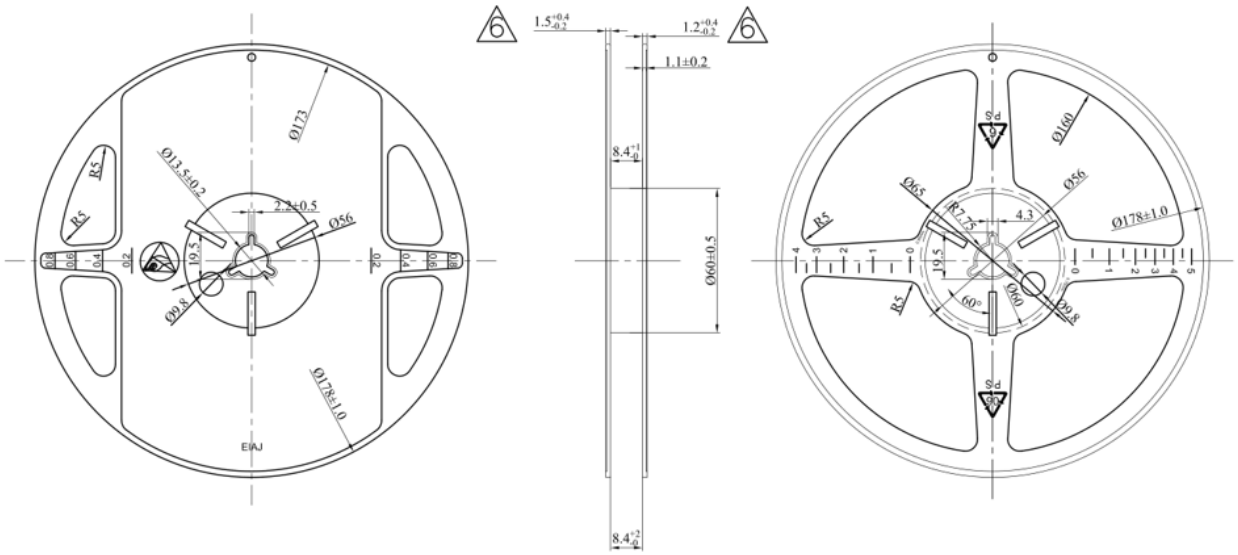
SYMBOL	MIN	NOM	MAX
A	0.529	0.574	0.619
A1	0.176	0.196	0.216
A2	0.353	0.378	0.403
D	2.2582	2.2882	2.3182
D1		1.600BSC	
E	2.2182	2.2482	2.2782
E1		1.600BSC	
b	0.240	0.260	0.280
e		0.400BSC	
x1		0.3241 REF	
x2		0.3241 REF	
y1		0.3441 REF	
y2		0.3441 REF	



SIDE VIEW

TAPE AND REEL INFORMATION

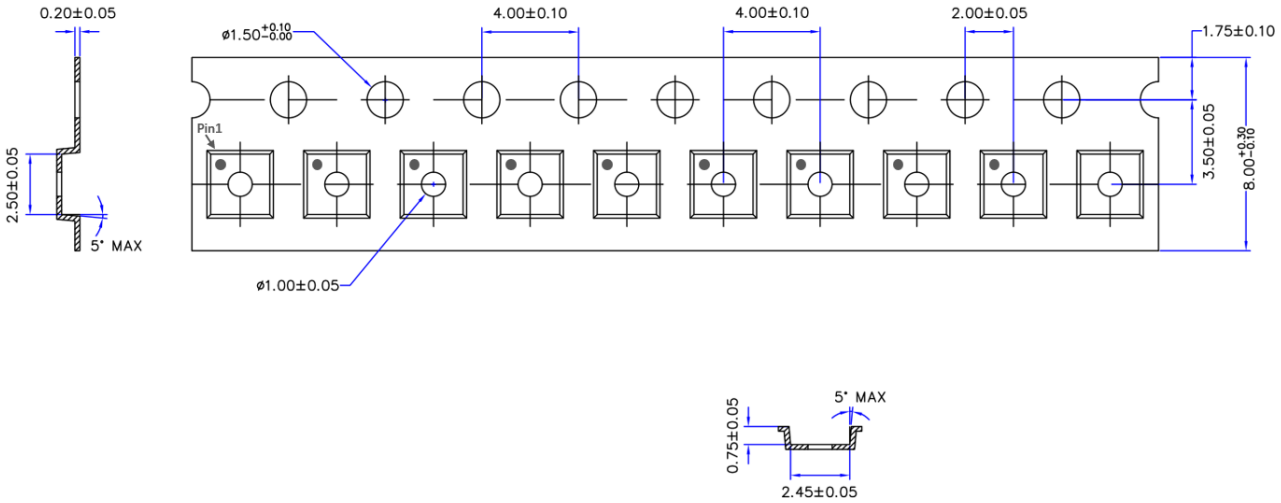
REEL



注意 ：

1. 材料 ： 聚苯乙烯（黑色）；
2. 平整度 ： 最大允许2毫米；
3. 所有尺寸为毫米；
4. 表面电阻 ： 10^5 TO 10^{10} OHMS/SQ.
5. 所有未注公差 ： ±0.25。

TAPE



NOTES：

1. ALL DIMS IN MM
2. MATERIAL：BLACK CONDUCTIVE PC
3. 10 sprocket hole pitch cumulative tolerance ±0.20mm
4. Carrier camber is within 1mm in 250mm
5. There must not be foreign body adhesion and the state of the surface must be excellent
6. Surface resistance 1X10E4≤Rs<1X10E9 OHMS/SQ
7. 17" PLASTIC-Reel，121250 pockets（485m）

产品订购信息

器件编号	产品丝印	工作温度范围	封装信息	湿敏等级	包装方法
ASW5480WLG	A80 YYWW(*)	-40°C 至 +85°C	WLCSP25-2.28x2.24	MSL-3	卷带和卷盘 (每卷 3000 只)

注：(*) YY 表示年号，WW 表示周号。

单击下面可查看定价，库存，交付和生命周期等信息

>>GrandMicro(有容微)