GPL6301 Series

18V Low Current Consumption
300mA CMOS Voltage Regulator

Introduction

The GPL6301 series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The GPL6301 series can deliver 300mA output current and allow an input voltage as high as 18V. The series are very suitable for the battery-powered equipment, such as RF applications and other systems requiring a quiet voltage source.

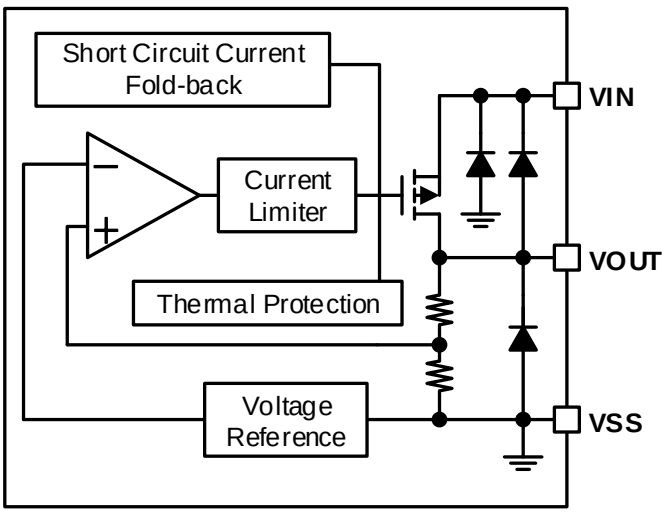
Features

- Low Quiescent Current: 2μA
- Operating Voltage Range: 2.5V～18V
- Output Current: 300mA
- Low Dropout Voltage: 160mV@100mA (VOUT=5V)
- Output Voltage: 1.2~ 5.0V
- High Accuracy: ±1%（Typ.）
- High Power Supply Rejection Ratio: 65dB@1kHz
- Low Output Noise:27xV_{OUT}μV_{RMS} (10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection
- Over-Temperature Protection

Applications

- Cordless Phones
- Radio control systems
- Laptop, Palmtops and PDAs
- Single-lens reflex DSC
- PC peripherals with memory
- Wireless Communication Equipment
- Portable Audio Video Equipment
- Car Navigation Systems
- LAN Cards
- Ultra-Low Power Microcontrollers

Block Diagram



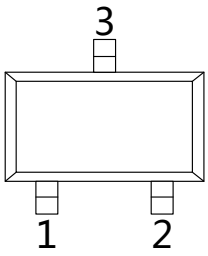
Order Information

GPL6301①②③④

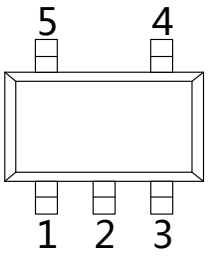
Designator	Symbol	Description
①②③	Integer	Output Voltage e.g.1.8V=①:V, ②:1,③:8
④	K3	Package:SOT-23-3L
	K5	Package:SOT-23-5L
	KE	Package:SOT-89-3L
	KT	Package:SOT-89-5L
	H4	Package:WBFBP-04C(2B)

Pin Configuration

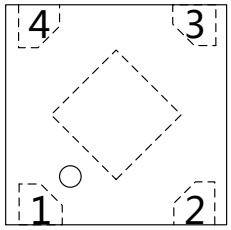
SOT-23-3L



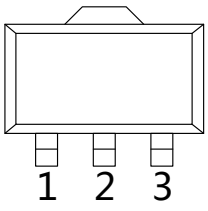
SOT-23-5L



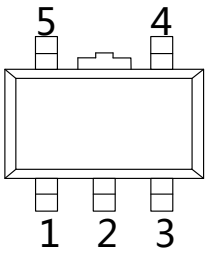
WBFBP-04C(DFN1*1-4)



SOT-89-3L



SOT-89-5



SOT-23-3L & SOT-89-3L

Pin Number		Pin Name	Function
SOT-23-3L	SOT-89-3L		
1	1	V_{SS}	Ground
2	3	V_{OUT}	Output
3	2	V_{IN}	Power input

SOT-23-5L & SOT-89-5L

Pin Number		Pin Name	Function
SOT-23-5L	SOT-89-5L		
1	5	V_{IN}	Power Input Pin
2	2	V_{SS}	Ground
3	4	CE	Chip Enable Pin
4	3	NC	No Connection
5	1	V_{OUT}	Output Pin

WBFBP-04C(DFN1*1-4)

Pin Number	Pin Name	Function
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{OUT}	Output Pin

Absolute Maximum Ratings[1] (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Ratings	Units
Input Voltage[2]	V_{IN}	-0.3~24	V
Output Voltage[2]	V_{OUT}	-0.3~10	V
CE Pin Voltage	V_{CE}	-0.3~24	V
Output Current	I_{OUT}	300	mA
Power Dissipation	P_D	0.4	W
Operating Junction Temperature Range[3]	T_j	-40~125	°C
Storage Temperature	T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)	T_{solder}	260	°C
ESD rating[4]	Human Body Model -(HBM)	8	kV
	Machine Model- (MM)	400	V

1) Stresses beyond those listed under *absolute maximum ratings may* cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
2) All voltages are with respect to network ground terminal.
3) This GPL6301 includes over temperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.
4) ESD testing is performed according to the respective JESD22 JEDEC standard.The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Themachine model is a 200pF capacitor discharged directly into each pin.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Units
Supply voltage at V_{IN}	2.5		18	V
Operating junction temperature range, T_j	-40		125	°C
Operating free air temperature range, T_A	-40		85	°C

Electrical Characteristics

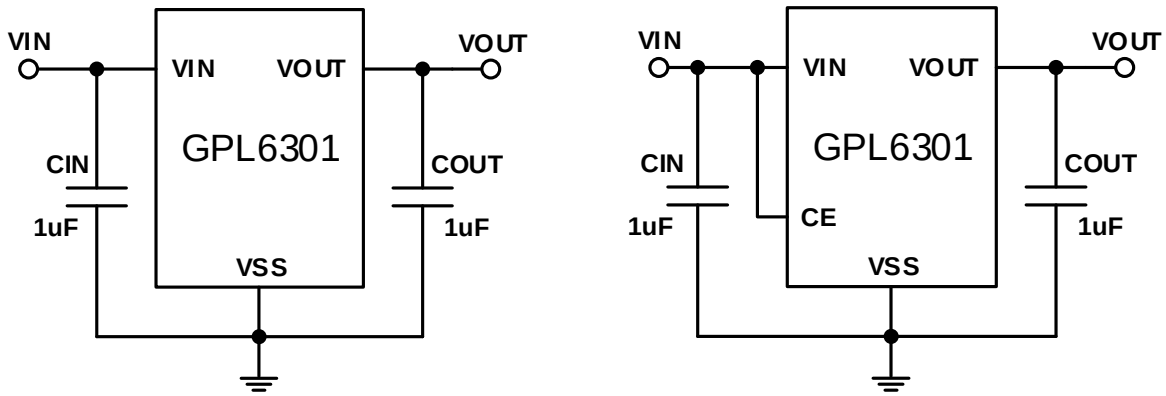
GPL6301 Series (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.[5]	Max.	Units
Input Voltage	V_{IN}			2.5		18	V
Output Voltage Range	V_{OUT}			1.2		5	V
DC Output Accuracy		I_{OUT}=1mA		-1		1	%
Dropout Voltage	V_{dif}[6]	I_{OUT} =100mA,V_{OUT}=5V			160		mV
Supply Current	I_{SS}	I_{OUT}=0A			2	5	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤18V			0.01	0.3	%/V
Load Regulation	ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA			10		mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	I_{OUT}=10mA, -40°C<T_A<125°C			50		ppm
Output Current Limit	I_{LIM}	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN} = 7V		350	500		mA
Short Current	I_{SHORT}	V_{OUT} =V_{SS}			25		mA
Power Supply Rejection Ratio	PSRR	I_{OUT}=50mA	100Hz		80		dB
			1kHz		65		
			10kHz		50		
			100kHz		45		
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz			27 x V_{OUT}		μV_{RMS}
Thermal Shutdown Temperature	T_{SD}				150		°C
Thermal Shutdown Hysteresis	ΔT_{SD}				20		°C

5) Typical numbers are at 25°C and represent the most likely norm.

6) V_{dif}: The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

Typical Application Circuit



Application Information

Selection of Input/ Output Capacitors

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current.

A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC/DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

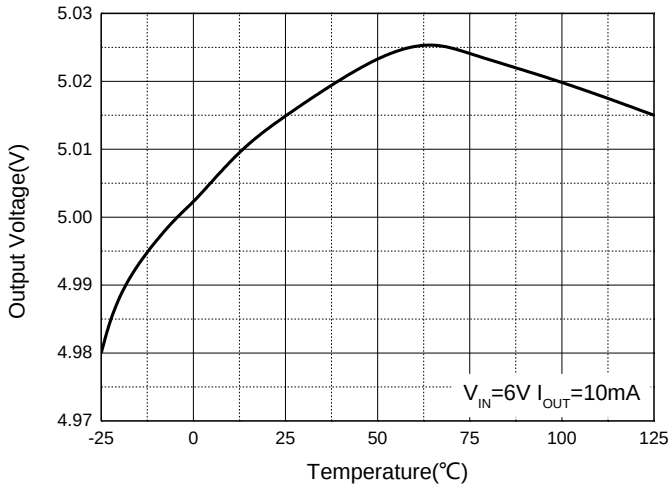
Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step. (See “Ceramic Input Capacitors Can Cause Overvoltage Transients”---Linear Technology application note 88, March 2001)

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

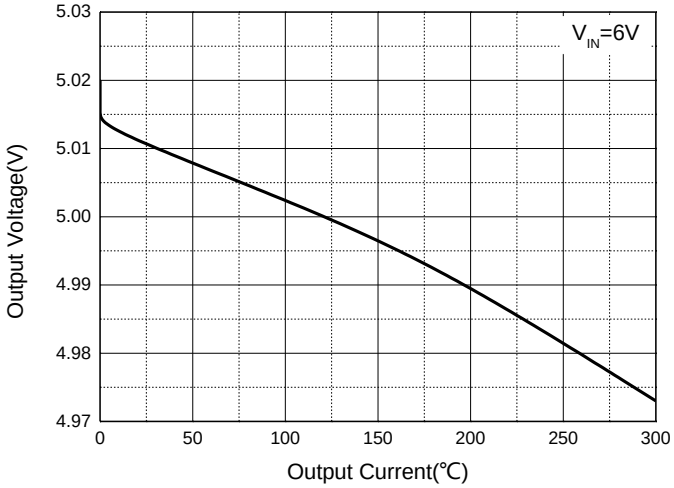
The LDO also requires an output capacitor for loop stability. Connect a 1μF tantalum capacitor from OUT to GND close to the pins. For improved transient response, this output capacitor may be ceramic.

Typical Performance Characteristics

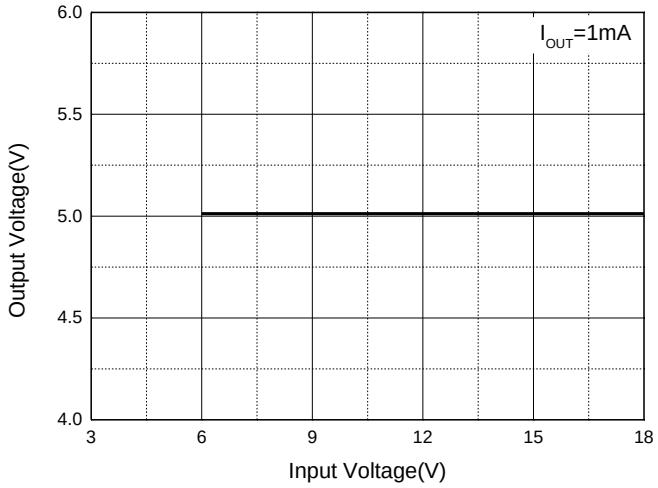
Output Voltage vs. Temperature



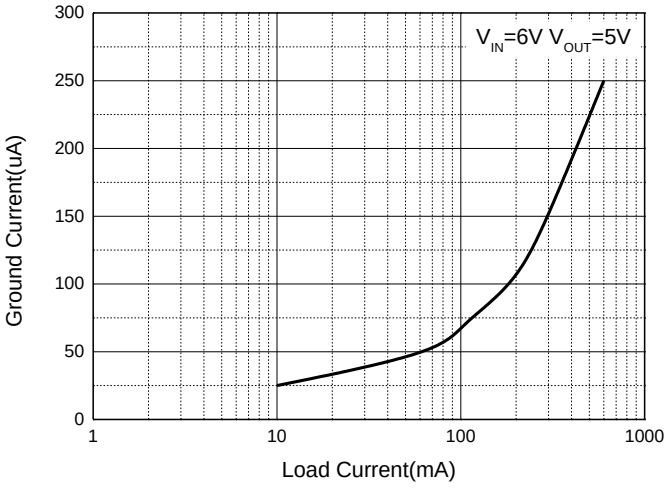
Output Voltage vs. Output Current



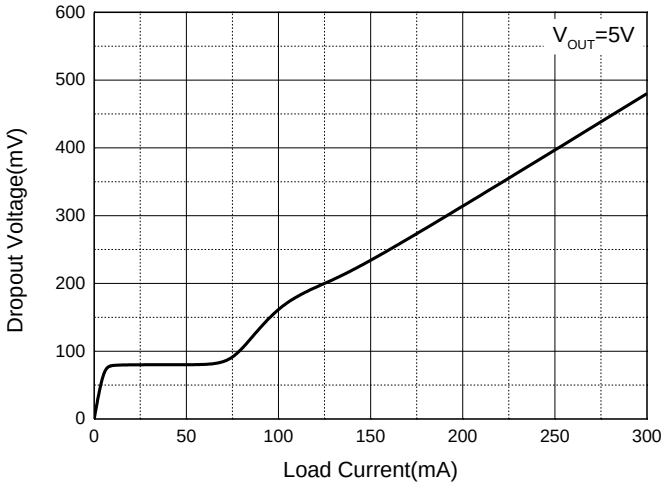
Output Voltage vs. Input Voltage



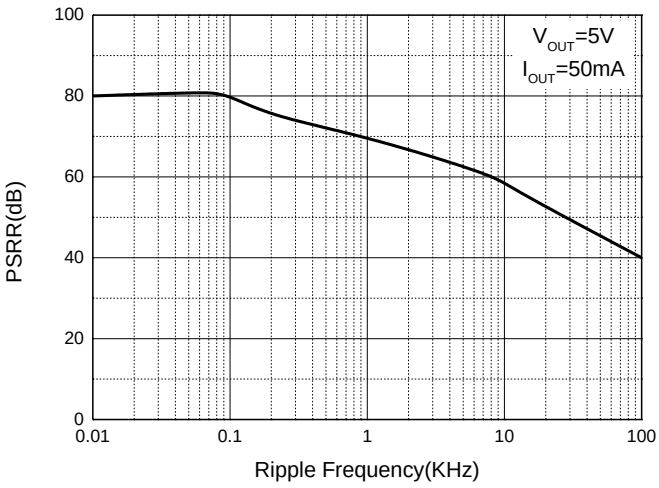
Ground Current VS. Load Current



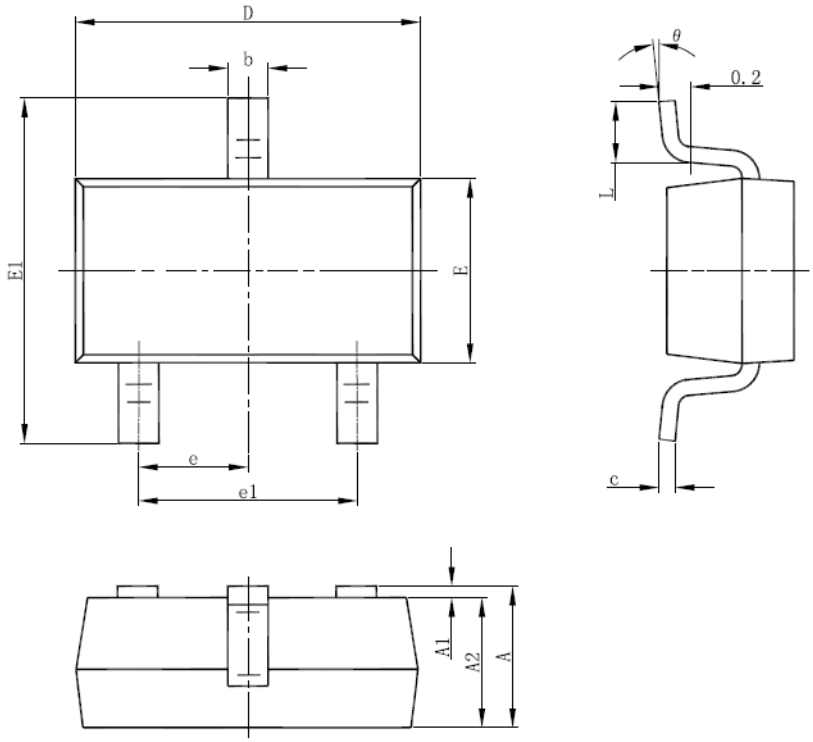
Dropout Voltage vs. Load Current



PSRR vs. Frequency(Vin=6V+aV$_{P-P}$AC)

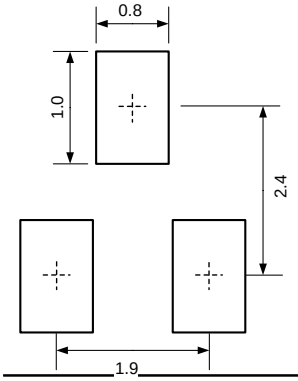


SOT-23-3L Package Outline Dimensions



Symbol	Dimensions in millimeters		
	Min.	Typ.	Max.
A	1.050	-	1.250
A1	0.000	-	0.100
A2	1.050	-	1.150
b	0.300	-	0.500
c	0.100	-	0.200
D	2.820	-	3.020
E	1.500	-	1.700
E1	2.650	-	2.950
e	0.950TYP		
e1	1.800	-	2.000
L	0.300	-	0.600
θ	0°	-	8°

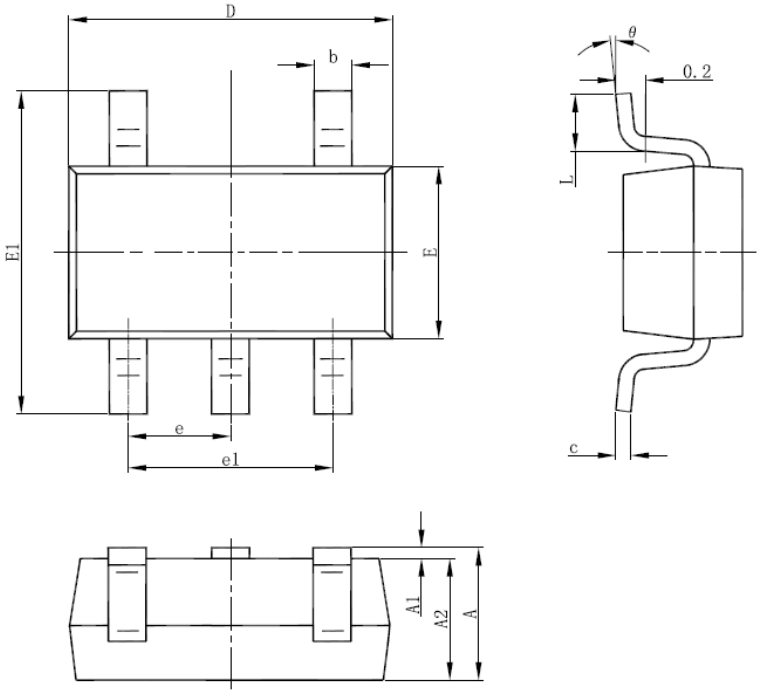
SOT-23-3L Suggested Pad Layout (Unit: mm)



Notes:

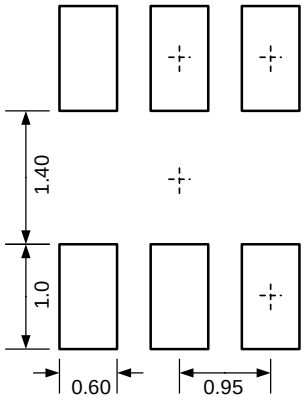
1. General tolerance: ±0.05mm.
2. The pad layout is for reference purposes only.

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

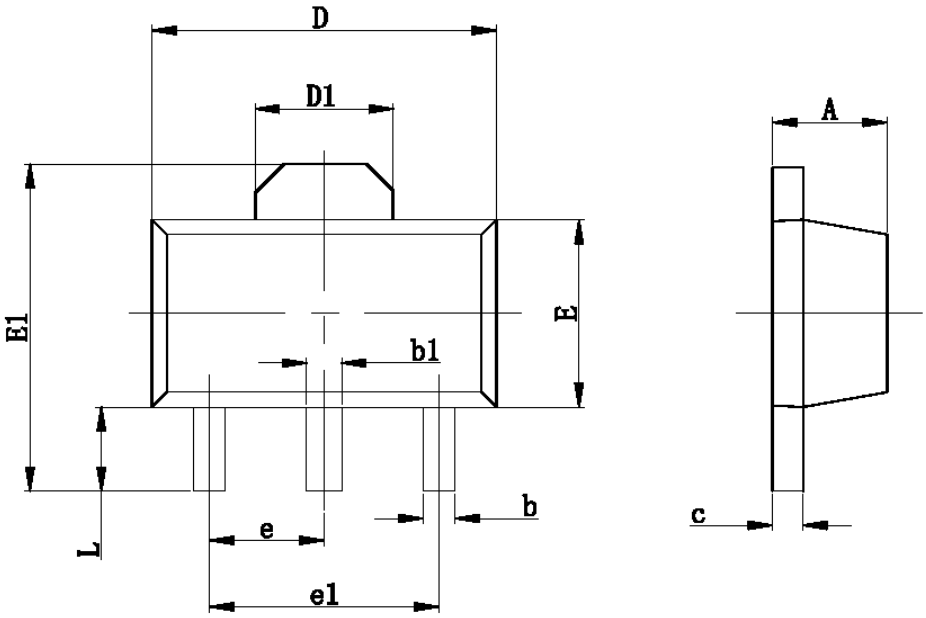
SOT-23-5L Suggested Pad Layout (Unit: mm)



Notes:

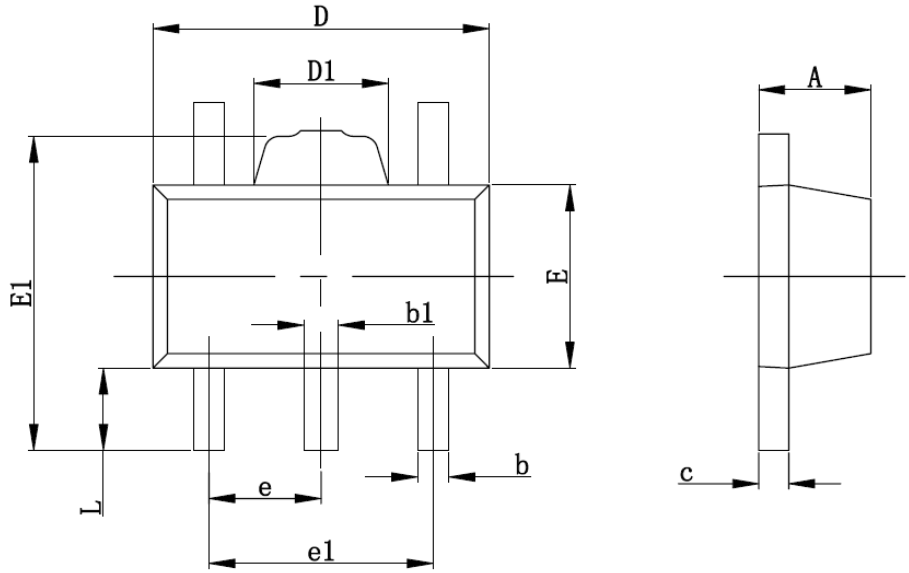
1. General tolerance:±0.05mm.
2. The pad layout is for reference purposes only.

SOT-89-3L Package Outline Dimensions



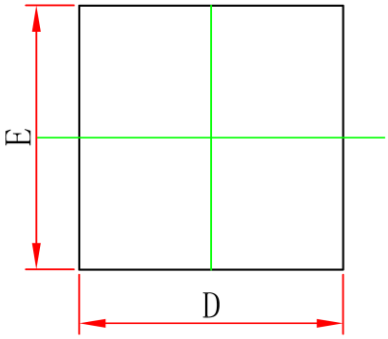
Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550REF		0.061REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	3.000TYP		0.118TYP	
L	0.900	1.200	0.035	0.047

SOT-89-5L Package Outline Dimensions

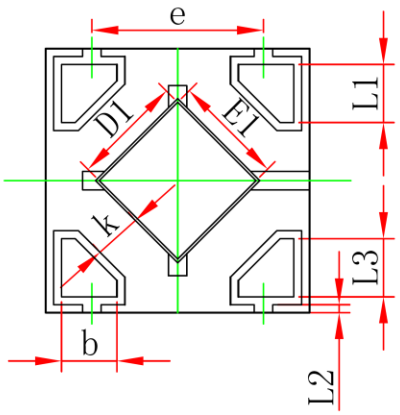


Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.400	1.800	0.055	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043

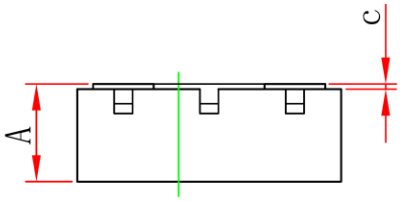
WBFBP-04C Package Outline Dimensions



TOP VIEW
[顶视图]



BOTTOM VIEW
[背视图]



SIDE VIEW
[侧视图]

Symbol	Dimensions in millimeters		Dimensions in inches	
	Min.	Max.	Min.	Max.
A	0.335	0.495	0.013	0.016
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.037	0.047	0.015	0.019
E1	0.037	0.047	0.015	0.019
k	0.17MIN		0.007MIN	
b	0.160	0.260	0.006	0.010
c	0.010	0.090	0.000	0.004
e	0.600	0.700	0.024	0.028
L1	0.185	0.255	0.007	0.010
L2	0.030REF		0.001REF	
L3	0.185	0.255	0.007	0.010

单击下面可查看定价，库存，交付和生命周期等信息

>>GP(格瑞宝)