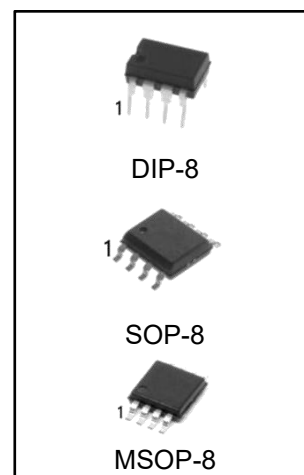


DC-to- DC Converter Control Circuits

FEATURES

- Operation from 3.0V to 40V input
- Low standby current
- Current limiting
- Output switch current up to 1.5A
- Adjustable output voltage
- Operation at frequencies up to 100kHz
- Precision reference (2%)



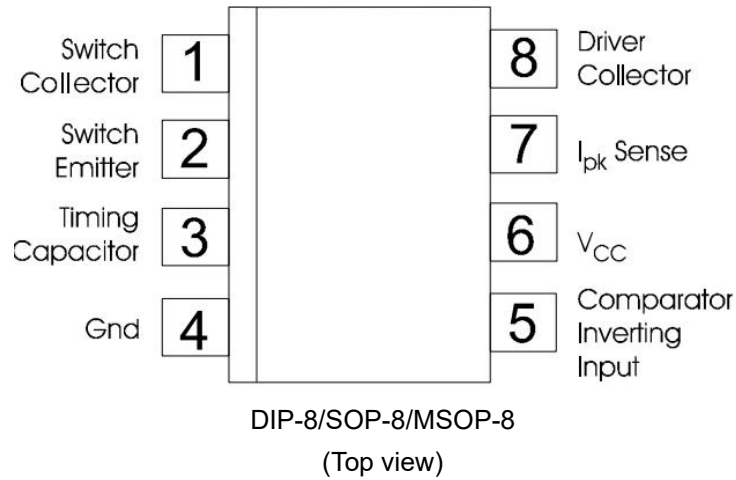
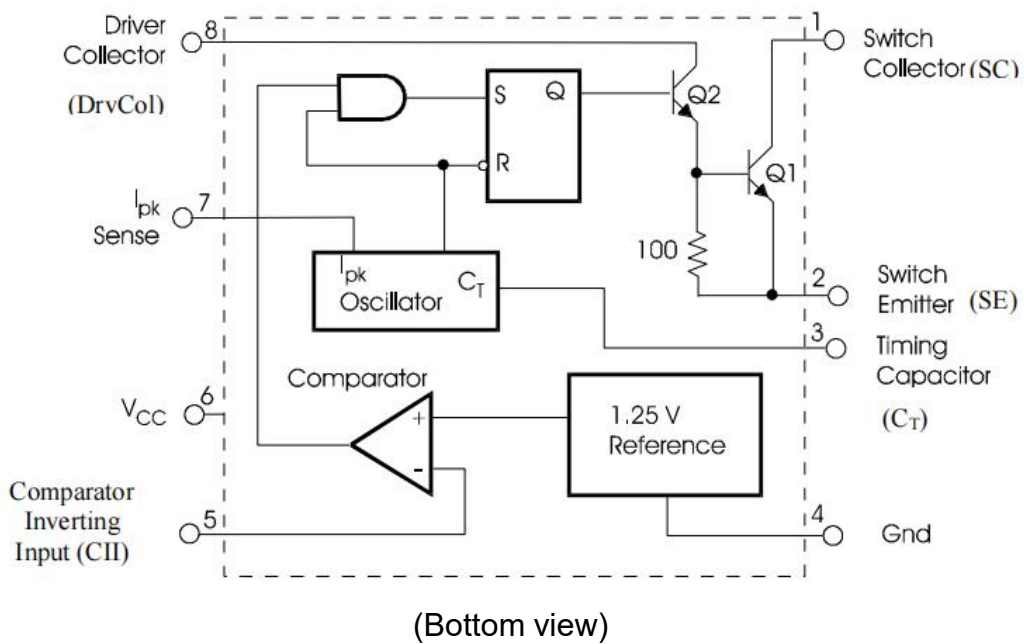
ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
MC33063P	DIP-8	MC33063	TUBE	2000pcs/box
MC33063DRG	SOP-8	MC33063	REEL	2500pcs/reel
MC33063DGKRG	MSOP-8	33063	REEL	2500pcs/reel

DESCRIPTION

The MC33063 series is a monolithic control circuit containing primary functions required for DC-to-DC converters.

These devices consist of an internal temperature-compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in step-down and step-up and voltage-inverting applications with a minimum number of external components.

PIN CONNECTIONS

SCHEMATIC DIAGRAM


ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	40	V
Comparator input voltage range	V_{IR}	-0.3 to +40	V
Switch collector voltage	$V_{C(Switch)}$	40	V
Switch emitter voltage ($V_{Pin1}=40V$)	$V_{E(Switch)}$	40	V
Switch collector-to-emitter voltage	$V_{CE(Switch)}$	40	V
Driver collector voltage	$V_{C(Driver)}$	40	V
Driver collector current (Note 1)	$I_{C(Driver)}$	100	mA
Switch current	I_{Sw}	1.5	A
Operating junction temperature	T_J	+150	°C
Operating ambient temperature range	T_A	-40 to +85	°C
Storage temperature range	T_{STG}	-65 to +150	°C
ESD (HBM)		2500	V
Lead Temperature (Soldering, 10 seconds)	T_L	245	°C

Note: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0V$, $T_A=T_{Low}$ to T_{High} , unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin5}=0V$, $C_T=1.0nF$, $T_A=25^\circ C$)	fosc	24	33	42	kHz
Charge current ($V_{CC}=5.0V$ to $40V$, $T_A=25^\circ C$)	Ichg	24	35	42	μA
Discharge current ($V_{CC}=5.0V$ to $40V$, $T_A=25^\circ C$)	Idischg	140	220	260	μA
Discharge-to-charge current ratio (Pin7 to V_{CC} , $T_A=25^\circ C$)	Idischg/Ichg	5.2	6.5	7.5	-
Current limit sense voltage (Ichg=Idischg, $T_A=25^\circ C$)	Vlpk(sense)	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation voltage, Darlington connection $I_{Sw}=1.0A$, Pins1, 8 connected	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation voltage, Darlington connection ($I_{Sw}=1.0A$, $R_{Pin8}=82\Omega$ to V_{CC} , forced $\beta=20$)	$V_{CE(sat)}$	-	0.45	0.7	V
DC current gain ($I_{Sw}=1.0A$, $V_{CE}=5.0$, $T_A=25^\circ C$)	h_{FE}	50	75	-	-
Collector off-state current ($V_{CE}=40V$)	$I_{C(off)}$	-	1.0	100	μA
COMPARATOR					
Threshold voltage	V_{th}	1.225 1.21	1.25 -	1.275 1.29	V
Threshold voltage line regulation ($V_{CC}=3.0V$ to $40V$)	Reg _{line}	-	1.4	5.0	mV
Input bias current ($V_{in}=0V$)	I_{IB}	-	-20	-400	nA
TOTAL DEVICE					
Supply current ($V_{CC}=5.0V$ to $40V$, $C_T=1.0nF$, Pin7= V_{CC} , $V_{Pin5}>V_{th}$, Pin2 =Gnd, remaining pins - open)	I_{CC}	-	-	4.0	mA

Notes: 1. Maximum package power dissipation limits must be observed.

2. Low duty cycle pulse techniques are used during the test to maintain the junction temperature as close to the ambient temperature as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

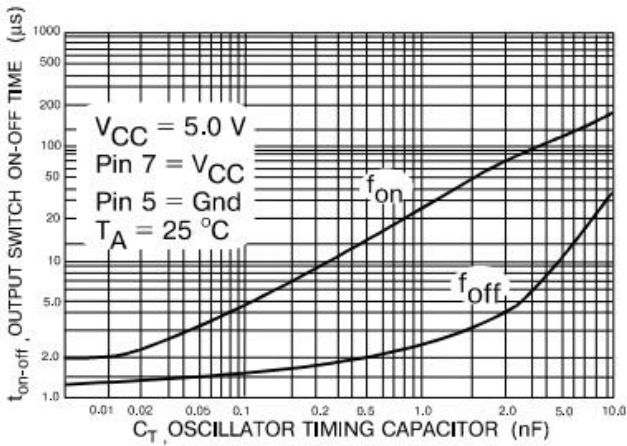


Fig.1. Output Switch on-off time versus Oscillator timing capacitor

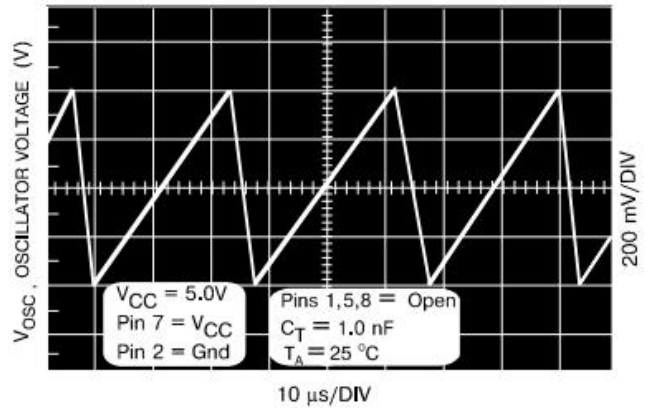


Fig.2. Timing capacitor waveform

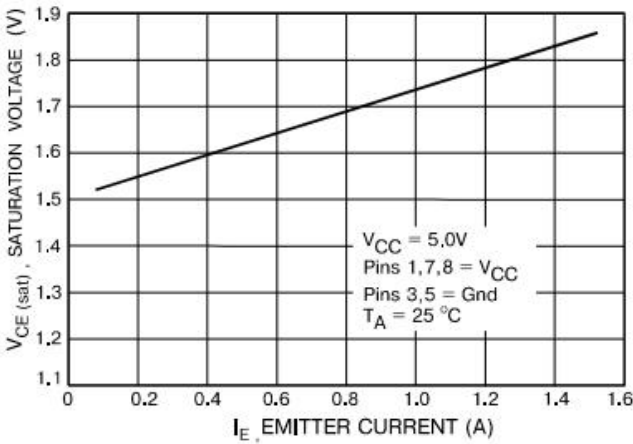


Fig.3. Emitter follower configuration output saturation voltage versus Emitter current

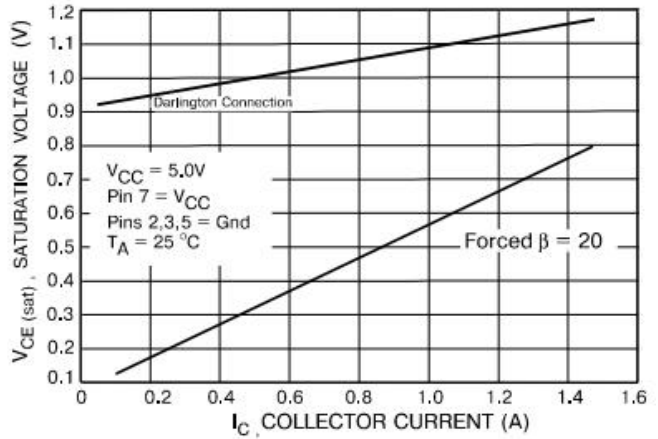


Fig.4. Common emitter configuration output saturation voltage versus Collector current

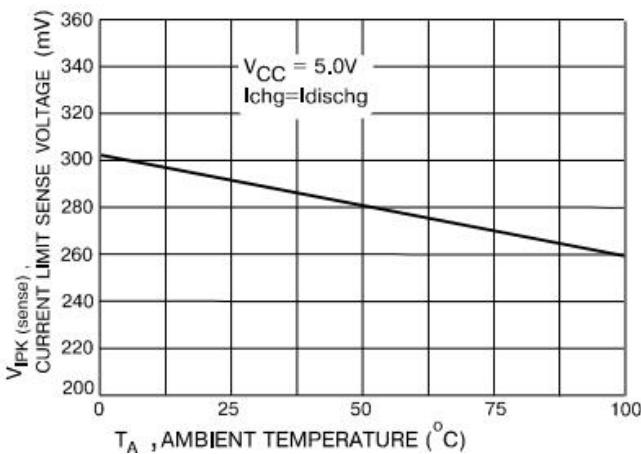


Fig.5. Current limit sense voltage versus Temperature

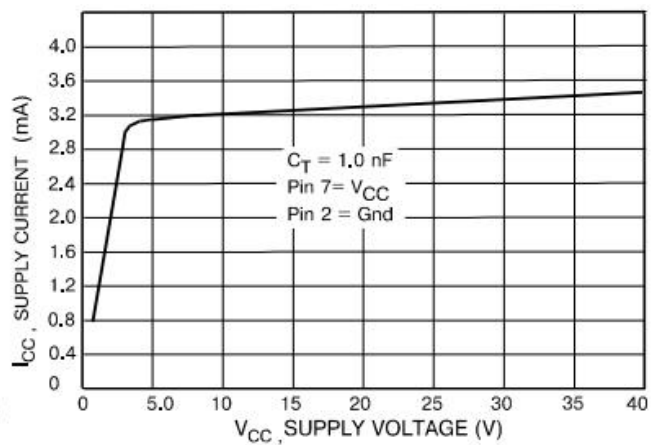


Fig.6. Standby supply current versus Supply voltage

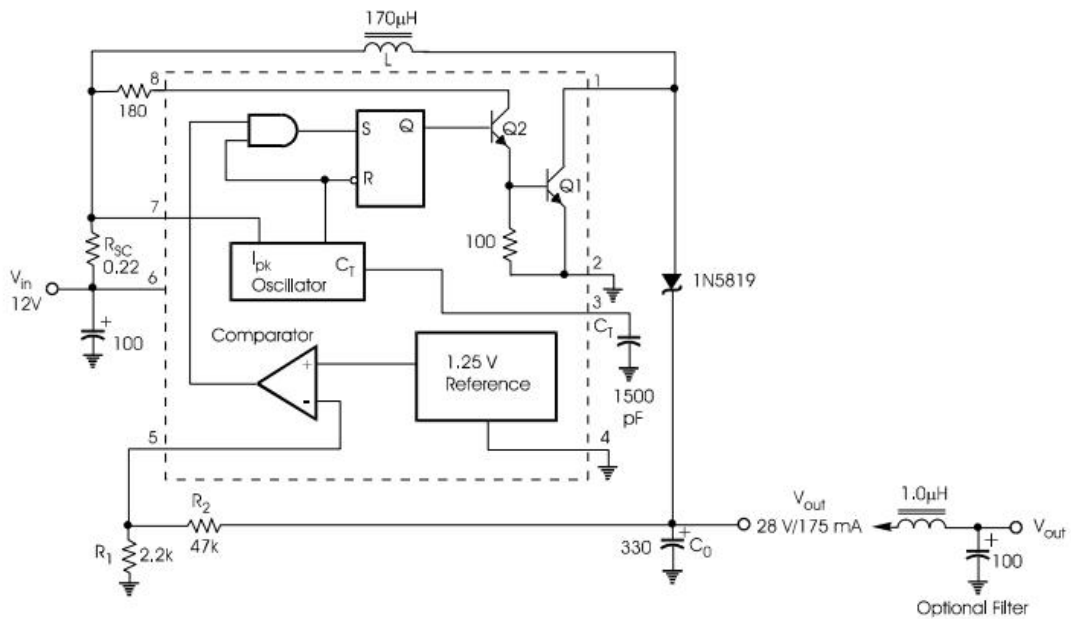
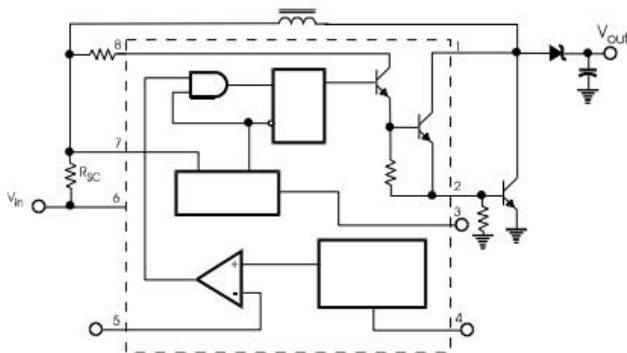
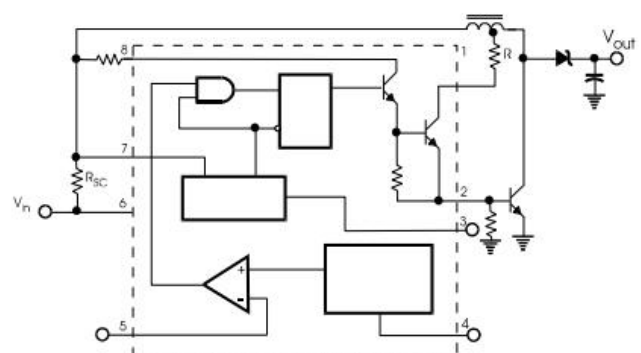
APPLICATION INFORMATION
Fig.1. Step-up converter

Fig.2. External current boost connections for IC Peak greater than 1.5A
2a. External NPN switch

2b. External NPN saturated switch


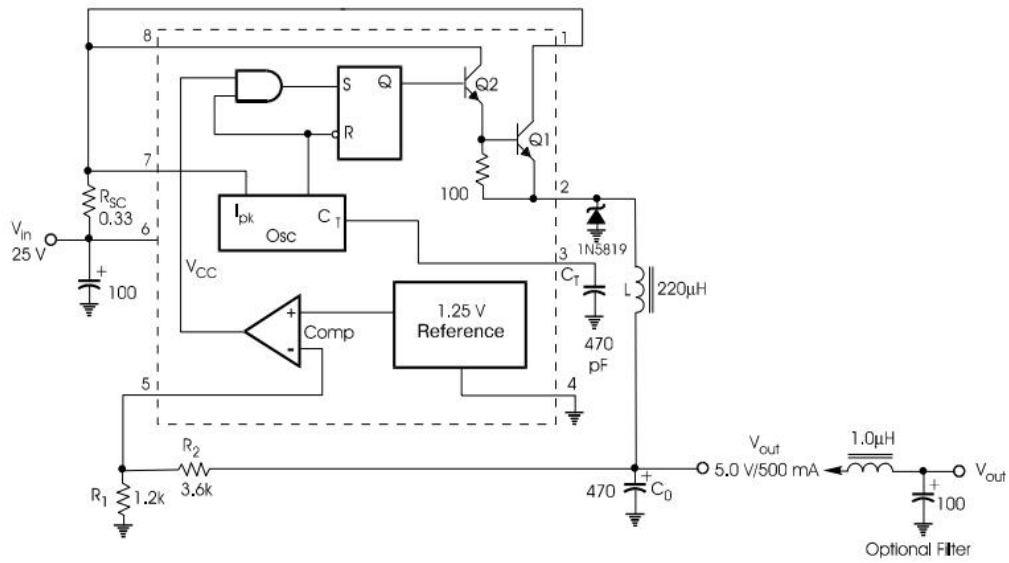
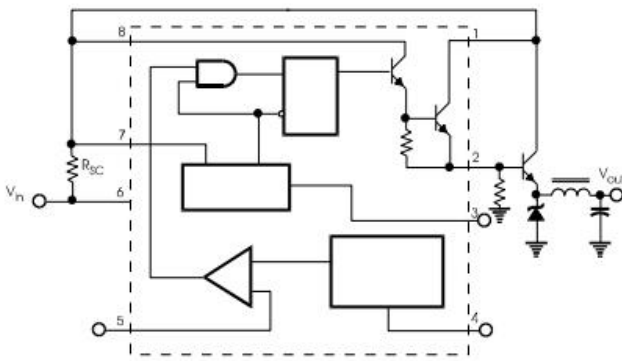
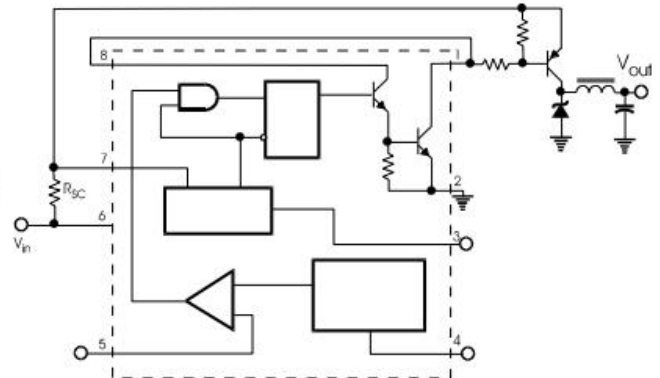
Fig.3. Step-down Converter

Fig.4. External current boost connections for $I_{C\ Peak}$ greater than 1.5A
4a. External NPN switch

4b. External PNP saturated switch


Fig.5. Voltage inverting converter

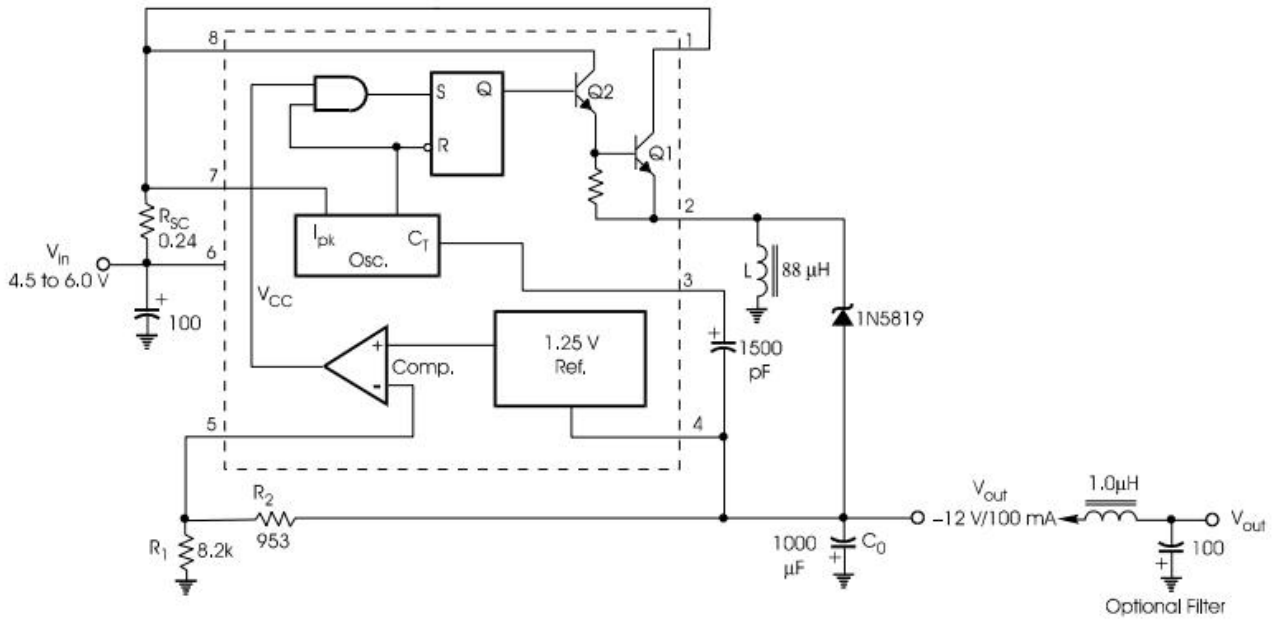
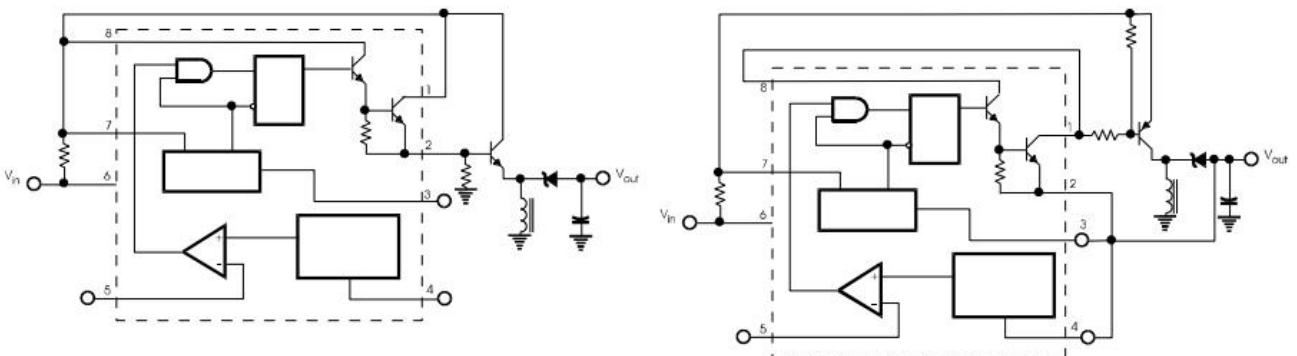


Fig.6. External current boost connections for Ic Peak greater than 1.5A

6a. External NPN switch

6b. External PNP saturated switch



DESIGN FORMULA

Calculation	Step-up	Step-down	Voltage-inverting
t_{on}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} + V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$
$L(min)$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) \times t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}} \right) \times t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}} \right) \times t_{on(max)}$
C_o	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

TERMS AND DEFINITIONS

V_{sat} – Saturation voltage of the output switch.

V_F – Forward voltage drop of the output rectifier.

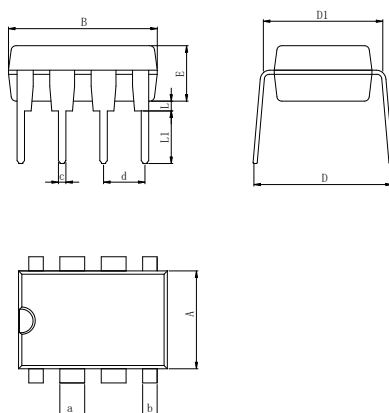
The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.

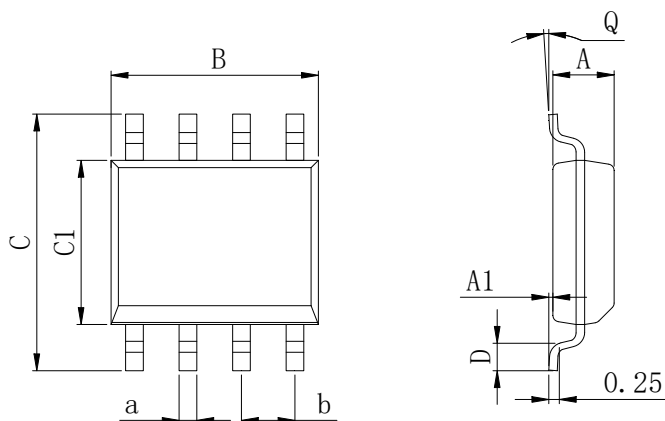
V_{out} – Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_{out} .

$V_{ripple(p-p)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

PHYSICAL DIMENSIONS
DIP-8


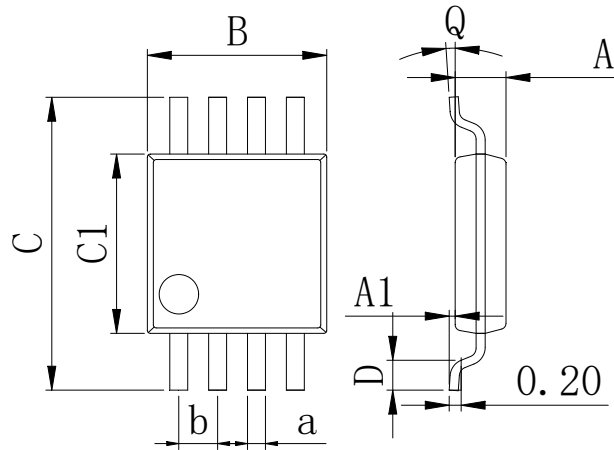
Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-8 (150mil)


Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

PHYSICAL DIMENSIONS

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

REVISION HISTORY

DATE	REVISION	PAGE
2014-6-9	New	1-12
2023-9-14	Update encapsulation type 、 Update Lead Temperature 、 Updated DIP-8 dimension、 Add annotation for Maximum Ratings.	1、 3、 9

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