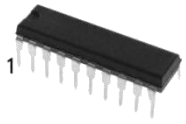
10-BIT ANALOG-TO-DIGITAL CONVERTERSWITH SERIAL CONTROL AND 11 ANALOG INPUTS

Features

- 10-Bit Resolution A/D Converter
- 11 Analog Input Channels
- Three Built-In Self-Test Modes
- Inherent Sample-and-Hold Function
- Total Unadjusted Error …±1 LSB Max
- On-Chip System Clock
- End-of-Conversion (EOC) Output
- Terminal Compatible With TLC542
- CMOS Technology



DIP-20

SOP-20W

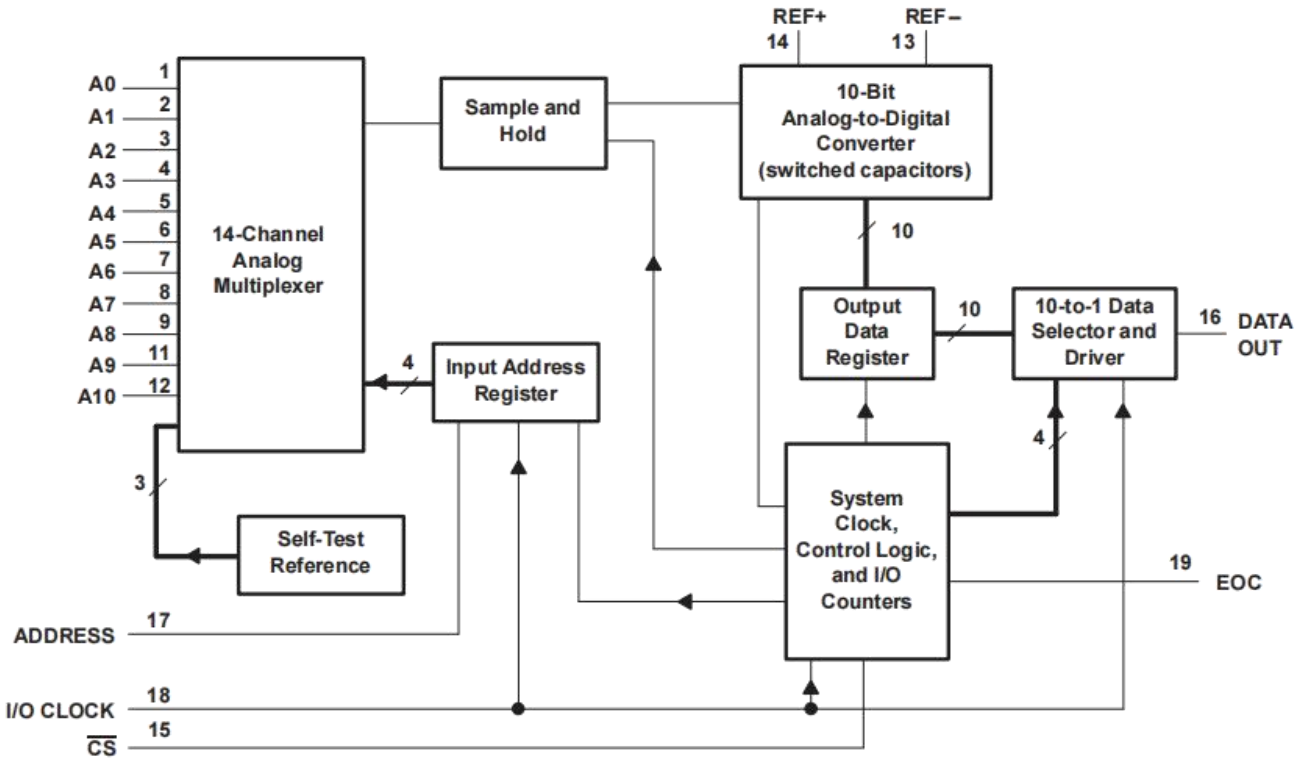
Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
TLC1543CPG	DIP-20	TLC1543C	TUBE	720pcs/box
TLC1543IPG	DIP-20	TLC1543I	TUBE	720pcs/box
TLC1543CDRG	SOP-20W	TLC1543C	REEL	2000pcs/reel
TLC1543IDRG	SOP-20W	TLC1543I	REEL	2000pcs/reel

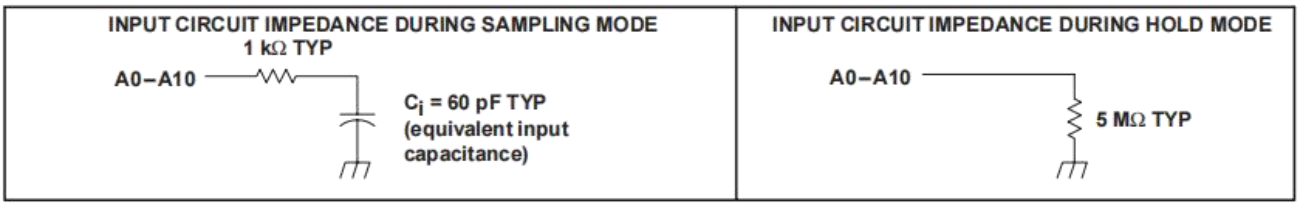
Description

The TLC1543C and TLC1543I are CMOS10 bit switched-capacitor successive-approximation analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. These devices allow high-speed data transfers from the host.
In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

functional block diagram

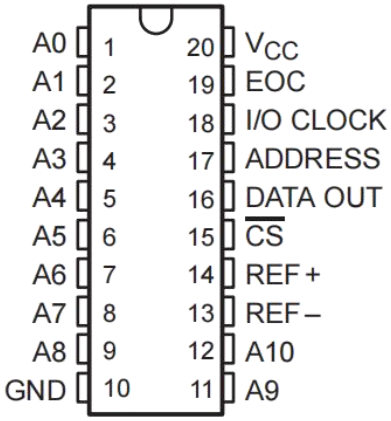


typical equivalent inputs



Pin Configuration

DIP-20/SOP-20W



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address input. A 4-bit serial address selects the desired analog input or test voltage that is tobe converted next. The address data is presented with the MSB first and shifts in on the first four risingedges of I/O CLOCK. After the four address bits have been read into the address register, this inputis ignored for the remainder of the current conversion period.
A0 – A10	1 – 9, 11, 12	I	Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed.The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enablesDATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges ofthe internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setuptime plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previousconversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits shift out in order with the LSB appearing on theninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unusedLSBs.
EOC	19	O	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/OCLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurementsare with respect to this terminal.
I/O CLOCK	18	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following fourfunctions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/OCLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex inputbegins charging the capacitor array and continues to do so until the tenth falling edge ofI/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenthclock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF – terminal.
REF–	13	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	20	I	Positive supply voltage

detailed description

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The serial interface then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first four I/O clocks load the address register with the 4-bit address on ADDRESS, selecting the desired analog channel, and the next six clocks providing the control timing for sampling the analog input.

detailed description (continued)

There are six basic serial-interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears at DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host-serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. Also, on the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero when the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. Mode Operation

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT DATA OUT(1)	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 to 16 (2)	$\overline{CS}$ falling edge	Figure 11
	Mode 4	Low continuously	16(2)	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16 (2)	$\overline{CS}$ falling edge	Figure 13
	Mode 6	Low continuously	16 (2)	16th clock falling edge	Figure 14

(1) These edges also initiate serial-interface communication.

(2) No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

mode 1: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 10-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

mode 3: fast mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers, and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host-serial interface and $\overline{CS}$ has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μs after the tenth I/O clock falling edge.

mode 5: slow mode, $\overline{CS}$ inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, $\overline{CS}$ active (low) continuously, 16-clock transfer

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or three internal test inputs).

analog inputs and test modes

The 11 analog inputs and the three internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

analog inputs and test modes (continued)

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED(1)	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)(2)
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

(1) Vref+ is the voltage applied to the REF+ input, and Vref– is the voltage applied to the REF– input.
(2) The output results shown are the ideal values and vary with the reference stability and with internal offsets.

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the SC switch and all ST switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all ST and SC switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half VCC), a 0 bit is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a 1 bit is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

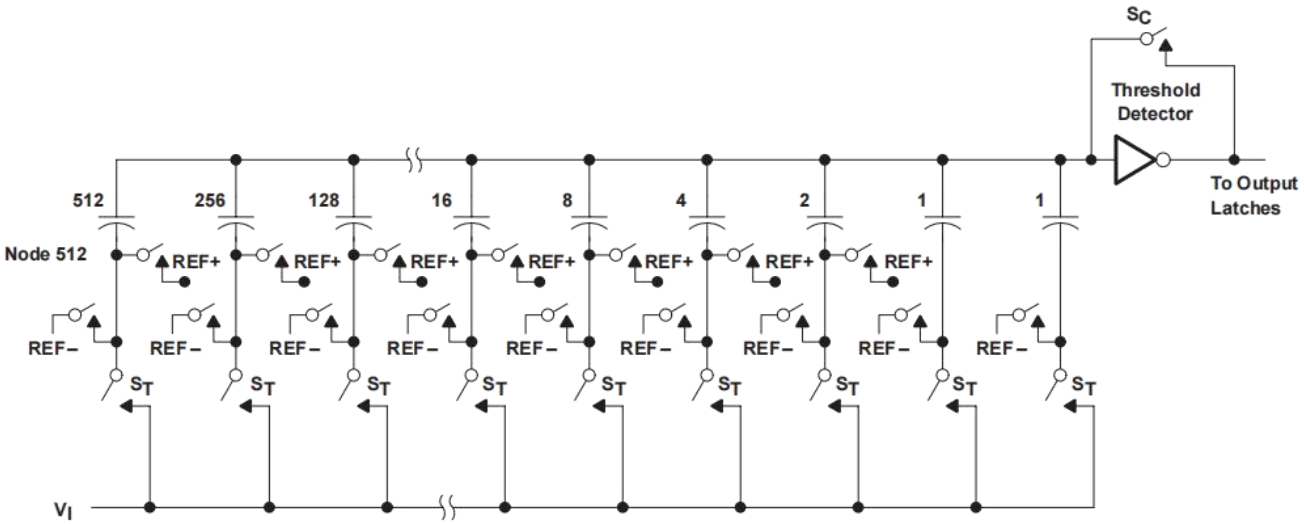


Figure 1. Simplified Model of the Successive-Approximation System chip-select operation

chip-select operation

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result).
Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with the device: REF+ and REF–. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, VCC (see Note 1)	-0.5 V to 6.5 V
Input voltage range, VI	-0.3V to VCC + 0.3 V
Output voltage range, VO	-0.3V to VCC + 0.3 V
Positive reference voltage, Vref+	VCC + 0.1 V
Negative reference voltage, Vref–	-0.1V
Peak input current (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, TA: TLC1543C	0℃ to 70℃
TLC1543I	-40℃ to 85℃
Storage temperature range, Tstg	-65℃ to 150℃
Lead Temperature (Soldering, 10 seconds)	245℃

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute - maximum rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF – and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Setup time, address bits at data input before I/O CLOCK ↑, $t_{su(A)}$ (see Figure 4)		100			ns
Hold time, address bits after I/O CLOCK ↑, $t_{h(A)}$ (see Figure 4)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK ↑, $t_{h(CS)}$ (see Figure 5)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 5)		1.425			μs
Clock frequency at I/O CLOCK (see Note 4)		0		2.1	MHz
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		190			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		190			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 5 and Figure 6)				1	μs
Transition time, ADDRESS and CS, $t_{t(CS)}$				10	μs
Operating free-air temperature, T_A	TLC1543C	0		70	℃
	TLC1543I	–40		85	

1. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (Vref + – Vref –); however, the electrical specifications are no longer applicable.
2. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within9.5μs.
4. This is the time required for the clock input signal to fall from VIHmin to VILmax or to rise from VILmax to VIHmin. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, VCC = Vref+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 μA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 μA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
Selected channel leakage current C, I, or Q			Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V,	Unselected channel at V_{CC}			–1	
Maximum static analog reference current into REF +			Vref + = VCC,	Vref – = GND			10	μA
C_i	Input capacitance	Analog inputs				7		pF
		Control inputs				5		

† All typical values are at VCC = 5 V, TA = 25℃.

operating characteristics over recommended operating free-air temperature range, VCC = Vref+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 6)				±1	LSB
E_{ZS}	Zero-scale error (see Note 7)	See Note 2			±1	LSB
E_{FS}	Full-scale error (see Note 7)	See Note 2			±1	LSB
Total unadjusted error (see Note 8)					±1	±1
Self-test output code (see Table 3 and Note 9)		ADDRESS = 1011	512			
		ADDRESS = 1100	0			
		ADDRESS = 1101	1023			
t_{conv}	Conversion time	See timing diagrams			21	µs
t_c	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 10			21+10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)	See timing diagrams and Note 10			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, tenth I/O CLOCK↑ to EOC↓	See Figure 7	70		240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑to DATA OUT (MSB)	See Figure 8			100	ns

† All typical values are at TA = 25℃.

NOTES:

1. Analog input voltages greater than that applied to REF + convert as all ones (1111111111), while input voltages less than that applied to REF – convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (Vref + – Vref –); however, the electrical specifications are no longer applicable.
2. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
3. Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
4. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
5. Both the input address and the output codes are expressed in positive logic.
6. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6)

operating characteristics over recommended operating free-air temperature range, VCC = Vref+ = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted) (continued)

		TEST CONDITIONS	MIN TYP† MAX	UNIT
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)	See Figure 3	1.3	μs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8	300	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7	300	ns
$t_{r(DATA)}$	Rise time, data bus	See Figure 6	300	ns
$t_{f(DATA)}$	Fall time, data bus	See Figure 6	300	ns
$t_{d(I/O-CS)}$	Delay time, tenth I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion(see Note 11)		9	μs

† All typical values are at TA = 25℃.

NOTE 11. Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock(1.425 μs) after the transition.

Parameter Measurement Information

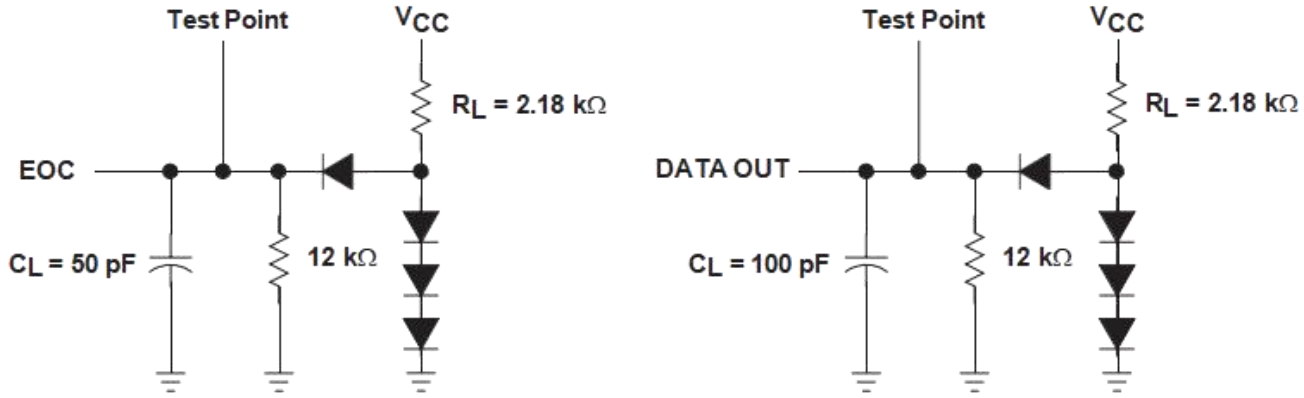


Figure 2. Load Circuits

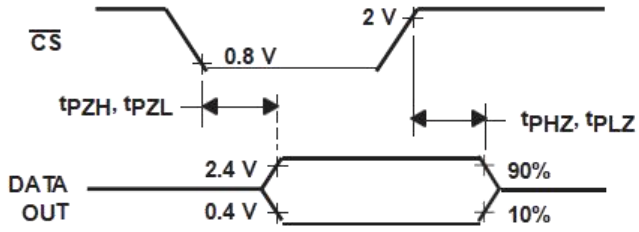


Figure 3. DATA OUT Enable and Disable Voltage Waveforms

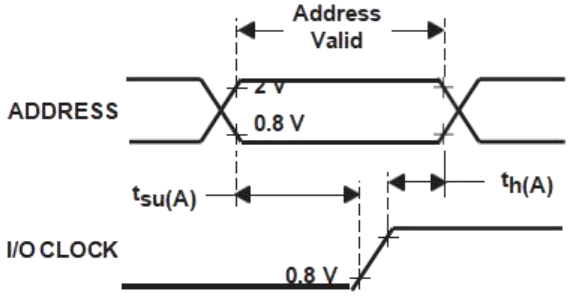


Figure 4. ADDRESS Setup and Hold TIme Voltage Waveforms

Parameter Measurement Information

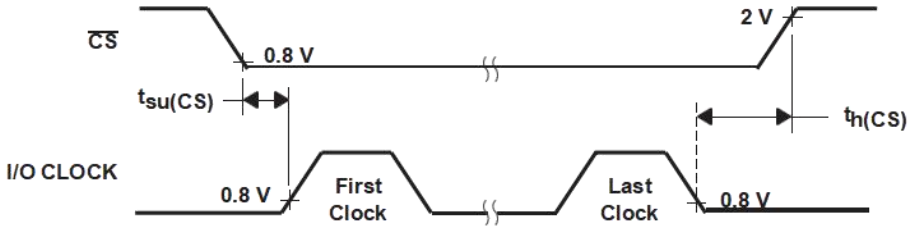


Figure 5. I/O CLOCK Setup and Hold Time Voltage Waveforms

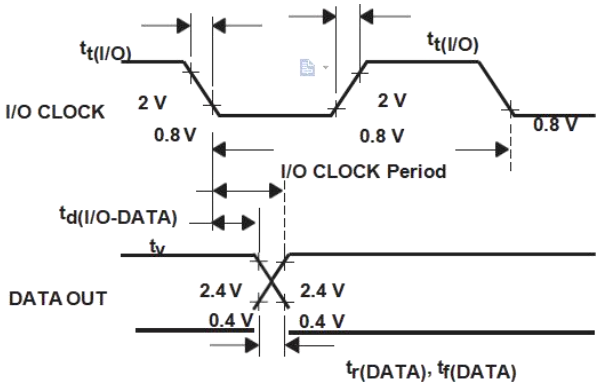


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

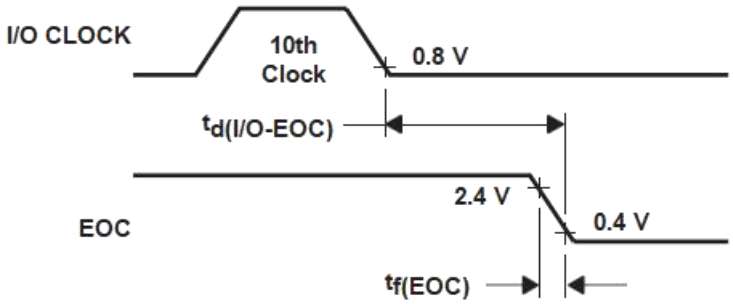


Figure 7. I/O CLOCK and EOC Voltage Waveforms

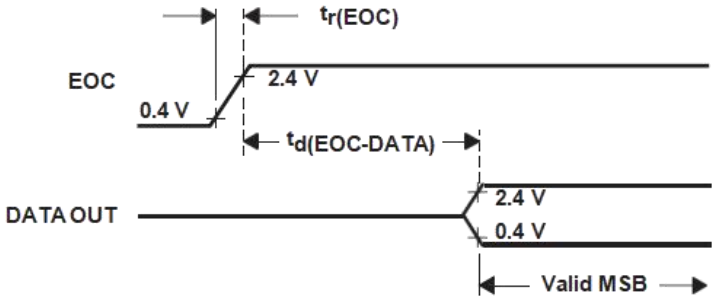
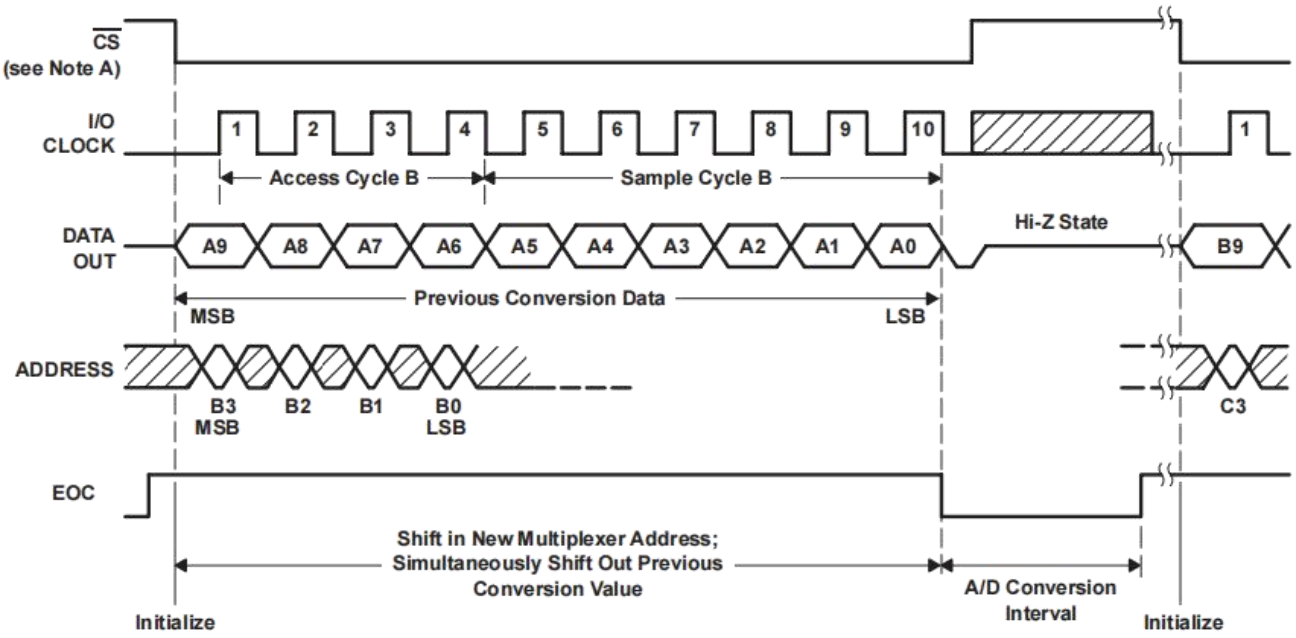


Figure 8. EOC and DATA OUT Voltage Waveforms

Parameter Measurement Information

timing diagrams

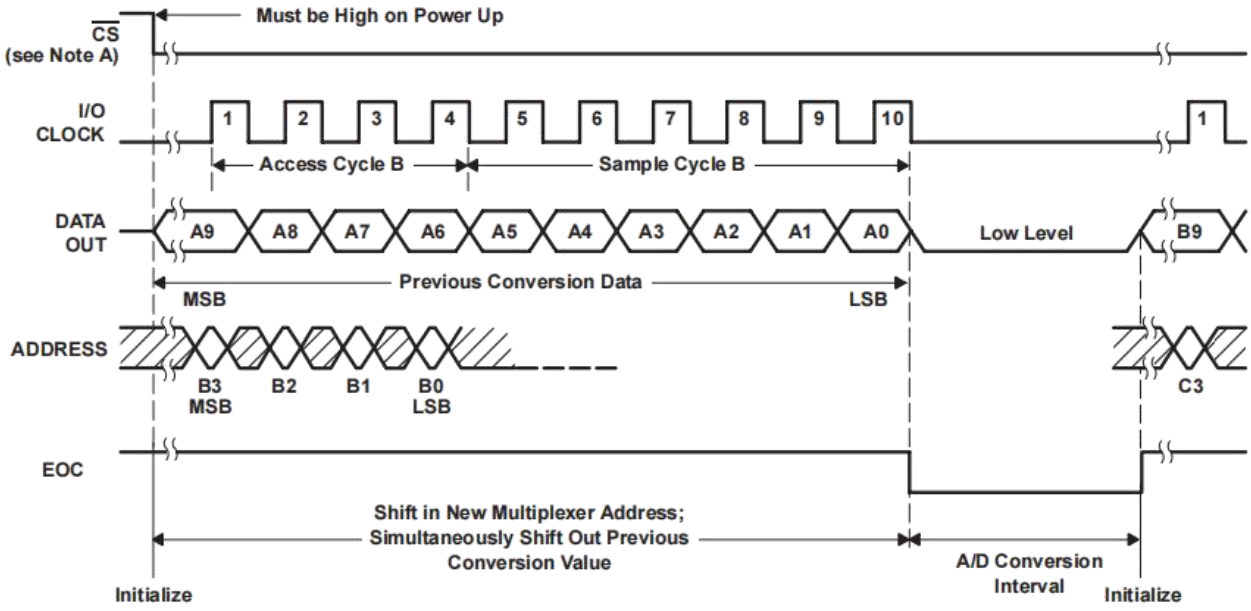


NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$

Parameter Measurement Information

timing diagrams (continued)

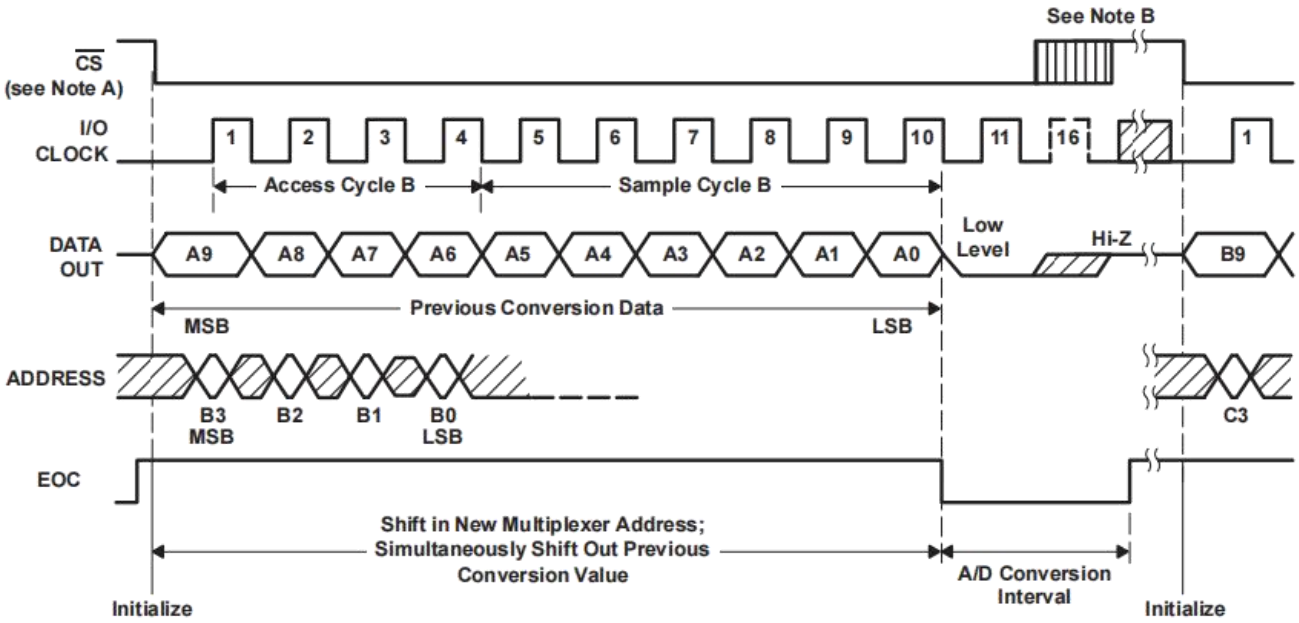


NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

Parameter Measurement Information

timing diagrams (continued)



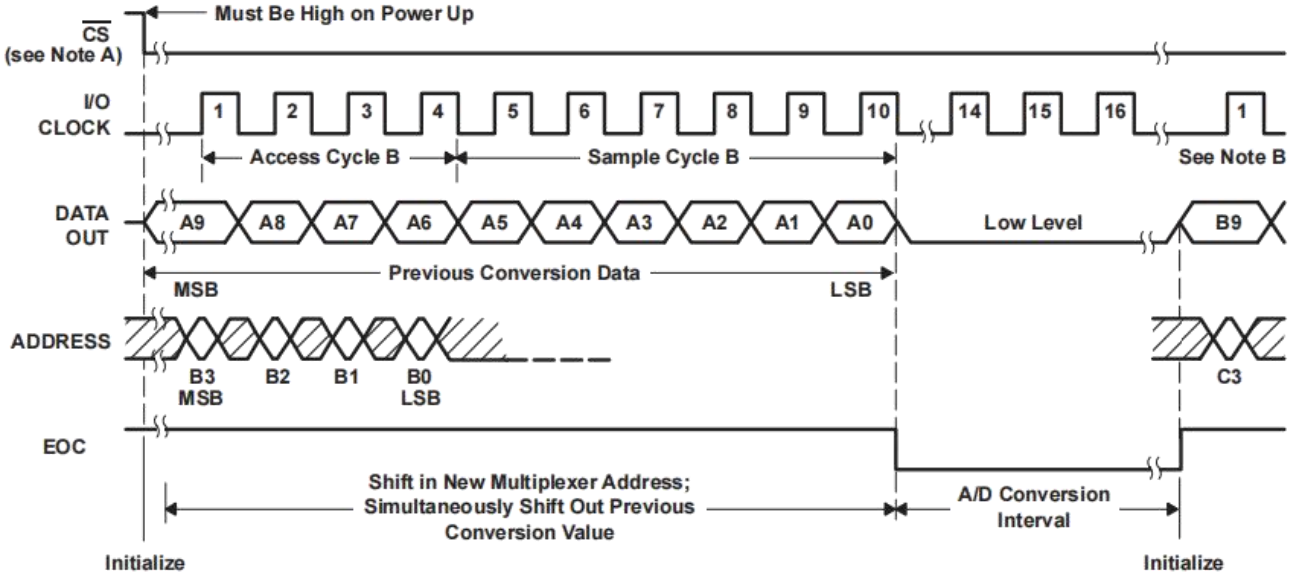
A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. B. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

Parameter Measurement Information

timing diagrams (continued)



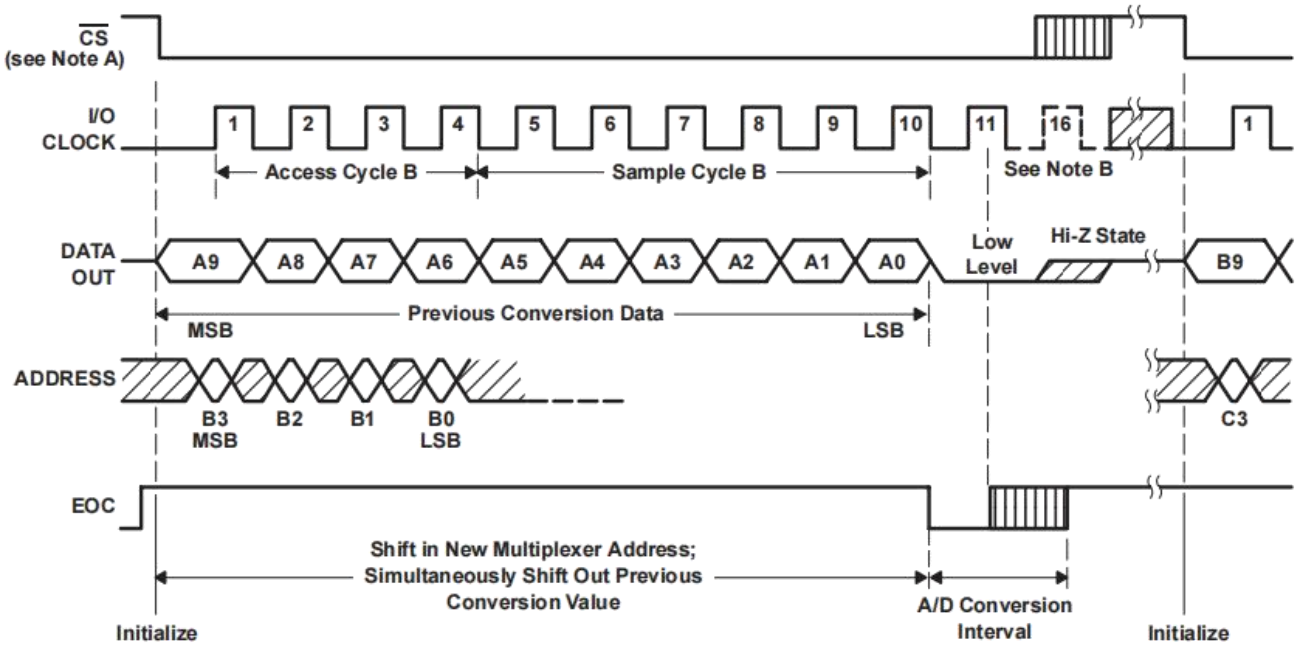
A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The first I/O CLOCK must occur after the rising edge of EOC.

Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

Parameter Measurement Information

timing diagrams (continued)



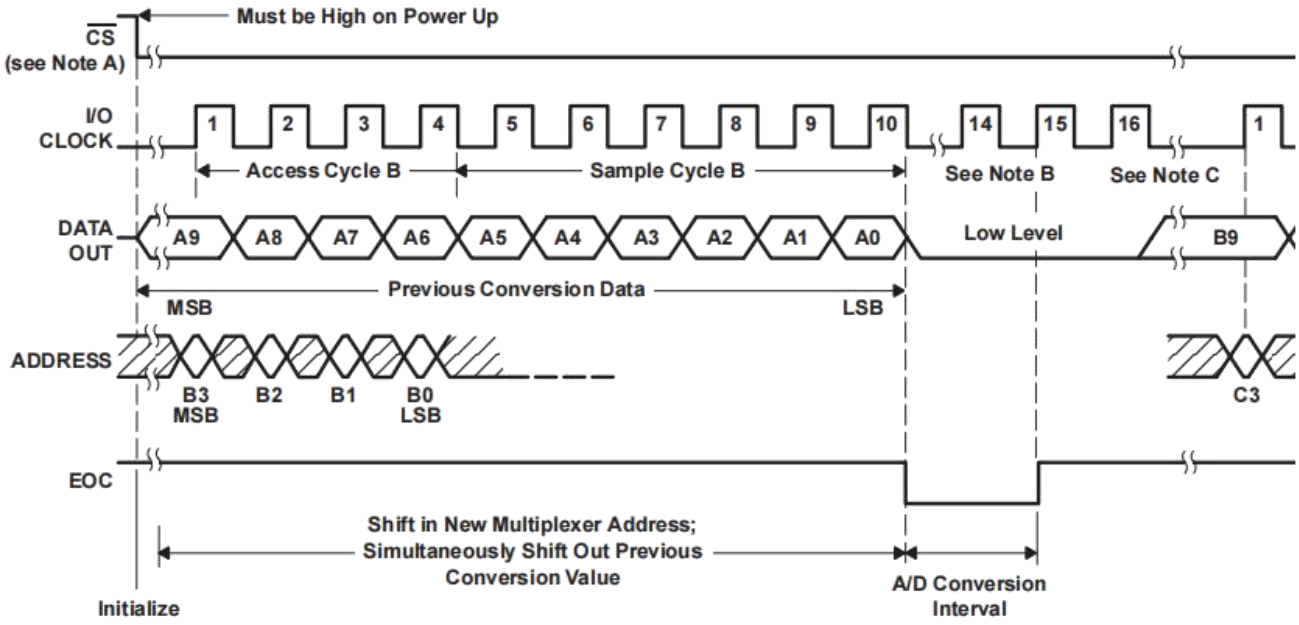
A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

Parameter Measurement Information

timing diagrams (continued)



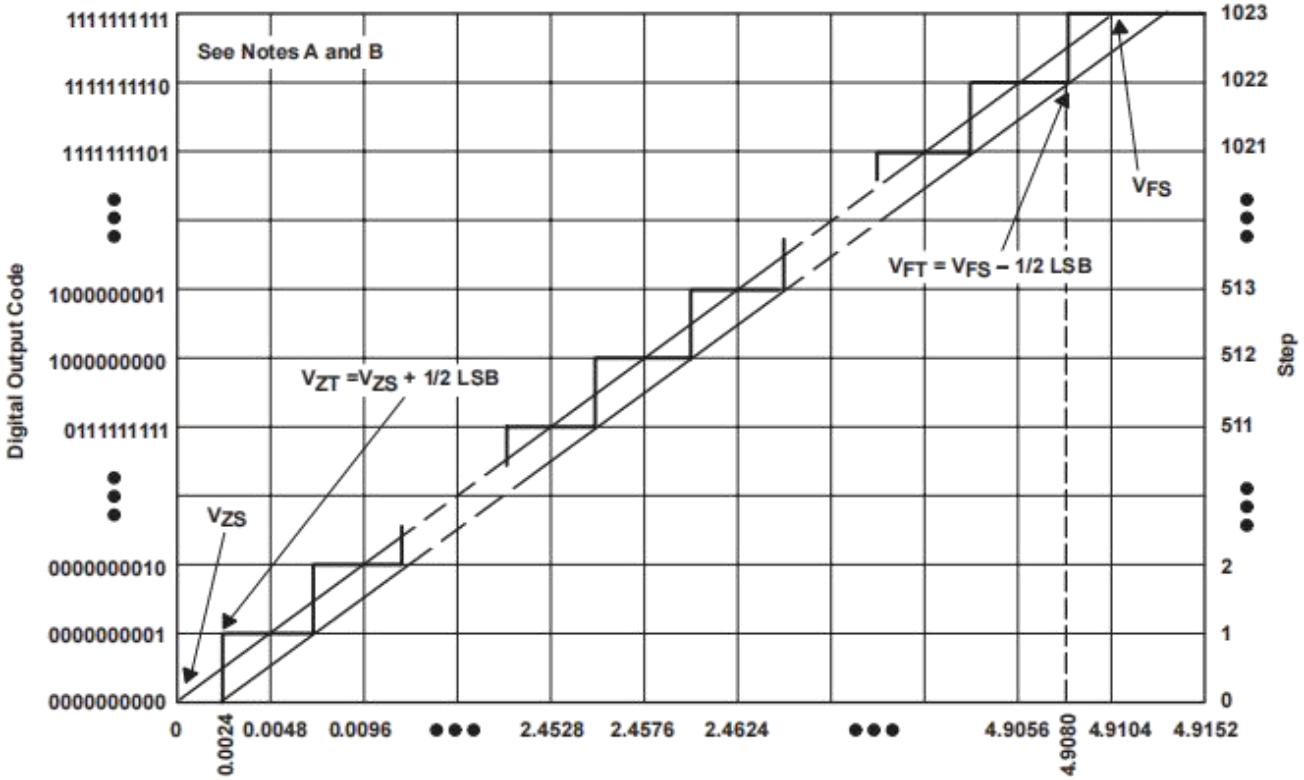
A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

Application Information



VI – Analog Input Voltage – V

A. This curve is based on the assumption that Vref+ and Vref– have been adjusted so that the voltage at the transition from digital 0 to 1 (VZT) is 0.0024 V and the transition to full scale (VFT) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (VFS) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (VZS) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

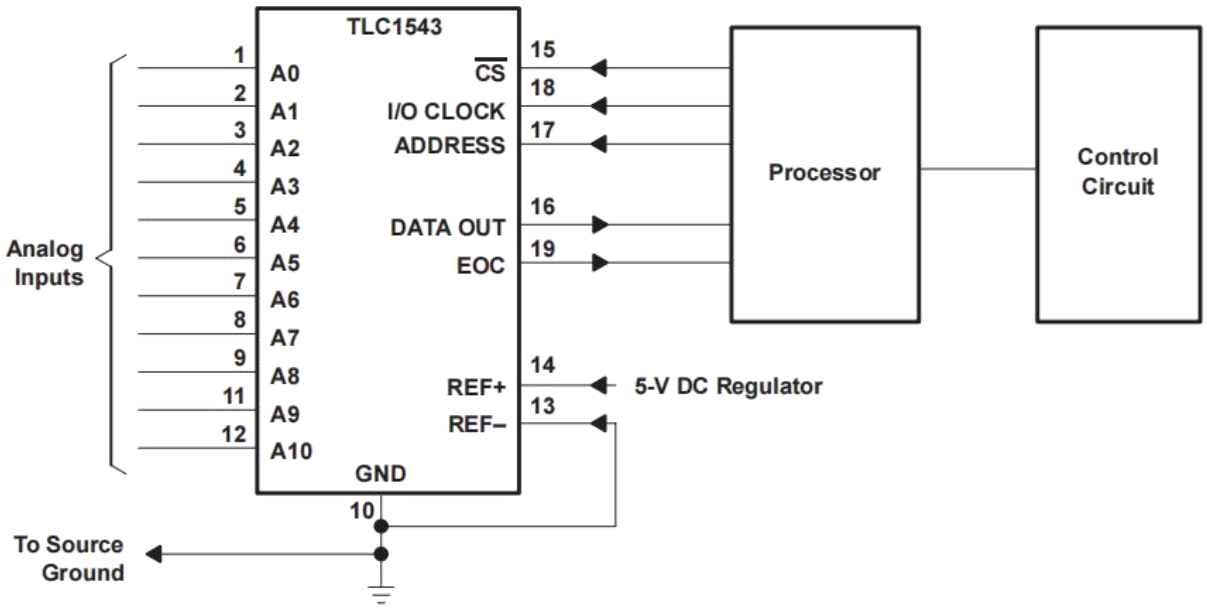


Figure 16. Serial Interface

Application Information

simplified analog input analysis

Using the equivalent circuit in Figure 17, the time required to charge the analog input capacitance from 0 to VS within 1/2 LSB can be derived as follows:
The capacitance charging voltage is given by

$$V_C = V_S(1 - e{-}t_c/R_tC_j) \quad (1)$$

where

$$R_t = R_s + r_i \quad (2)$$

The final voltage to 1/2 LSB is given by

$$V_C(1/2\ \text{LSB} = V_S - (V_S/2048)$$

Equating equation 1 to equation 2 and solving for ti

$$V_S - (V_S/2048) = V_S(1 - e{-}t_c/R_tC_j) \quad (3)$$

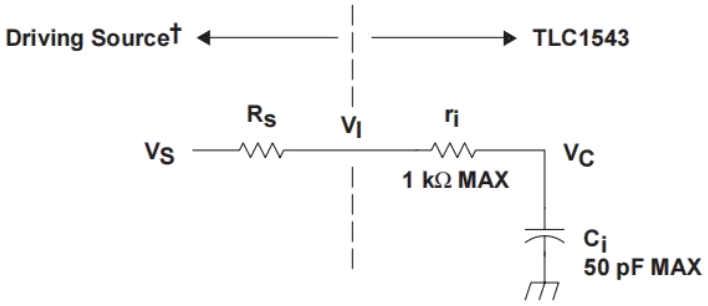
and

$$t_c(1/2\ \text{LSB}) = R_t \times C_j \times \text{in}(2048) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c(1/2\ \text{LSB}) = (R_s + 1\text{k}\Omega) \times 60\text{pF} \times \text{in}(2048) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



VI = Input Voltage at A0–A10
VS= External Driving Source Voltage
Rs = Source Resistance
ri = Input Resistance
Ci = Equivalent Input Capacitance

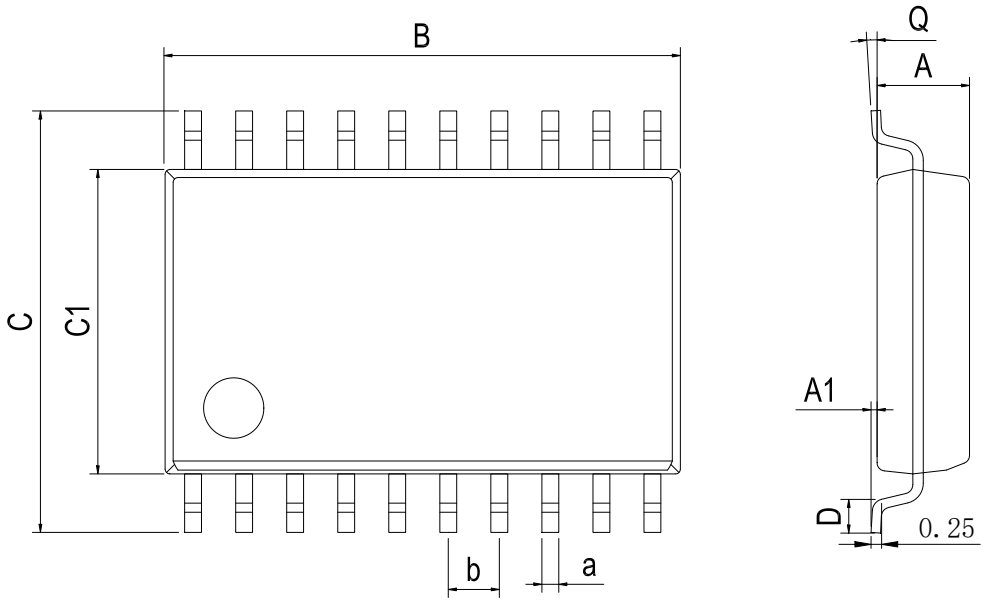
Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- Rs must be real at the input frequency.

Figure 17. Equivalent Input Circuit Including the Driving Source

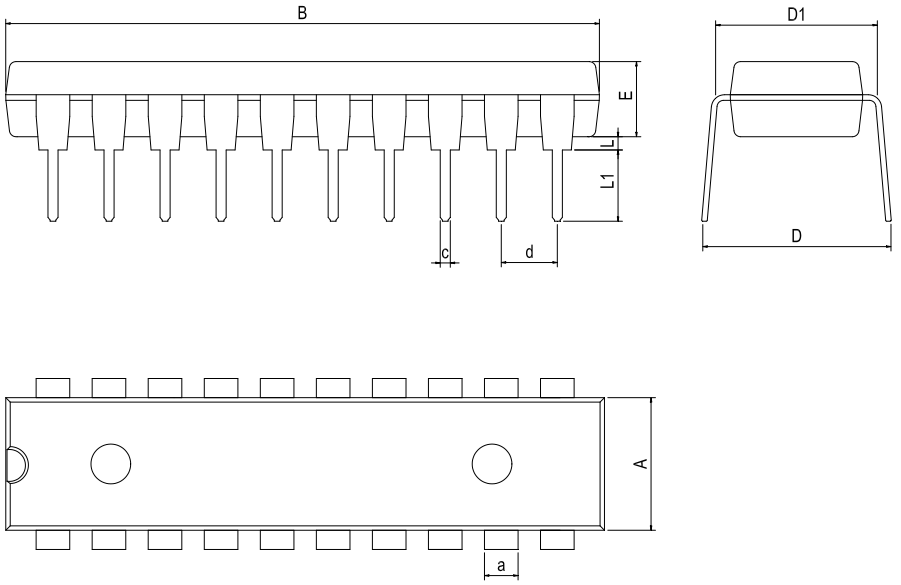
Physical Dimensions

SOP-20W



Dimensions In Millimeters(SOP-20W)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.05	12.50	10.21	7.40	0.45	0°	0.35	1.27 BSC
Max:	2.50	0.25	13.00	10.61	7.60	1.25	8°	0.45	

DIP-20



Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	24.95	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	26.55	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

Revision History

DATE	REVISION	PAGE
2017-8-5	New	1-23
2023-8-26	Update encapsulation type、Update Lead Temperature、Updated DIP-20 dimension	1、8、21
2024-2-22	Update packages model SOP-20W	1

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