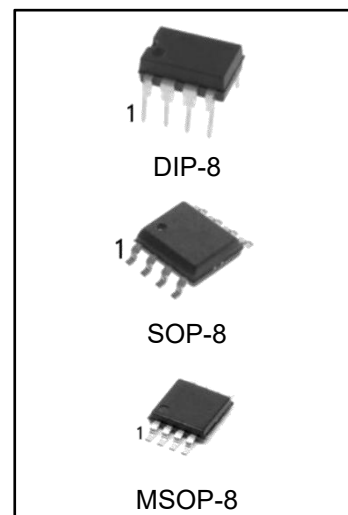


## TLC5615 10-BIT DIGITAL-TO-ANALOG CONVERTERS

### Features

- 10-Bit CMOS Voltage Output DAC in an 8-Terminal Package
- 5V Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range: 2 Times the Reference Input Voltage
- Internal Power-On Reset
- Low Power Consumption: 1.75mW(Max)
- Update Rate of 1.21 MHz
- Settling Time to 0.5 LSB: 12.5  $\mu$ s(Typ)
- Monotonic Over Temperature
- Pin Compatible With the Maxim MAX515



### Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
TLC5615IN	DIP-8	C5615I	TUBE	2000pcs/box
TLC5615CN	DIP-8	C5615C	TUBE	2000pcs/box
TLC5615IM/TR	SOP-8	C5615I	REEL	2500pcs/reel
TLC5615CM/TR	SOP-8	C5615C	REEL	2500pcs/reel
TLC5615IMM/TR	MSOP-8	C5615I	REEL	3000pcs/reel
TLC5615CMM/TR	MSOP-8	C5615C	REEL	3000pcs/reel

## Description

The TLC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5 V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

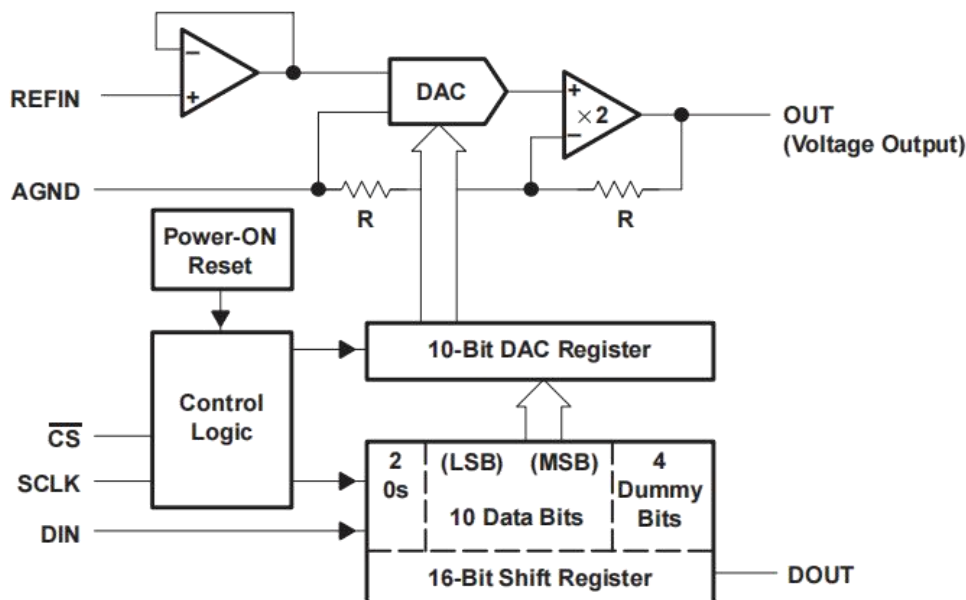
Digital control of the TLC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and micro controller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5615C is characterized for operation from 0°C to 70°C. The TLC5615I is characterized for operation from -40°C to 85°C.

## Applications

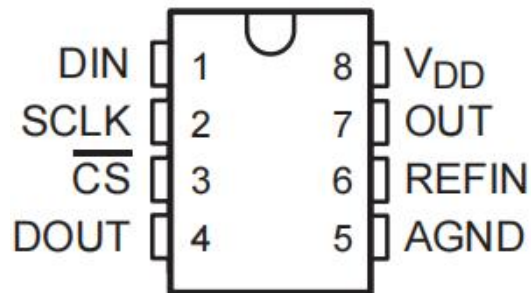
- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

## Functional block diagram



## Pin Configuration

DIP-8/SOP-8/MSOP-8



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
VDD	8		Positive power supply

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Condition		Min	Max
Supply voltage (VDD to AGND)		-	7 V
Digital input voltage range to AGND		-0.3 V	VDD + 0.3 V
Reference input voltage range to AGND		-0.3 V	VDD + 0.3 V
Output voltage at OUT from external source		-	VDD + 0.3 V
Continuous current at any terminal		-20mA	+20mA
Operating free-air temperature range, T <sub>A</sub> :	TLC5615C	0°C	70°C
	TLC5615I	-40°C	85°C
Storage temperature range, T <sub>stg</sub>		-65°C	150°C
Lead Temperature (Soldering, 10 seconds)		-	245°C

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

**Recommended Operating Conditions**

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4.5	5	5.5	V
High-level digital input voltage, V <sub>IH</sub>		2.4			V
Low-level digital input voltage, V <sub>IL</sub>				0.8	V
Reference voltage, V <sub>ref</sub> to REFIN terminal		2	2.048	VDD-2	V
Load resistance, R <sub>L</sub>		2			kΩ
Operating free-air temperature, T <sub>A</sub>	TLC5615C	0		70	°C
	TLC5615I	-40		85	°C

**Electrical Characteristics**

over recommended operating free-air temperature range, V<sub>DD</sub> = 5 V ±5%, V<sub>ref</sub> = 2.048 V (unless otherwise noted) static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			bits
Integral nonlinearity, end point adjusted (INL)		V <sub>ref</sub> = 2.048 V, See Note 1			±1	LSB
Differential nonlinearity (DNL)		V <sub>ref</sub> = 2.048 V, See Note 2		±0.1	±0.5	LSB
E <sub>ZS</sub>	Zero-scale error (offset error at zero scale)	V <sub>ref</sub> = 2.048 V, See Note 3			±3	LSB
Zero-scale-error temperature coefficient		V <sub>ref</sub> = 2.048 V, See Note 4		3		ppm/°C
E <sub>G</sub>	Gain error	V <sub>ref</sub> = 2.048 V, See Note 5			±3	LSB
Gain-error temperature coefficient		V <sub>ref</sub> = 2.048 V, See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio	See Notes 7 and 8	80	80		dB
	Zero scale					
	Gain					
Analog full scale output		R <sub>L</sub> = 100 kΩ	2V <sub>ref</sub> (1023/1024)			V

1. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
2. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).
4. Zero-scale-error temperature coefficient is given by:  

$$EZS\ TC = [EZS(T_{max}) - EZS(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$$
5. Gain error is the deviation from the ideal output ( $V_{ref} - 1\text{ LSB}$ ) with an output load of  $10\text{ k}\Omega$  excluding the effects of the zero-scale error.
6. Gain temperature coefficient is given by:  $EG\ TC = [EG(T_{max}) - EG(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$ .
7. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the  $V_{DD}$  from  $4.5\text{ V}$  to  $5.5\text{ V}$  dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain-error rejection ratio (EG-RR) is measured by varying the  $V_{DD}$  from  $4.5\text{ V}$  to  $5.5\text{ V}$  dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

## Voltage Output (Out)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$	Voltage output range	$R_L = 10\text{ k}\Omega$	0		$V_{DD}-0.4$	V
	Output load regulation accuracy	$V_O(\text{OUT}) = 2\text{ V}, R_L = 2\text{ k}\Omega$			0.5	LSB
$I_{OSC}$	Output short circuit current	OUT to $V_{DD}$ or AGND		20		mA
$V_{OL}(\text{low})$	Output voltage, low-level	$I_O(\text{OUT}) \leq 5\text{ mA}$			0.25	V
$V_{OH}(\text{high})$	Output voltage, high-level	$I_O(\text{OUT}) \leq -5\text{ mA}$	4.75			V

## Electrical Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 5\text{ V} \pm 5\%$ ,  $V_{ref} = 2.048\text{ V}$  (unless otherwise noted) (continued) reference input (REFIN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_I$	Input voltage		0		$V_{DD}-2$	V
$r_i$	Input resistance		10			$M\Omega$
$C_i$	Input capacitance		5			pF

## digital inputs (DIN, SCLK, CS)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level digital input voltage		2.4			V
$V_{IL}$	Low-level digital input voltage				0.8	V
$I_{IH}$	High-level digital input current	$V_I = V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	Low-level digital input current	$V_I = 0$			$\pm 1$	$\mu\text{A}$
$C_i$	Input capacitance		8			pF

## digital output (DOUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	Output voltage, high-level	$I_O = -2\text{ mA}$	$V_{DD}-1$			V
$V_{OL}$	Output voltage, low-level	$I_O = 2\text{ mA}$			0.4	V

**power supply**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>DD</sub> Supply voltage			4.5	5	5.5	V
I <sub>DD</sub> Power supply current	V <sub>DD</sub> = 5.5 V, No load, All inputs = 0 V or V <sub>DD</sub>	V <sub>ref</sub> = 0		150	250	μA
	V <sub>DD</sub> = 5.5 V, No load, All inputs = 0 V or V <sub>DD</sub>	V <sub>ref</sub> = 2.048 V		230	350	μA

**analog output dynamic performance**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, S/(N+D)	V <sub>ref</sub> = 1 V <sub>pp</sub> at 1 kHz + 2.048 V <sub>dc</sub> , code = 11 1111 1111, See Note 9	60			dB

NOTE 9: The limiting frequency value at 1 V<sub>pp</sub> is determined by the output-amplifier slew rate.

**digital input timing requirements (see Figure 1)**

PARAMETER	MIN	TYP	MAX	UNIT
t <sub>su</sub> (DS) Setup time, DIN before SCLK high	45			ns
t <sub>h</sub> (DH) Hold time, DIN valid after SCLK high	0			ns
t <sub>su</sub> (CSS) Setup time, $\overline{CS}$ low to SCLK high	1			ns
t <sub>su</sub> (CS1) Setup time, $\overline{CS}$ high to SCLK high	50			ns
t <sub>h</sub> (CSH0) Hold time, SCLK low to $\overline{CS}$ low	1			ns
t <sub>h</sub> (CSH1) Hold time, SCLK low to $\overline{CS}$ high	0			ns
t <sub>w</sub> (CS) Pulse duration, minimum chip select pulse width high	20			ns
t <sub>w</sub> (CL) Pulse duration, SCLK low	25			ns
t <sub>w</sub> (CH) Pulse duration, SCLK high	25			ns

**output switching characteristic**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>pd</sub> (DOUT) Propagation delay time, DOUT	C <sub>L</sub> = 50 pF			50	ns

## Operating Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 5\text{ V} \pm 5\%$ ,  $V_{ref} = 2.048\text{ V}$  (unless otherwise noted) analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Output slew rate	$C_L = 100\text{ pF}, T_A = 25^\circ\text{C}$ $R_L = 10\text{ k}\Omega$	0.3	0.5		V/ $\mu\text{s}$
$t_s$ Output settling time	To 0.5 LSB, $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Note 10		12.5		$\mu\text{s}$
Glitch energy	DIN = All 0s to all 1s		5		Nv · s

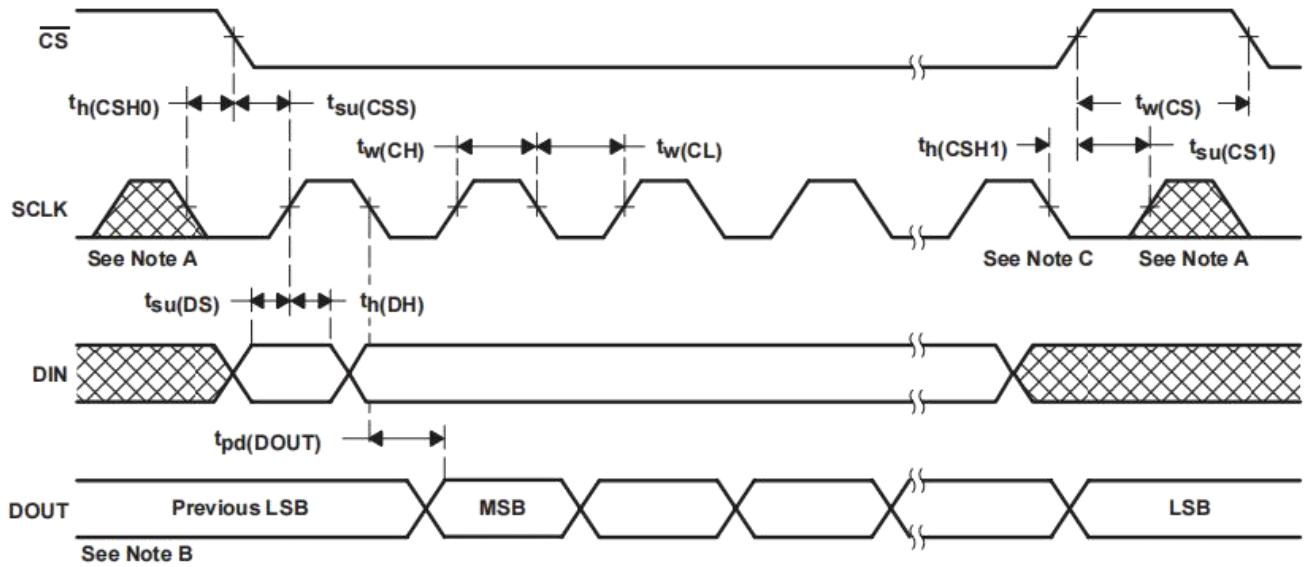
NOTE 10: Settling time is the time for the output signal to remain within  $\pm 0.5$  LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

## reference input (REFIN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference feedthrough	REFIN = 1 V <sub>pp</sub> at 1 kHz + 2.048 Vdc (see Note 11)		-80		dB
Reference input bandwidth (f-3dB)	REFIN = 0.2 V <sub>pp</sub> + 2.048 Vdc REFIN = 0.2 V <sub>pp</sub> + 2.048 Vdc		30		kHz

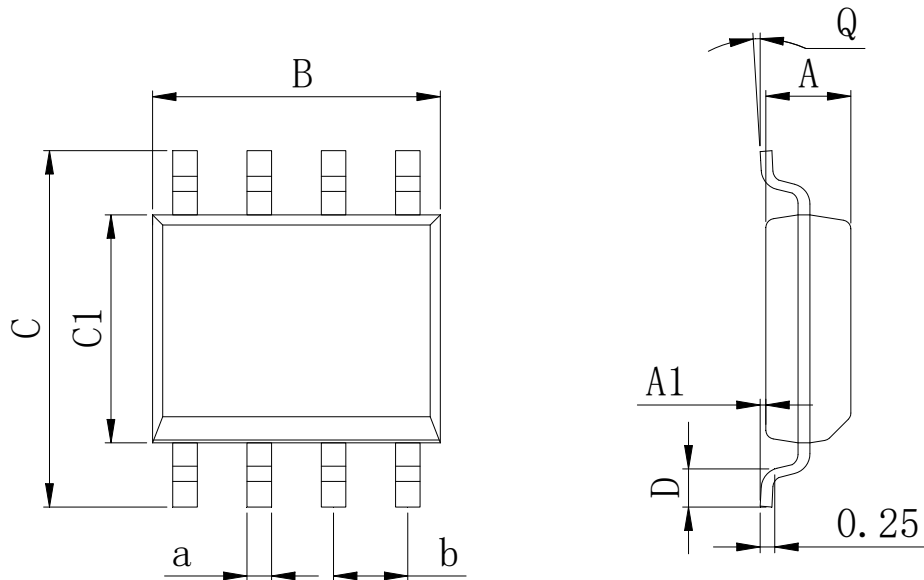
NOTE 11: Reference feed through is measured at the DAC output with an input code = 000 hex and a Vref input = 2.048 Vdc + 1 Vpp at 1 kHz.

**Parameter Measurement Information**

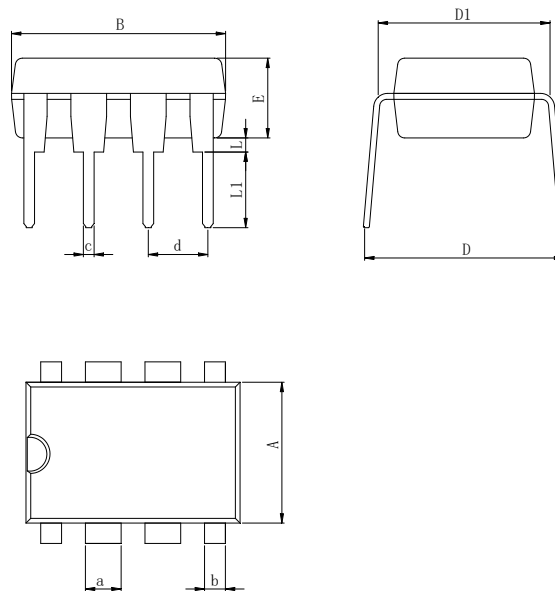


- A. The input clock, applied at the SCLK terminal, should be inhibited low when CS is high to minimize clock feedthrough.
- B. Data input from preceding conversion cycle.
- C. Sixteenth SCLK falling edge



**Physical Dimensions**
**SOP-8**

**Dimensions In Millimeters(SOP-8)**

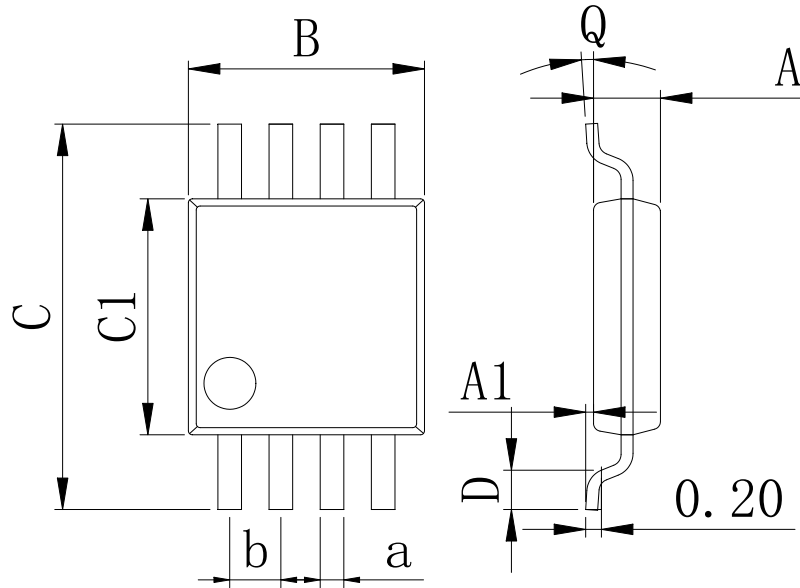
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

**DIP-8**

**Dimensions In Millimeters(DIP-8)**

Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

**Physical Dimensions**

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

## Revision History

DATE	REVISION	PAGE
2015-8-9	New	1-12
2023-8-26	Update encapsulation type 、 Update Lead Temperature 、 Updated DIP-8 dimension	1、 4、 9

**IMPORTANT STATEMENT:**

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety, security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.

单击下面可查看定价，库存，交付和生命周期等信息

[>>HGSEMI\(华冠\)](#)