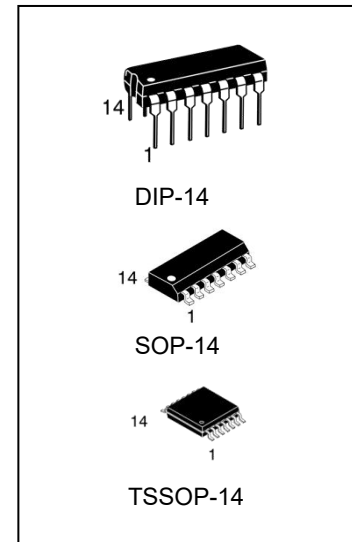


## Precision Waveform Generator/Voltage Controlled Oscillator

### Features

- Low Frequency Drift with Temperature: 250ppm/°C
- Low Distortion: 1% (Sine Wave Output)
- High Linearity: 0.1% (Triangle Wave Output)
- Wide Frequency Range: 0.001Hz to 300kHz
- Variable Duty Cycle: 2% to 98%
- High Level Outputs: TTL to 28V
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Easy to Use - Just a Handful of External Components Required



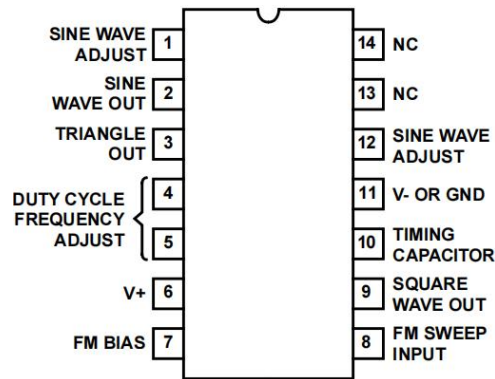
### Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
ICL8038N	DIP-14	ICL8038	TUBE	1000pcs/Box
ICL8038BN	DIP-14	ICL8038B	TUBE	1000pcs/Box
ICL8038AN	DIP-14	ICL8038A	TUBE	1000pcs/Box
ICL8038M/TR	SOP-14	ICL8038	REEL	2500pcs/reel
ICL8038BM/TR	SOP-14	ICL8038B	REEL	2500pcs/reel
ICL8038AM/TR	SOP-14	ICL8038A	REEL	2500pcs/reel
ICL8038MT/TR	TSSOP-14	ICL8038	REEL	2500pcs/reel
ICL8038BMT/TR	TSSOP-14	ICL8038B	REEL	2500pcs/reel
ICL8038AMT/TR	TSSOP-14	ICL8038A	REEL	2500pcs/reel

### Description

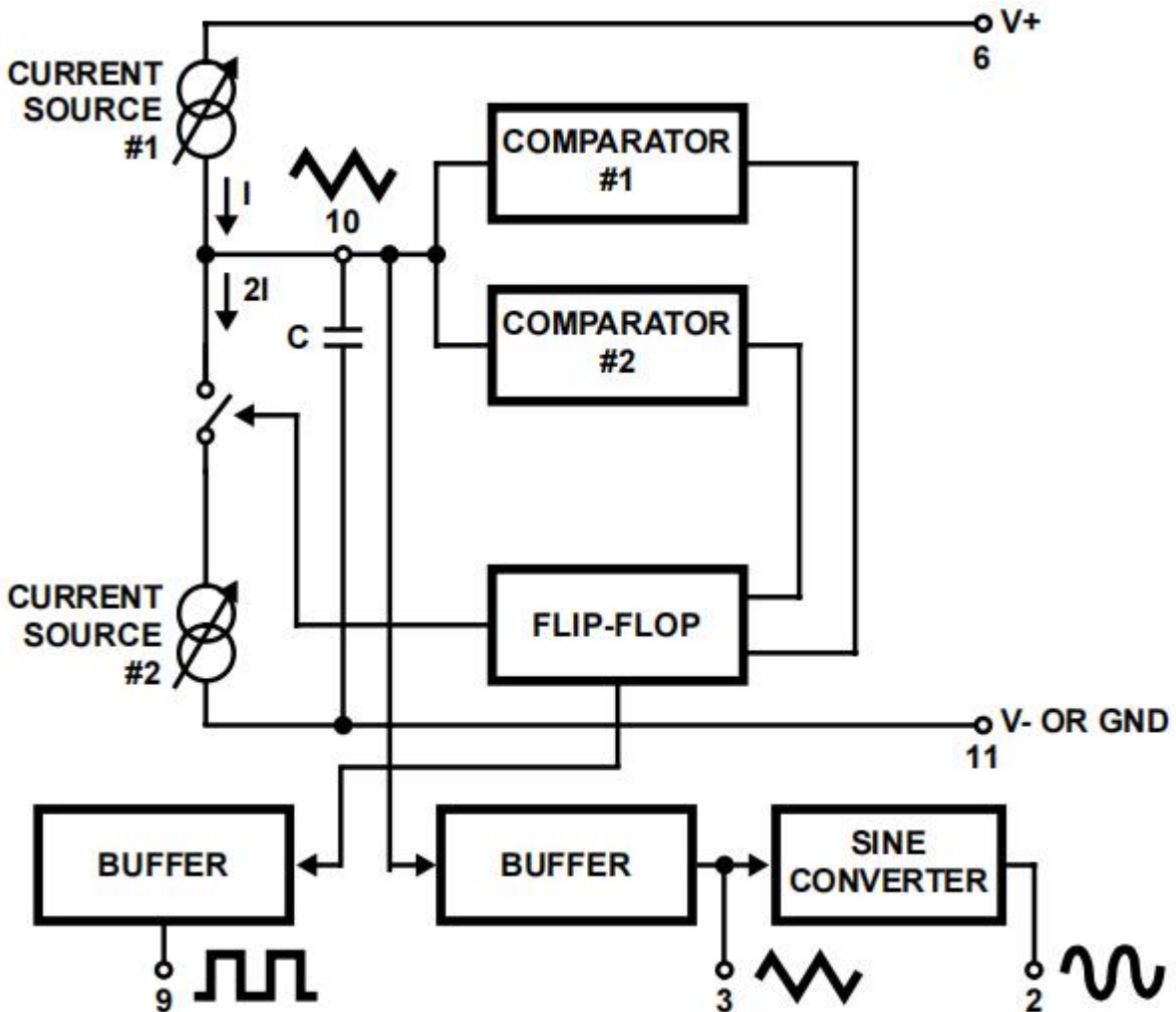
The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

**Pinout**



DIP-14/SOP-14/TSSOP-14

**Functional Diagram**



**Absolute Maximum Ratings**<sup>(Note 1)</sup>

Parameter	Value
Supply Voltage (V- to V+)	36V
Input Voltage (Any Pin)	V- to V+
Input Current (Pins 4 and 5)	25mA
Output Sink Current (Pins 3 and 9)	25mA
Lead Temperature (Soldering, 10 seconds)	245°C

**Operating Conditions**

Temperature Range

Parameter	Value
ICL8038A, ICL8038B, ICL8038	0°C to 70°C

**Thermal Information**

Parameter	Value
Thermal Resistance (Typical, Note 2)	
DIP Package $\theta_{JA}$ (°C/W)	115
DIP Package $\theta_{JC}$ (°C/W)	N/A
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C

**Die Characteristics**

Back Side Potential	V-
---------------------	----

NOTE:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.
2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$V_{\text{SUPPLY}} = \pm 10\text{V}$  or  $+20\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$ , Test Circuit Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038			ICL8038B			ICL8038A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Operating Range	$V_{\text{SUPPLY}}$ V+	Single Supply	+10	-	+30	+10	-	+30	+10	-	+30	V
	V+, V-	Dual Supplies	$\pm 5$	-	$\pm 15$	$\pm 5$	-	$\pm 15$	$\pm 5$	-	$\pm 15$	V
Supply Current	$I_{\text{SUPPLY}}$	$V_{\text{SUPPLY}} = 10\text{V}$ (Note 2)		12	20	-	12	20	-	12	20	mA
<b>FREQUENCY CHARACTERISTICS</b> (All Waveforms)												
Max. Frequency of Oscillation	$f_{\text{MAX}}$		100	-	-	100	-	-	100	-	-	kHz
Sweep Frequency of FM Input	$f_{\text{SWEEP}}$		-	10	-	-	10	-	-	10	-	kHz
Sweep FM Range		(Note 3)	-	35:1	-	-	35:1	-	-	35:1	-	
FM Linearity		10:1 Ratio	-	0.5	-	-	0.2	-	-	0.2	-	%
Frequency Drift with Temperature (Note 5)	$\Delta f/\Delta T$	$0^\circ\text{C}$ to $70^\circ\text{C}$	-	250	-	-	180	-	-	120		ppm/ $^\circ\text{C}$
Frequency Drift with Supply Voltage	$\Delta f/\Delta V$	Over Supply Voltage Range	-	0.05	-	-	0.05		-	0.05	-	%/V
<b>OUTPUT CHARACTERISTICS</b>												
Square Wave Leakage Current	$I_{\text{OLK}}$	$V_g = 30\text{V}$	-	-	1	-	-	1	-	-	1	$\mu\text{A}$
Saturation Voltage	$V_{\text{SAT}}$	$I_{\text{SINK}} = 2\text{mA}$	-	0.2	0.5	-	0.2	0.4	-	0.2	0.4	V
Rise Time	$t_{\text{R}}$	$R_L = 4.7\text{k}\Omega$	-	180	-	-	180	-	-	180	-	ns
Fall Time	$t_{\text{F}}$	$R_L = 4.7\text{k}\Omega$	-	40	-	-	40	-	-	40	-	ns
Typical Duty Cycle Adjust (Note 6)	$\Delta D$		2		98	2	-	98	2	-	98	%
Triangle/Sawtooth/Ramp Amplitude	$V_{\text{TRIANGLE}}$	$R_{\text{TRI}} = 100\text{k}\Omega$	0.30	0.33	-	0.30	0.33	-	0.30	0.33	-	$\times V_{\text{SUPPLY}}$
Linearity			-	0.1	-	-	0.05	-	-	0.05	-	%
Output Impedance	$Z_{\text{OUT}}$	$I_{\text{OUT}} = 5\text{mA}$	-	200	-	-	200	-	-	200	-	$\Omega$
Sine Wave Amplitude	$V_{\text{SINE}}$	$R_{\text{SINE}} = 100\text{k}\Omega$	0.2	0.22	-	0.2	0.22	-	0.2	0.22	-	$\times V_{\text{SUPPLY}}$
THD	THD	$R_{\text{S}} = 1\text{M}$ (Note 4)	-	2.0	5	-	1.5	3	-	1.0	1.5	%
THD Adjusted	THD	Use Figure 4	-	1.5	-	-	1.0	-	-	0.8	-	%

### NOTES:

1. RA and RB currents not included.
2.  $V_{\text{SUPPLY}} = 20\text{V}$ ; RA and RB =  $10\text{k}\Omega$ ,  $f \cong 10\text{kHz}$  nominal; can be extended 1000 to 1. See Figures 5A and 5B.
3.  $82\text{k}\Omega$  connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use RA and RB.)
4. Figure 1, pins 7 and 8 connected,  $V_{\text{SUPPLY}} = 10\text{V}$ . See Typical Curves for T.C. vs  $V_{\text{SUPPLY}}$ .
5. Not tested, typical value for design purposes only.

## Test Conditions

PARAMETER	RA	RB	RL	C	SW <sub>1</sub>	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current Into Pin 6
Sweep FM Range (Note 7)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage (Note 8)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude (Note 10) Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 2
10kΩ	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 3
Leakage Current (Off) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (On) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Output (Low) at Pin 9
Rise and Fall Times (Note 11)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust (Note 11) Max	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Min	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

### NOTES:

- The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 ( $f_{HI}$ ) and then connecting pin 8 to pin 6 ( $f_{LO}$ ). Otherwise apply Sweep Voltage at pin 8 ( $\frac{2}{3} V_{SUPPLY} + 2V$ )  $V_{SWEEP} \leq V_{SUPPLY}$  where  $V_{SUPPLY}$  is the total supply voltage. In Figure 5B, pin 8 should vary between 5.3V and 10V with respect to ground.
- $8. 10V \leq V+ \leq 30V$ , or  $\pm 5V \leq V_{SUPPLY} \leq 15V$ .
- Oscillation can be halted by forcing pin 10 to +5V or -5V.
- Output Amplitude is tested under static conditions by forcing pin 10 to 5V then to -5V.
- Not tested; for design purposes only.

## Test Circuit

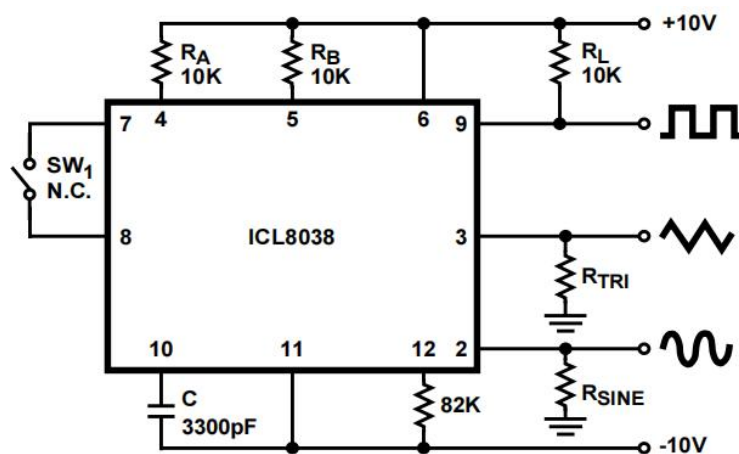
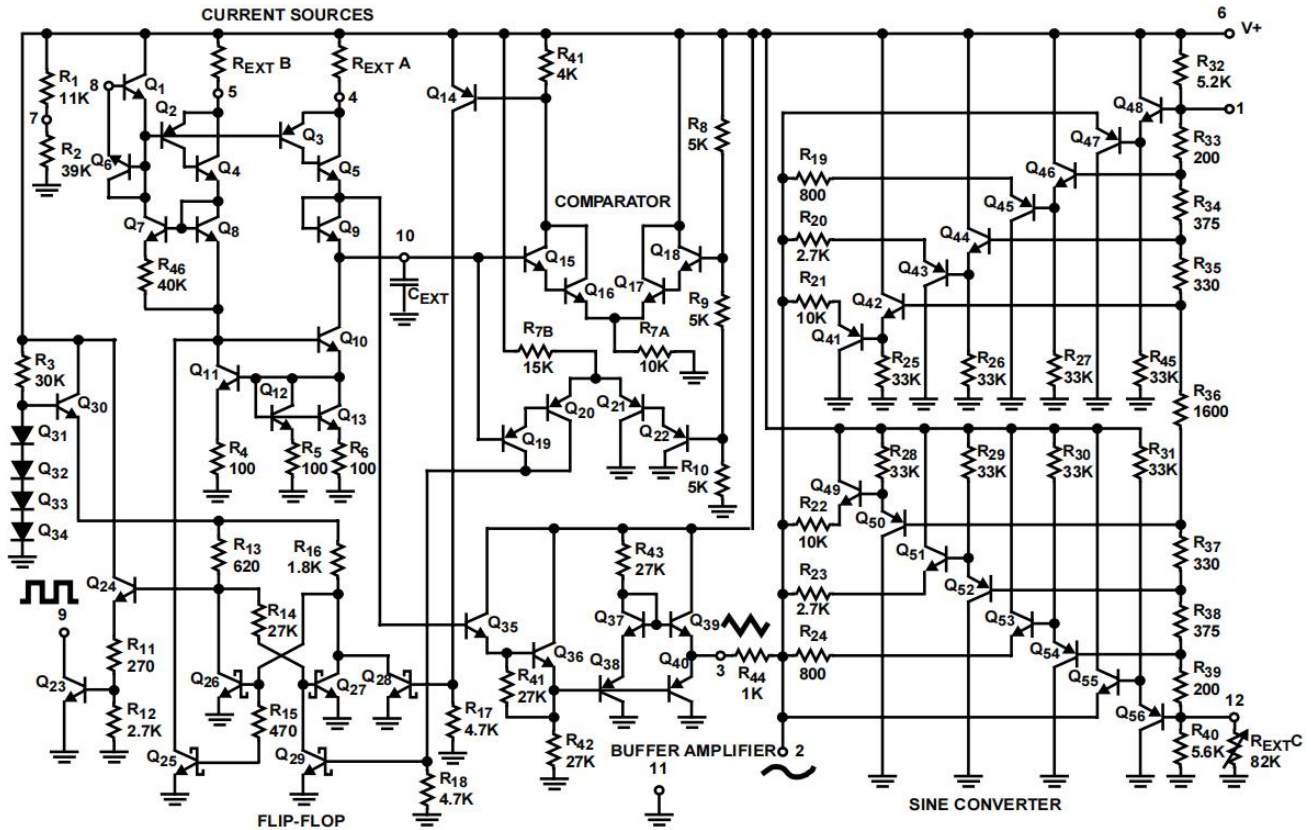


FIGURE 1. TEST CIRCUIT

## Detailed Schematic



## Application Information(See Functional Diagram)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at Terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at Terminal 9.

The sine wave is created by feeding the triangle wave into a nonlinear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves toward the two extremes.

## Waveform Timing

The symmetry of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 3. Best results are obtained by keeping the timing resistors  $R_A$  and  $R_B$  separate (A).  $R_A$  controls the rising portion of the triangle and sine wave and the 1 state of the square wave.

The magnitude of the triangle waveform is set at  $1/3 V_{SUPPLY}$ ; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times 1/3 \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{1} = \frac{C \times 1/3 V_{SUPPLY}}{2(0.22) \frac{V_{SUPPLY}}{R_B} - 0.22 \frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when  $R_A = R_B$ .

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 3B is slightly more convenient. A  $1k\Omega$  potentiometer may not allow the duty cycle to be adjusted through 50% on all devices. If a 50% duty cycle is required, a  $2k\Omega$  or  $5k\Omega$  potentiometer should be used. With two separate timing resistors, the frequency is given by:

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66} \left( 1 + \frac{R_B}{2R_A - R_B} \right)}$$

or, if  $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 3A)}$$

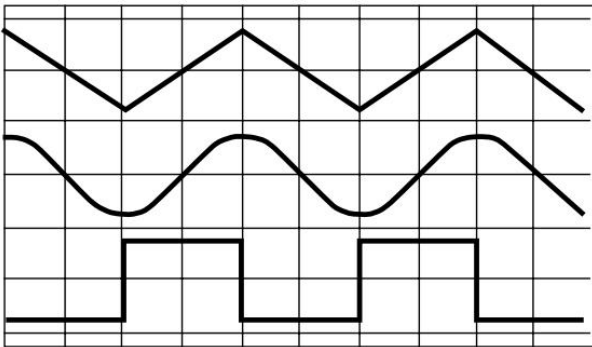


FIGURE 2A. SQUARE WAVE DUTY CYCLE - 50%

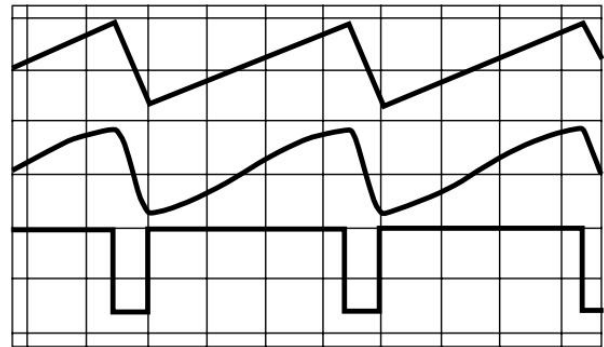


FIGURE 2B. SQUARE WAVE DUTY CYCLE - 80%

**FIGURE 2. PHASE RELATIONSHIP OF WAVEFORMS**



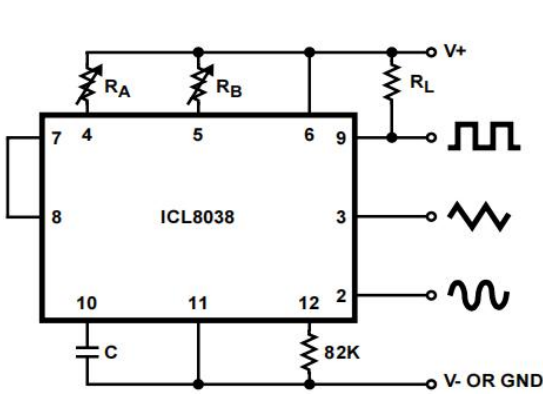


FIGURE 3A.

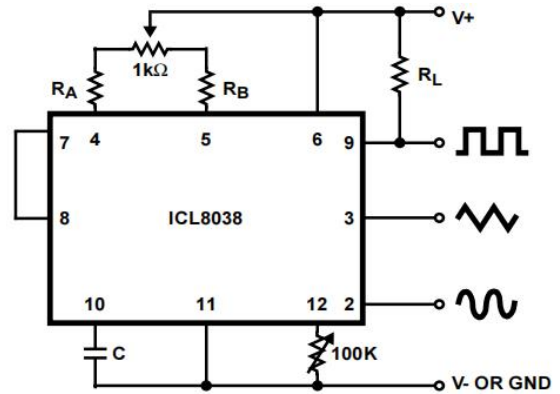


FIGURE 3B.

FIGURE 3. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents and thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

### Reducing Distortion

To minimize sine wave distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 4; this configuration allows a typical reduction of sine wave distortion close to 0.5%.

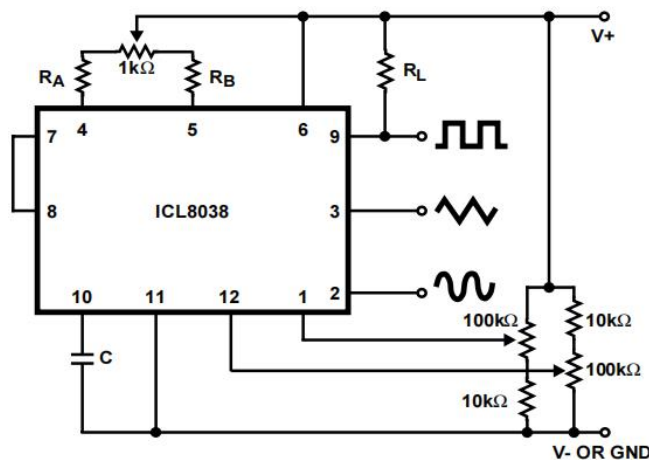


FIGURE 4. CONNECTION TO ACHIEVE MINIMUM SINE WAVE DISTORTION

### Selecting RA, RB and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents ( $I > 5\text{mA}$ ), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to RA can be calculated from:

$$I = \frac{R_1 \times (V_+ - V_-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V_+ - V_-)}{R_A}$$



R1 and R2 are shown in the Detailed Schematic.

A similar calculation holds for RB.

The capacitor value should be chosen at the upper end of its possible range.

## Waveform Out Level Control and Power Supplies

The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply ( $\pm 5V$  to  $\pm 15V$ ). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

## Frequency Modulation and Sweeping

The frequency of the waveform generator is a direct function of the DC voltage at Terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g.  $\pm 10\%$ ) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 5A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about  $8k\Omega$  (pins 7 and 8 connected together), to about  $(R + 8k\Omega)$ .

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 5B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created ( $f = 0$  at  $V_{SWEEP} = 0$ ). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by  $(1/3 V_{SUPPLY} - 2V)$ .

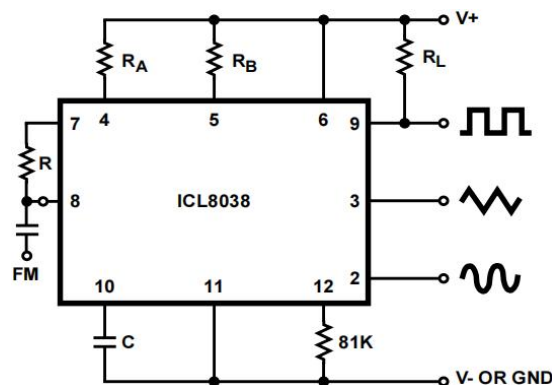


FIGURE 5A. CONNECTIONS FOR FREQUENCY MODULATION

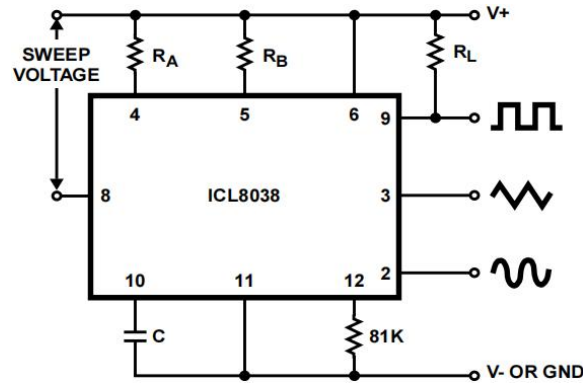


FIGURE 5B. CONNECTIONS FOR FREQUENCY SWEEP

FIGURE 5.

## Typical Applications

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 6 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

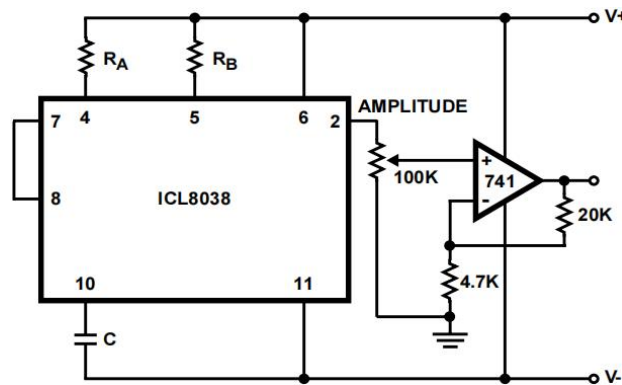


FIGURE 6. SINE WAVE OUTPUT BUFFER AMPLIFIERS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 7 shows a FET switch, diode ANDED with an input strobe signal to allow the output to always start on the same slope.

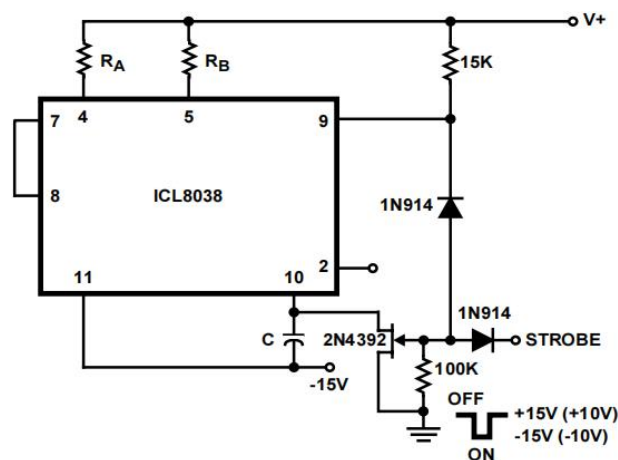


FIGURE 7. STROBE TONE BURST GENERATOR

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors RA and RB must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of RA and RB by a few hundred mV. The Circuit of Figure 8 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 10.

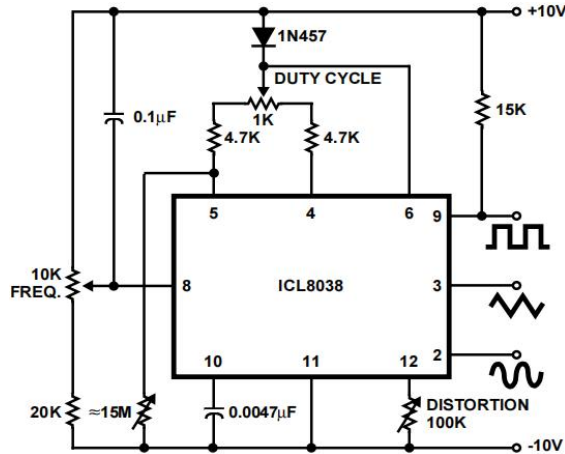


FIGURE 8. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHzY

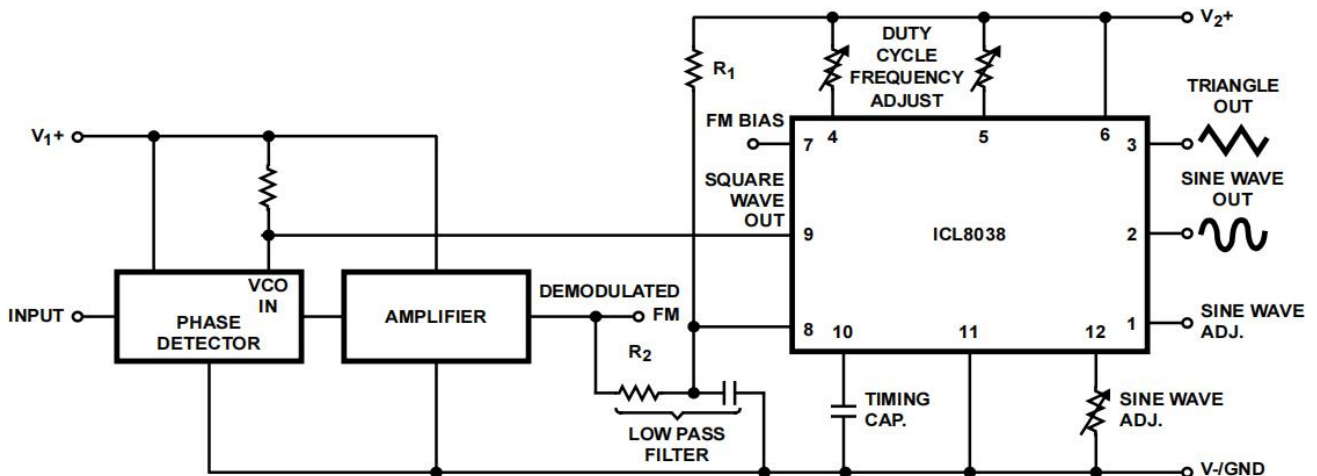


FIGURE 9. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP

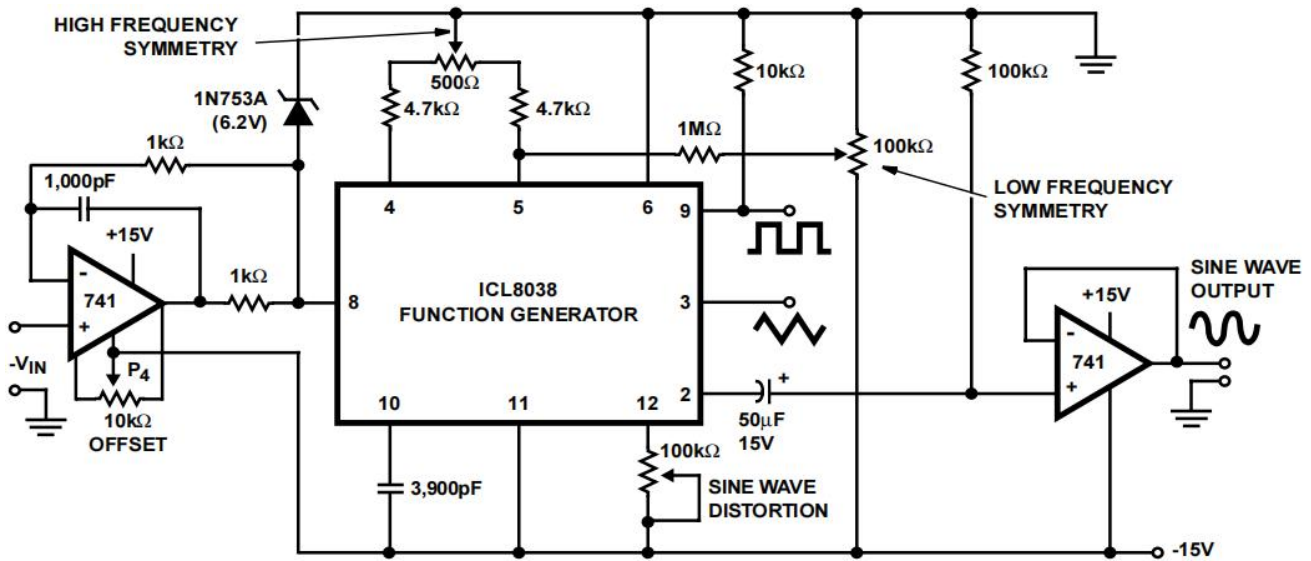


FIGURE 10. LINEAR VOLTAGE CONTROLLED OSCILLATOR

## Use in Phase Locked Loops

Its high frequency stability makes the ICL8038 an ideal building block for a phase locked loop as shown in Figure 9. In this application the remaining functional blocks, the phase detector and the amplifier, can be formed by a number of available ICs (e.g., MC4344, NE562).

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to  $V+$  ( $R_1$ ,  $R_2$  as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note AN013, "Everything You Always Wanted to Know About the ICL8038".

## Definition of Terms

**Supply Voltage** ( $V_{SUPPLY}$ ). The total supply voltage from  $V+$  to  $V-$ .

**Supply Current**. The supply current required from the power supply to operate the device, excluding load currents and the currents through  $R_A$  and  $R_B$ .

**Frequency Range**. The frequency range at the square wave output through which circuit operation is guaranteed.

**Sweep FM Range**. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range:

$$(\frac{2}{3} V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

**FM Linearity**. The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

**Output Amplitude**. The peak-to-peak signal amplitude appearing at the outputs.

**Saturation Voltage**. The output voltage at the collector of Q23 when this transistor is turned on. It is measured for a sink current of 2mA.

**Rise and Fall Times**. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

**Triangle Waveform Linearity**. The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

**Total Harmonic Distortion**. The total harmonic distortion at the sine wave output.

## Typical Performance Curves

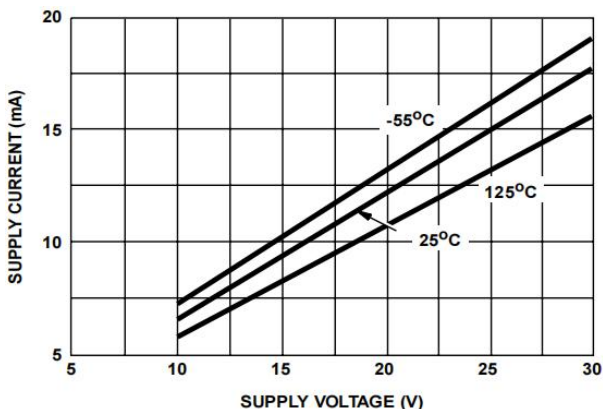


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

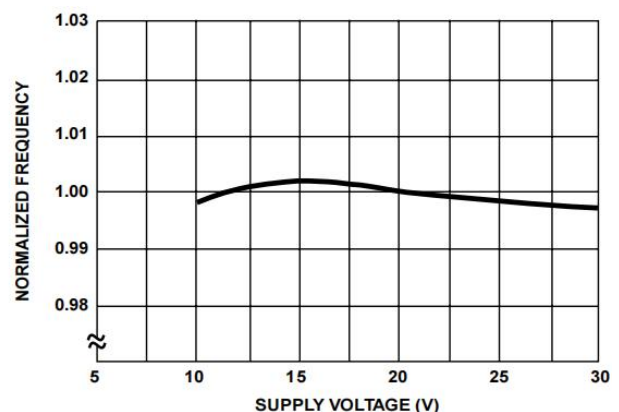


FIGURE 12. FREQUENCY vs SUPPLY VOLTAGE

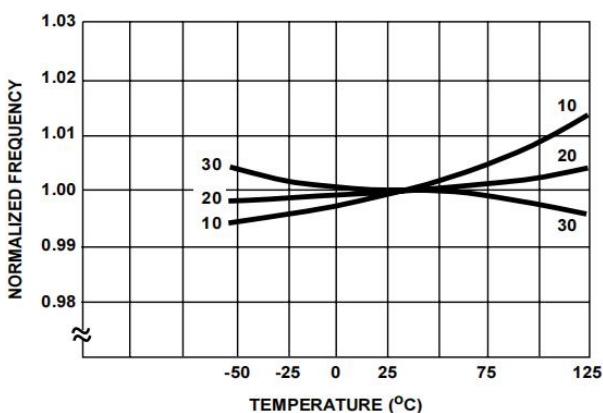


FIGURE 13. FREQUENCY vs TEMPERATURE

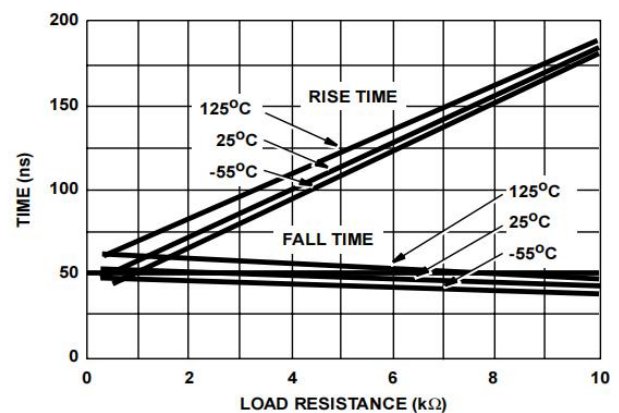


FIGURE 14. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE

Typical Performance Curves (Continued)

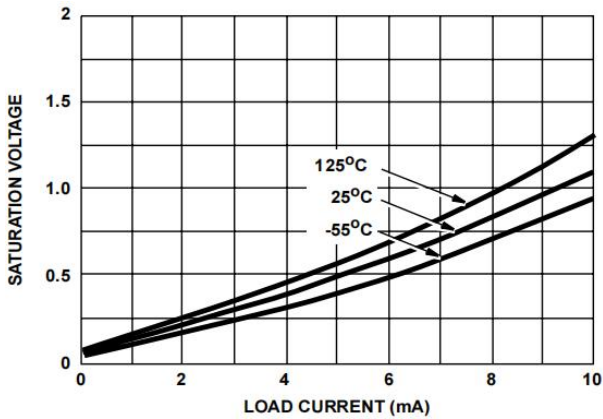


FIGURE 15. SQUARE WAVE SATURATION VOLTAGE vs LOAD CURRENT

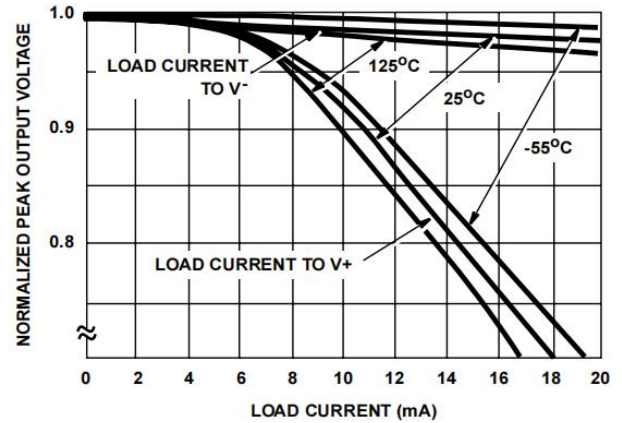


FIGURE 16. TRIANGLE WAVE OUTPUT VOLTAGE vs LOAD CURRENT

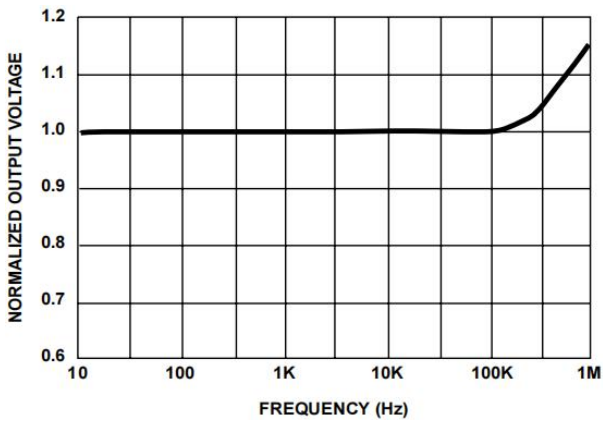


FIGURE 17. TRIANGLE WAVE OUTPUT VOLTAGE vs FREQUENCY

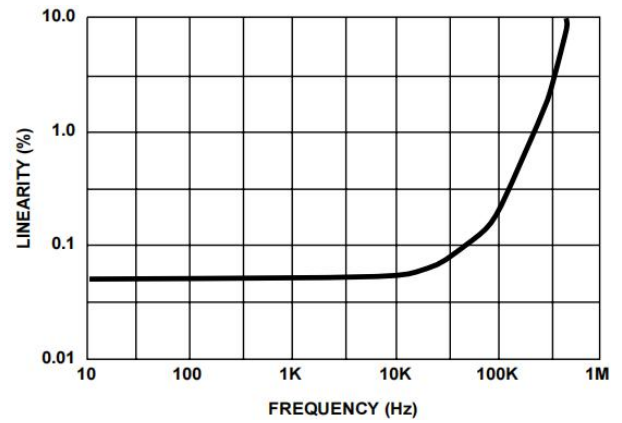


FIGURE 18. TRIANGLE WAVE LINEARITY vs FREQUENCY

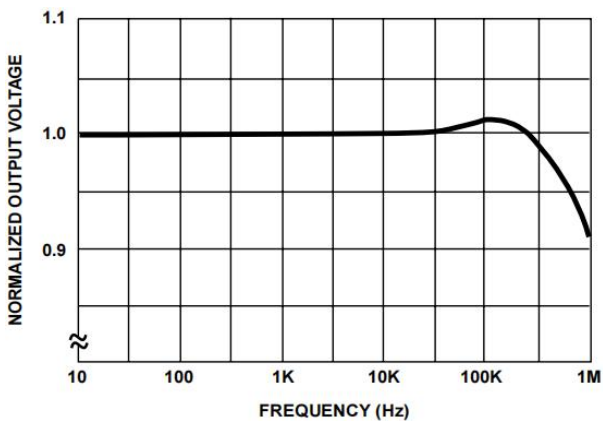


FIGURE 19. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

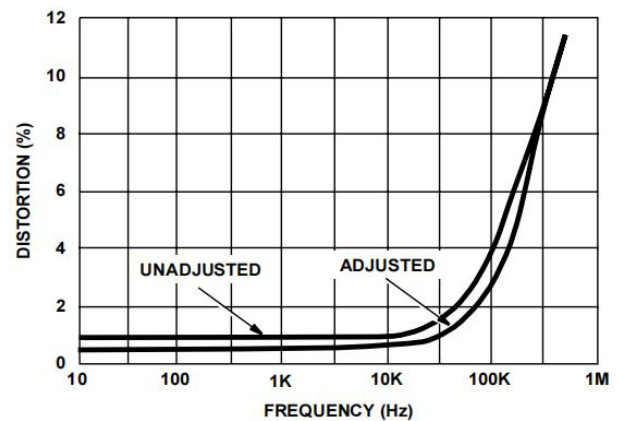
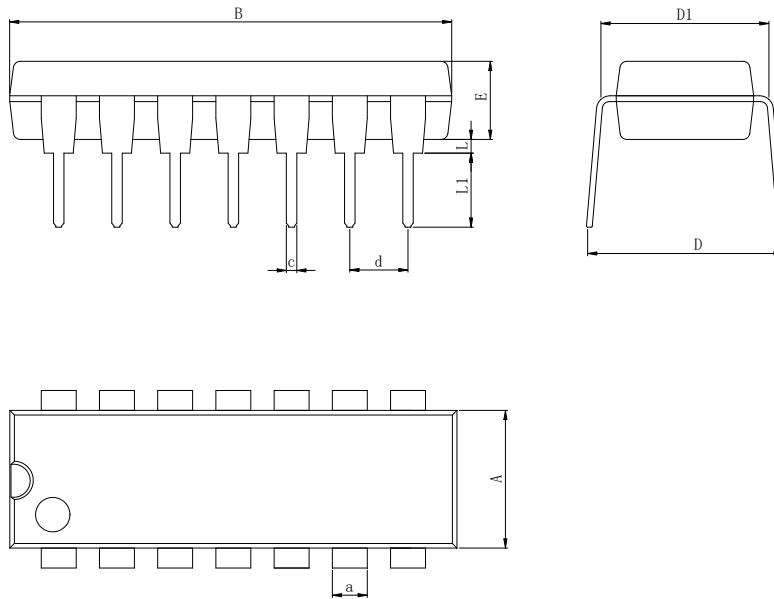


FIGURE 20. SINE WAVE DISTORTION vs FREQUENCY

## Physical Dimensions

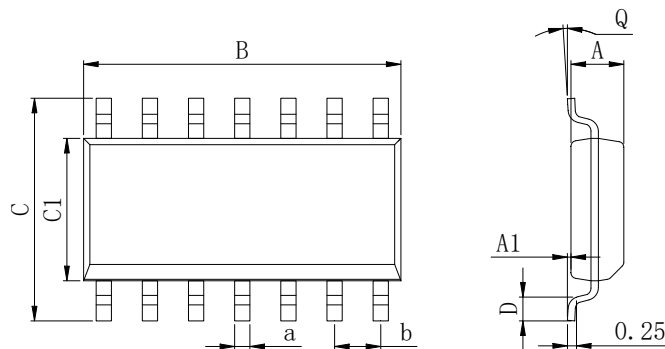
### DIP-14



Dimensions In Millimeters(DIP-14)

Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

### SOP-14



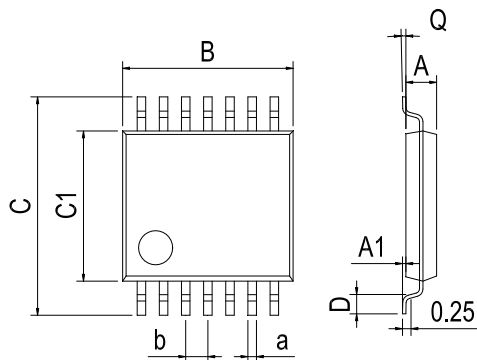
Dimensions In Millimeters(SOP-14)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	



**Physical Dimensions**

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

## Revision History

DATE	REVISION	PAGE
2018-8-9	New	1-17
2023-10-6	Update encapsulation type、 Update Lead Temperature、 Updated DIP-14 dimension、 Add annotation for Maximum Ratings、 Add Package sop-14 and Tssop-14.	1、 3、 15

**IMPORTANT STATEMENT:**

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety, security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.

单击下面可查看定价，库存，交付和生命周期等信息

[>>HGSEMI\(华冠\)](#)