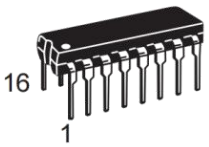
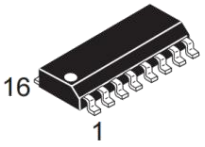
Features

- High Voltage Types (20V Rating)
- CD4518B Dual BCD Up Counter
- CD4520B Dual Binary Up Counter
- Medium Speed Operation: 6MHz Typical Clock Frequency at 10V
- Positive or Negative Edge Triggering
- Synchronous Internal Carry Propagation
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



DIP-16



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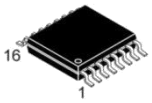


TSSOP-16

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4518BE/ CD4518BN	DIP-16	CD4518B	TUBE	1000pcs/box
CD4520BE/ CD4520BN	DIP-16	CD4520B	TUBE	1000pcs/box
CD4518BM/TR	SOP-16	CD4518B	REEL	2500pcs/reel
CD4520BM/TR	SOP-16	CD4520B	REEL	2500pcs/reel
CD4518BMT/TR	TSSOP-16	CD4518B	REEL	2500pcs/reel
CD4520BMT/TR	TSSOP-16	CD4520B	REEL	2500pcs/reel

Description

CD4518B Dual BCD Up Counter and CD4520B Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flflip-flflops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

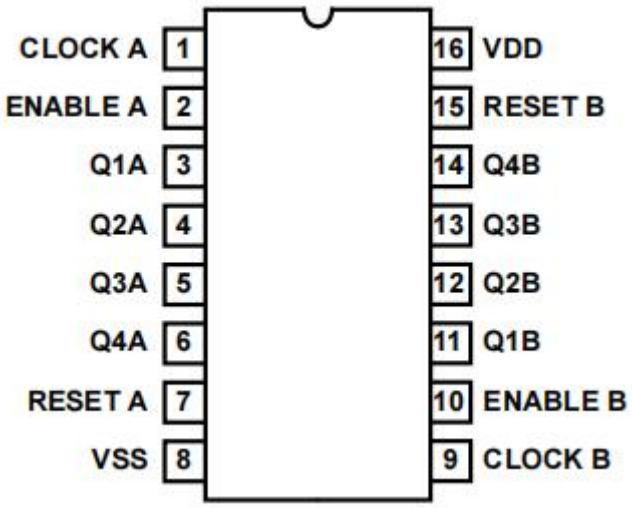
The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

Applications

- Multistage Synchronous Counting
- Multistage Ripple Counting
- Frequency Dividers

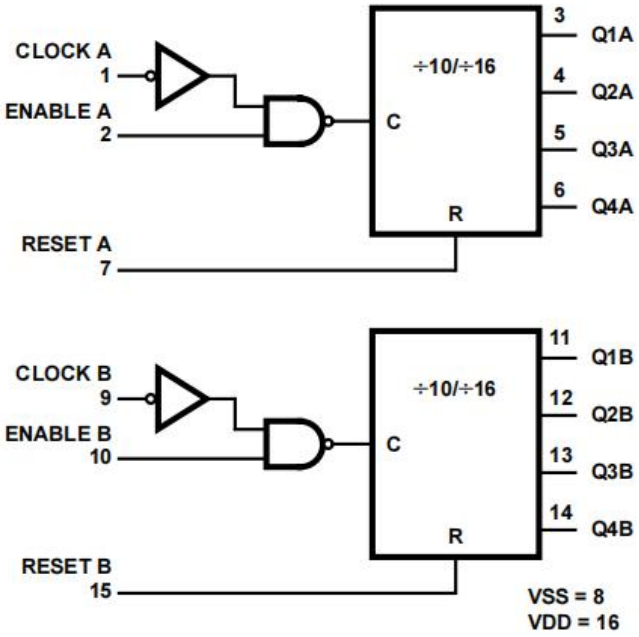
Pinout

TOP VIEW



CD4518B/CD4520B

Functional Diagram



Absolute Maximum Ratings

Condition	Min	Max	UNITS
DC Supply Voltage Range, (VDD) (Voltage Referenced to VSS Terminals)	-0.5	+20	V
Input Voltage Range, All Inputs	-0.5	Vdd+0.5	V
DC Input Current, Any One Input	-10	+10	mA
Operating Temperature Range	-40	+85	°C
Storage Temperature Range (TSTG)	-65	+150	°C
Lead Temperature (During Soldering) At Distance (1.59mm ± 0.79mm) from case for 10s Maximum	-	+245	°C

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

Dc Electrical Performance Characteristics

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	μA
				2	+85°C	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-40°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+85°C	-1000	-	nA
			VDD = 18V	3	-40°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+85°C	-	1000	nA
			VDD = 18V	3	-40°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +85°C, -40°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +85°C, -40°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+85°C			
		VDD = 3V, VIN = VDD or GND		8B	-40°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +85°C, -40°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C,+85°C, -40°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +85°C, -40°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +85°C, -40°C	11	-	V

NOTES:

1. All voltages referenced to device GND, 100% testing being implemented.

2. Go/No Go test with limits applied to inputs.

3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

Ac Electrical Performance Characteristics

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	560	ns
			10, 11	+85°C, -40°C	-	756	ns
Propagation Delay Reset to Ouput	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	650	ns
			10, 11	+85°C, -40°C	-	878	ns
Transition Time (Note 2)	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+85°C, -40°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+85°C, -40°C	1.11	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

2. -40°C and +85°C limits guaranteed, 100% testing being implemented.

Electrical Performance Characteristics

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-40°C, +25°C	-	5	μA
				+85°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-40°C, +25°C	-	10	μA
				+85°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-40°C, +25°C	-	10	μA
				+85°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +85°C,-40°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +85°C,-40°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +85°C,-40°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +85°C,-40°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+85°C	0.36	-	mA
				-40°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+85°C	0.9	-	mA
				-40°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+85°C	2.4	-	mA
				-40°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+85°C	-	-0.36	mA
				-40°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+85°C	-	-1.15	mA
				-40°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+85°C	-	-0.9	mA
				-40°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+85°C	-	-2.4	mA
				-40°C	-	-4.2	mA
Input Voltage Low	VIL	VDD=10V, VOH>9V, VOL<1V	1, 2	+25°C, +85°C,-40°C	-	3	V
Input Voltage High	VIH	VDD=10V, VOH>9V, VOL<1V	1, 2	+25°C, +85°C,-40°C	+7	-	V

Electrical Performance Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	225	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4	-	MHz
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	5	µs
Minimum Enable Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.

2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Post Irradiation Electrical Performance Characteristics

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND		+25°C			
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

Logic Diagrams

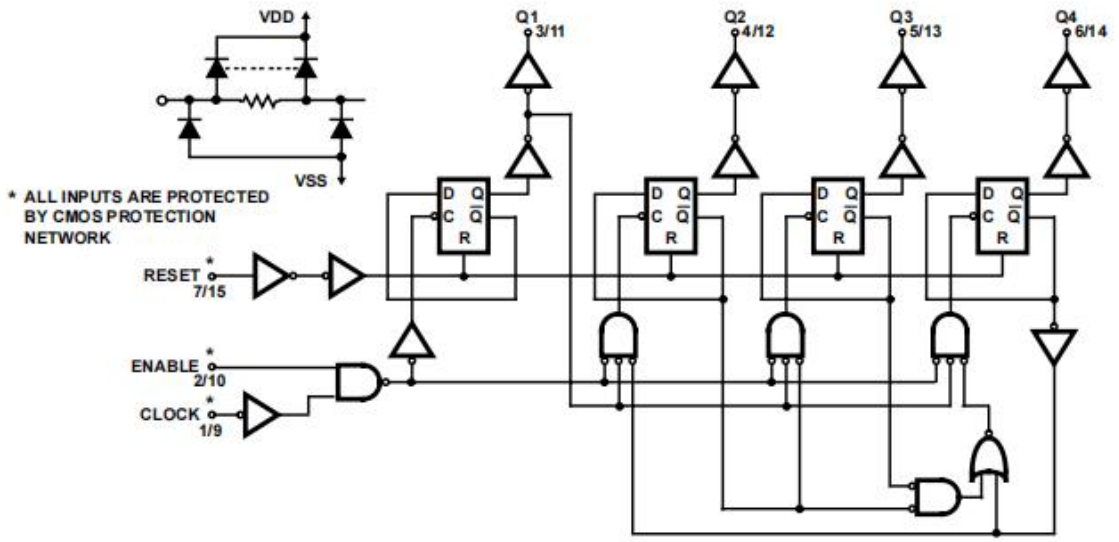


FIGURE 1. DECADE COUNTER (CD4518B) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS

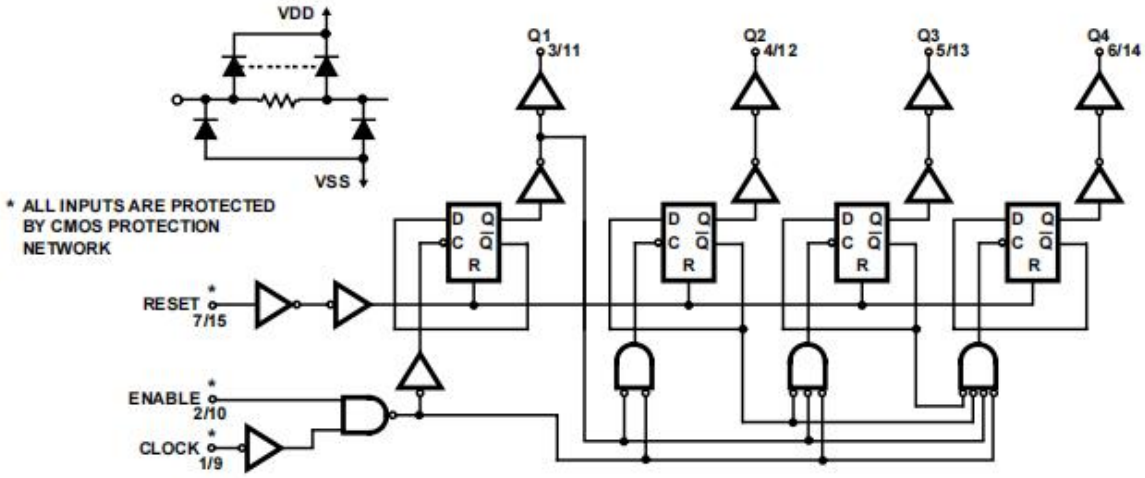


FIGURE 2. BINARY COUNTER (CD4520B) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	¬	0	Increment Counter
¬	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	¬	0	No Change
X	X	1	Q1 thru Q4 = 0

Typical Performance Curves

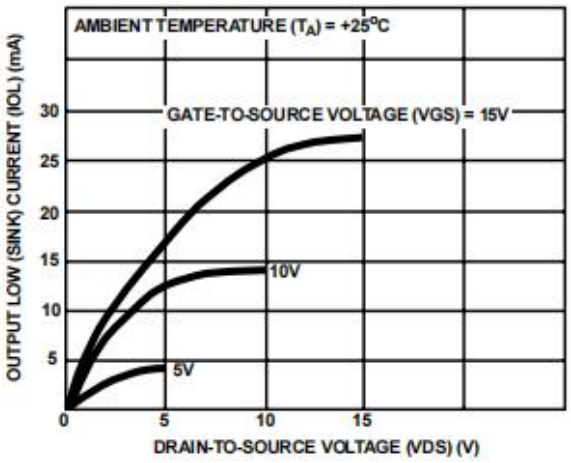


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

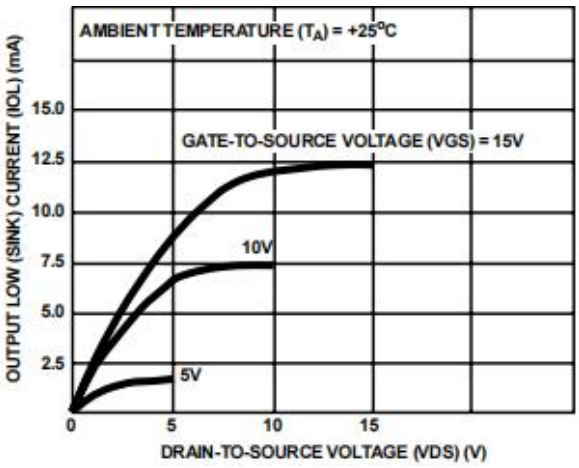


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

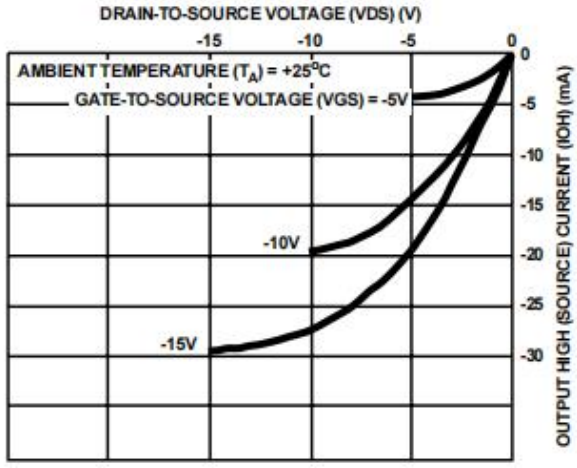


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

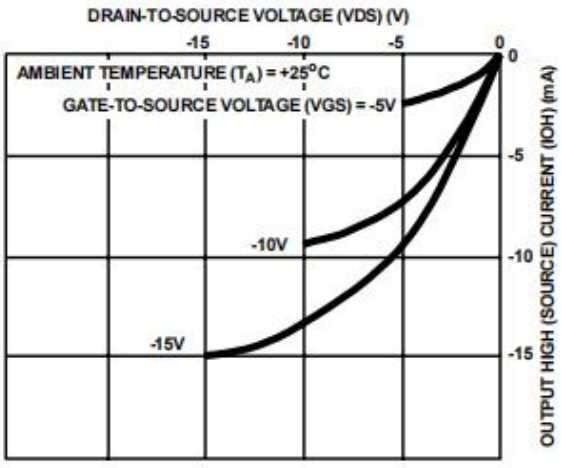


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

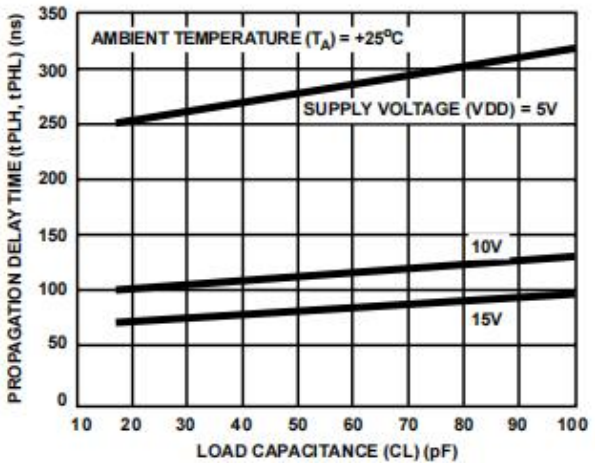


FIGURE 7. TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, CLOCK OR ENABLE TO OUTPUT

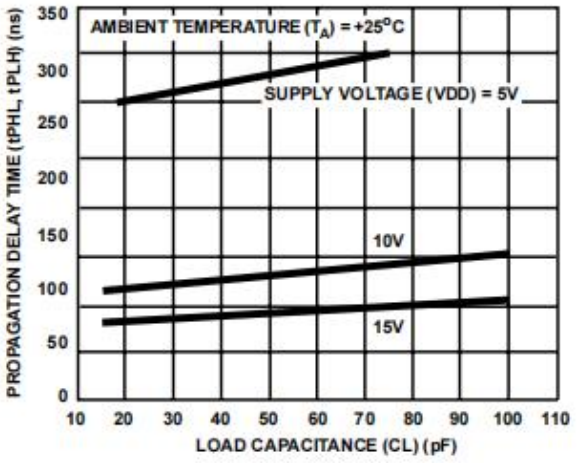


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE, RESET TO OUTPUT

Typical Performance Curves

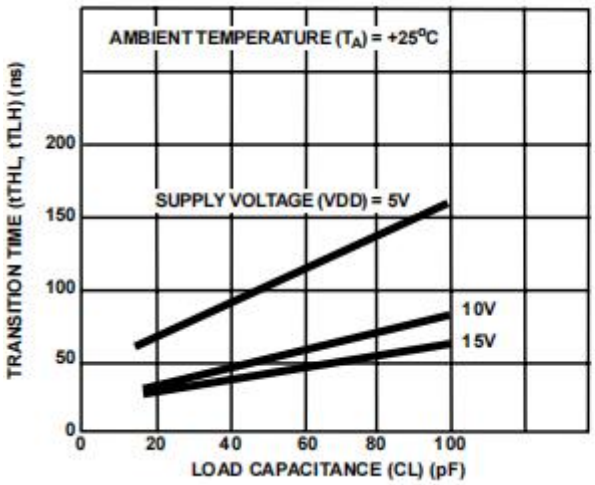


FIGURE 9. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

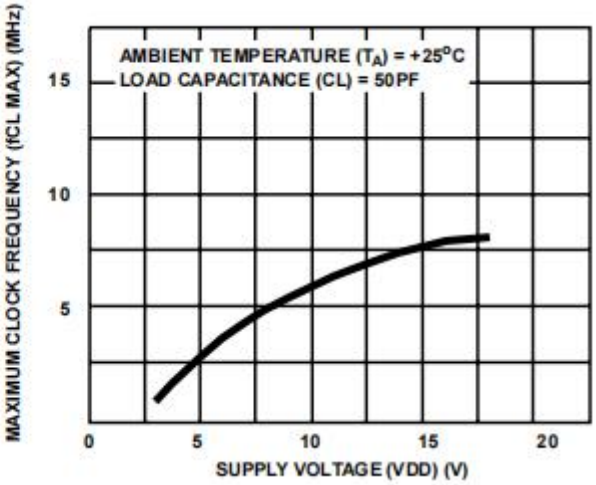


FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE

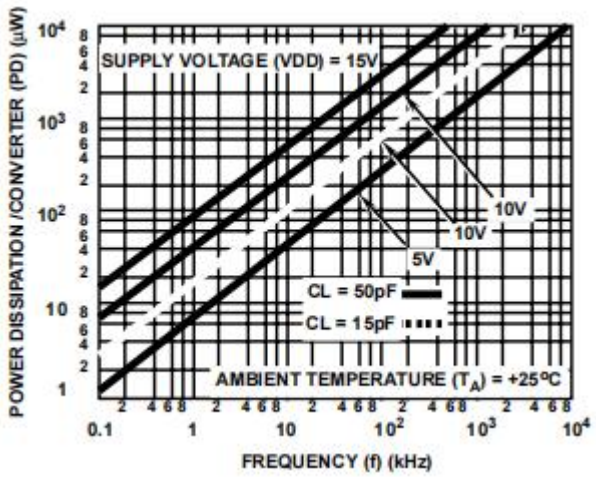


FIGURE 11. TYPICAL POWER DISSIPATION CHARACTERISTICS

Timing Diagrams

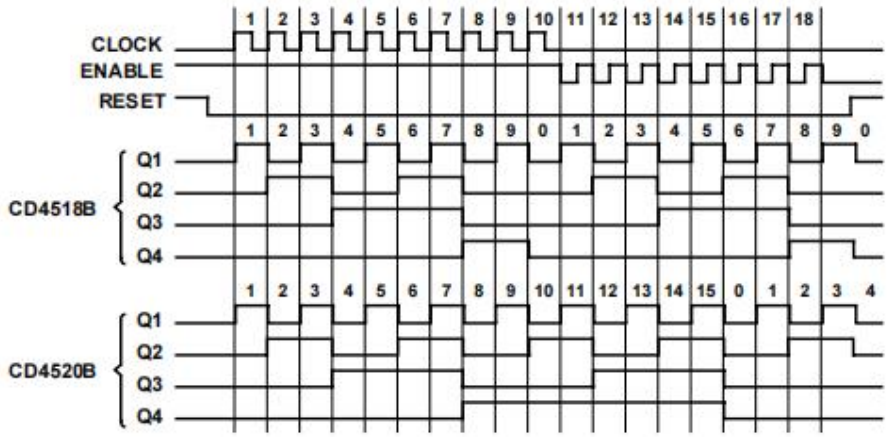


FIGURE 12. TIMING DIAGRAMS FOR CD4518B AND CD4520B

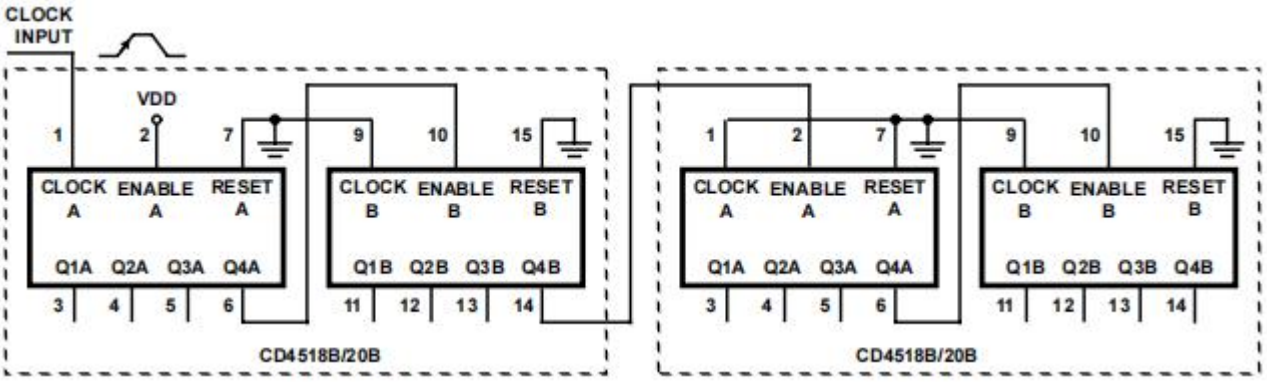
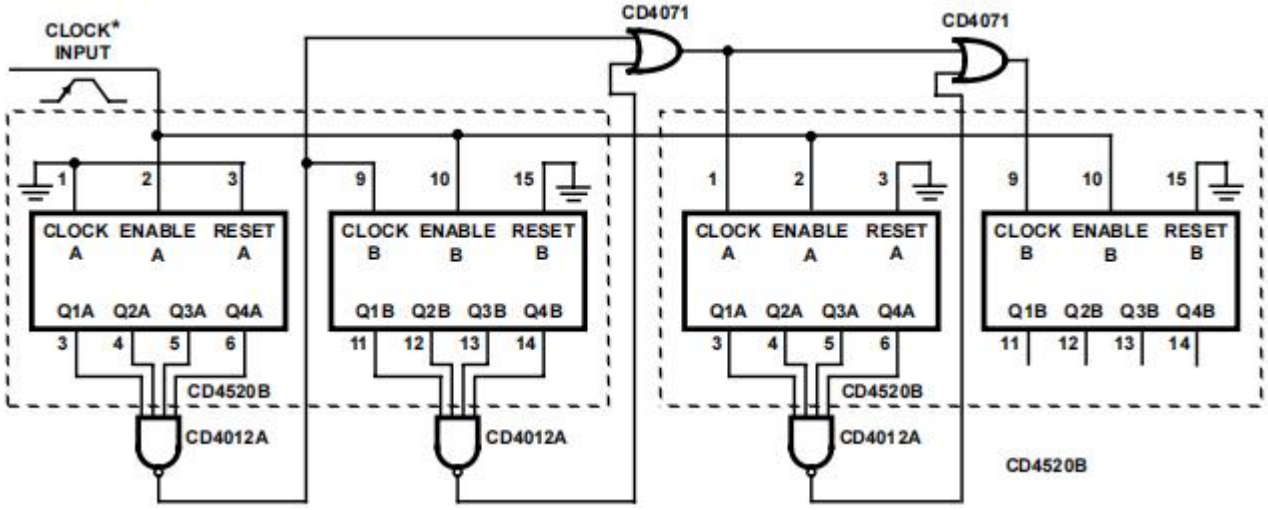


FIGURE 13. RIPPLE CASCADING OF FOUR COUNTERS WITH POSITIVE EDGE TRIGGERING

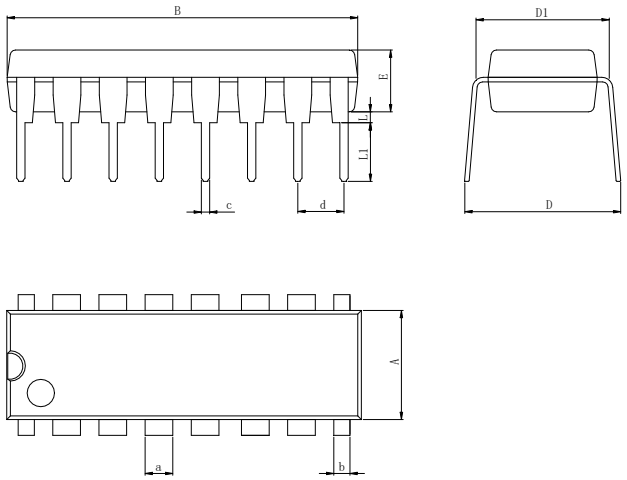


*For synchronous cascading, the clock transition time should be made less than or equal to the sum of the fifixed propagation delay at 15pF and the transition time of the output driver stage for the estimated capacitive load.

FIGURE 14. SYNCHRONOUS CASCADING OF FOUR BINARY COUNTERS WITH NEGATIVE EDGE TRIGGERING

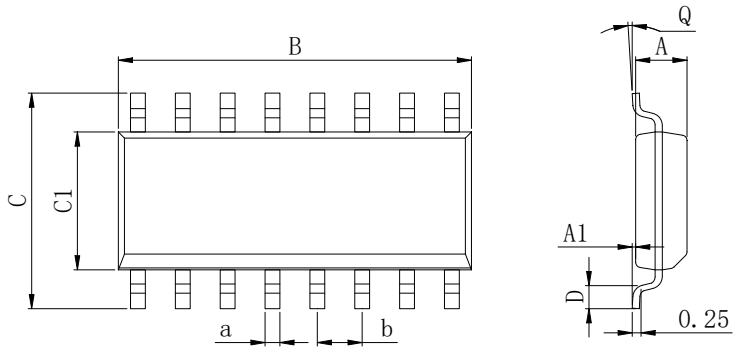
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

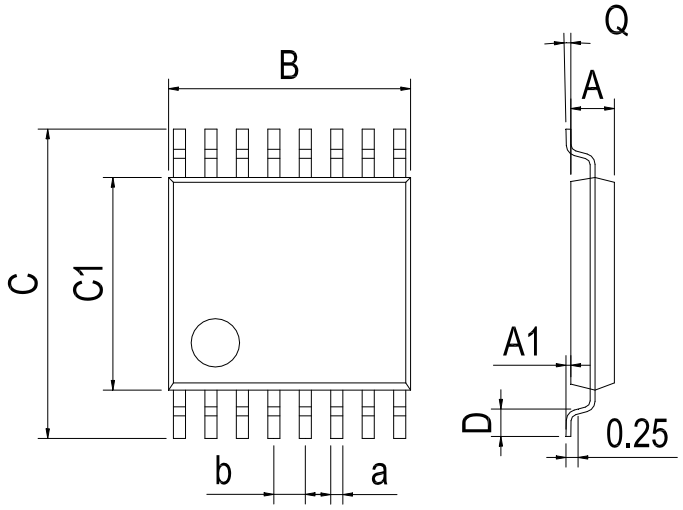
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2014-6-8	New	1-14
2023-11-15	Modify the package dimension diagram TSSOP-16、Update encapsulation type、Update Lead Temperature、Updated DIP-16dimension、Add annotation for Maximum Ratings、Update DIP Package New Model	1、3、11、12

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