TOW - Wirs Serlal EEPROM

Features

Wide Voltage Operation

- VCC = 1.8V to 5.5V

Operating Ambient Temperature: -40℃ to +85℃

Internally Organized:

- HG24C04, 512 X 8 (4K bits)

-Schmitt Trigger, Filtered Inputs for Noise Suppression

-Bidirectional Data Transfer Protocol

-1 MHz (2.5-5V), 400 kHz (1.8V) Compatibility

-Write Protect Pin for Hardware Data Protection

- 16-byte Page 4K, Write Modes

-Partial Page Writes Allowed

-Self-timed Write Cycle (5 ms max) High-reliability

- Endurance: 1 Million Write Cycles

- Data Retention: 100 Years

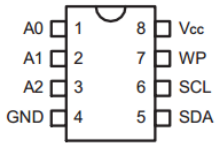
General Description

The HG24C04 provides 4096 bits of serial electrically erasable and programmable read -only memory (EEPROM) organized as 512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low -power and low-voltage operation are essentia l. The HG24C04 is available in space-saving 8-lead PDIP, 8-lead SOP, 8-lead TSSOP ,8-lead MSOP, 8 PAD DFN and SOT23-5 packages and is accessed via a two-wire serial interface.

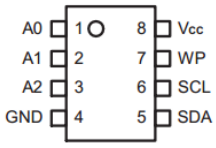
Pin Configuration

Pin Name	Founctions
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
VCC	Power Supply

8 - lead PDIP

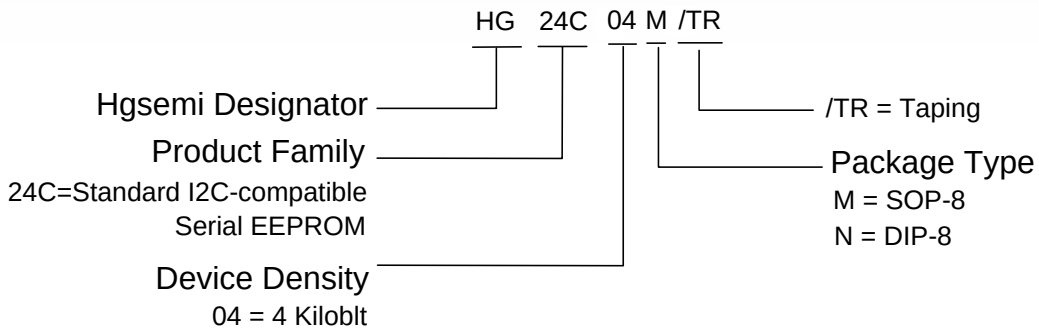


8 - lead SOP

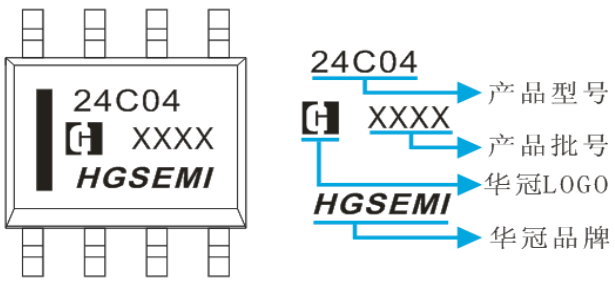


PACKAGING INFORMATION

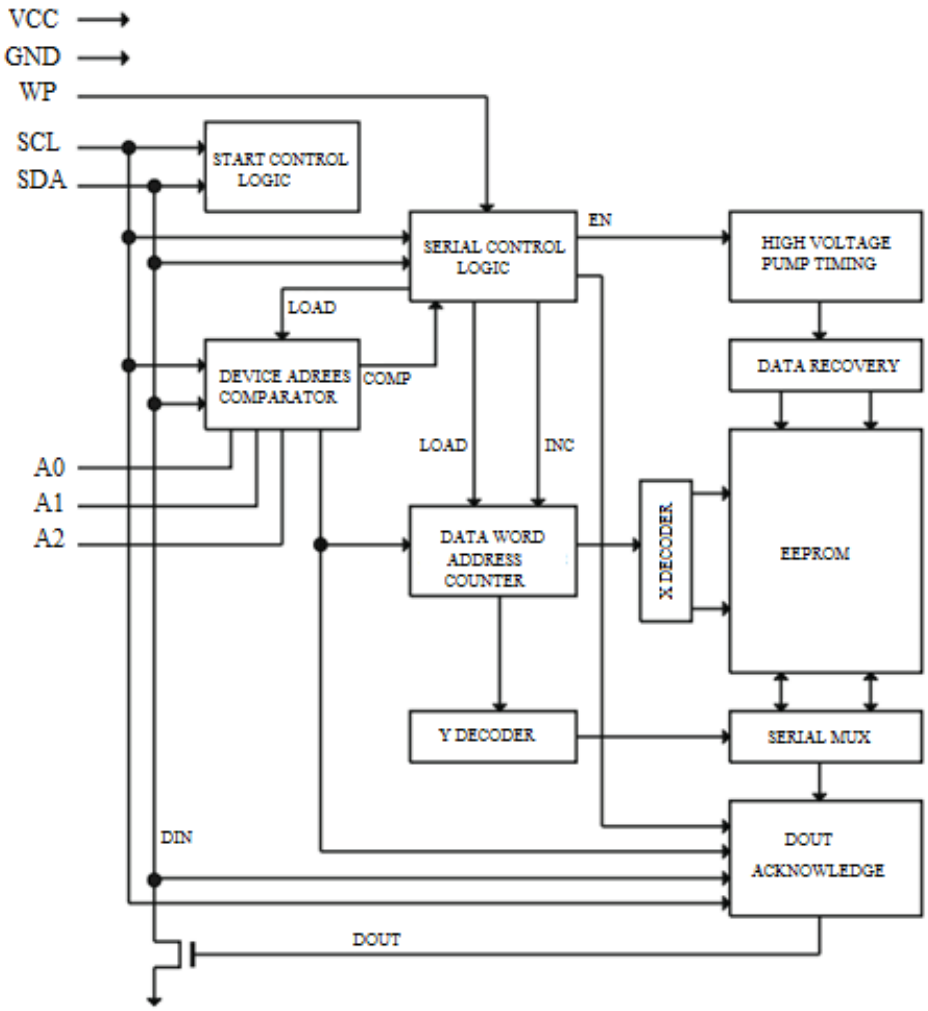
Device	Package Type	Device Marking	Package Qty
HG24C04M/TR	SOP-8	24C04	2500
HG24C04N	DIP-8	24C04	2000



MARKING



Block Diagram



Pin Descriptions

DEVICE/PAGE ADDRESSES (A2, A1 and A0):

The HG24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no conn ect and can be connected to ground.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-Read with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The HG24C04 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to VCC , the write protection feature is enabled and operates as shown in the following

Table 2:Write Protect

WP Pin Status	Part of the Array Protected
	HG24C04D
At Vcc	Full(4K)Array
At GND	Normal Read/Write Operations

Memory Organization

HG24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1 on page 4). Data changes during SCL high periods will indicate a start or stop condition as define d below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2 on page 4).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a s tandby power mode (see Figure 2 on page 4).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sen ds a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The HG24C04 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the recei pt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycle s.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start cond ition.

Figure 1: Data Validity

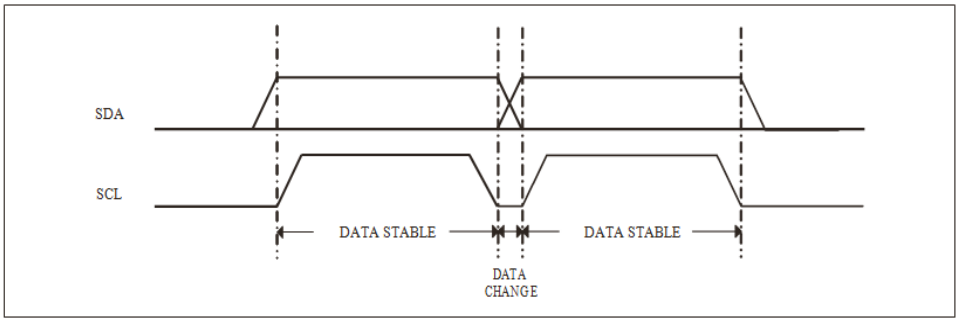


Figure 2: Start and Stop Definition

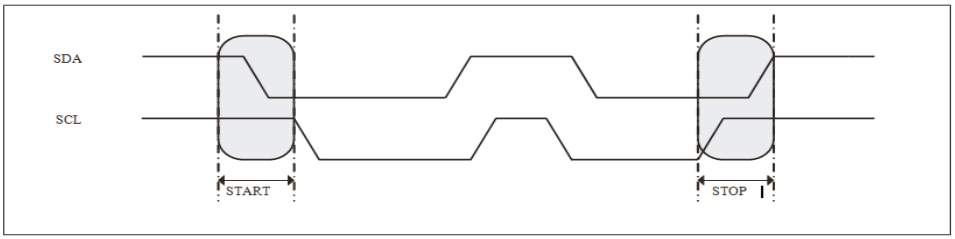
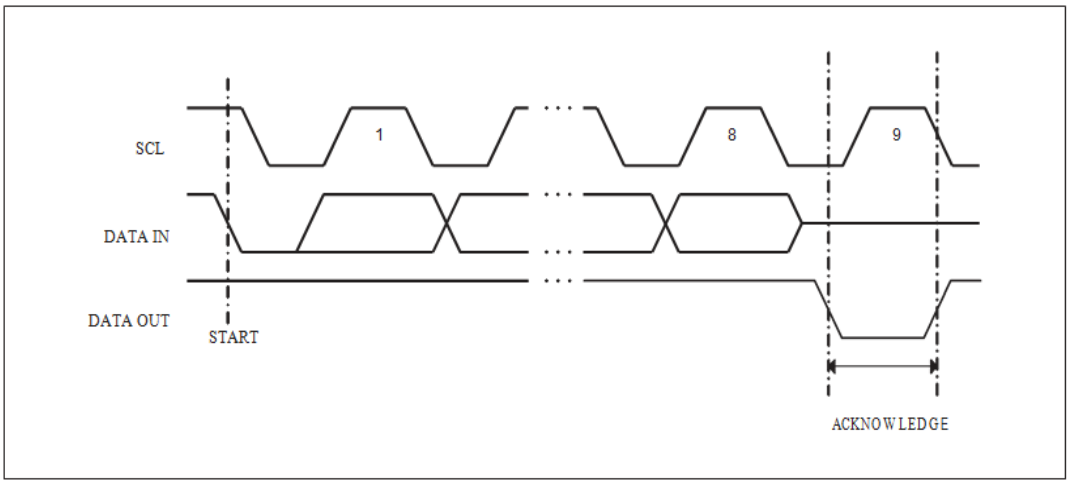


Figure 3: Output Acknowledge



Device Addressing

The 4K EEPROM devices all require an 8 - bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4 on page 7).

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device add ress bits must compare to their corresponding hardwired input pins. The A0 pin is no conn ect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device add ress, the EEPROM will output a "0 ". If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address follo wing the device address wo rd and acknowledgm en t. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is comp lete (see Figure 5 on page 7).

PAGE WRITE: The 4K -devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven 4K more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6 on page 7).

The data word address lower three 4K bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight 4K data words are tr ansmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowled ge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowi ng the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last accessed address, and incremented by one.*This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page.The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7 on page 8).

Read Operations

*For 16K EEPROM, we also provide special addressing product for certain applications, that is, . only lower 8 bits of the internal data word address counter maintains the last accessed address, the higher 3 bits (P2, P1, P0) wil l follow the device address input at each current address read .So, please contact your dealer for specia l ordering .

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledg ed by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8 on page 8).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowled ge. As long as the EEPROM receives an acknowled ge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue.The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9 on page 8).

Figure 4: Device Address

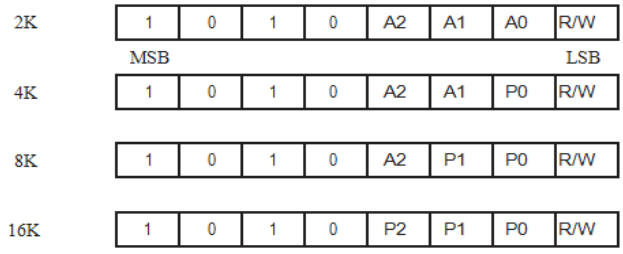


Figure 5: Byte Write

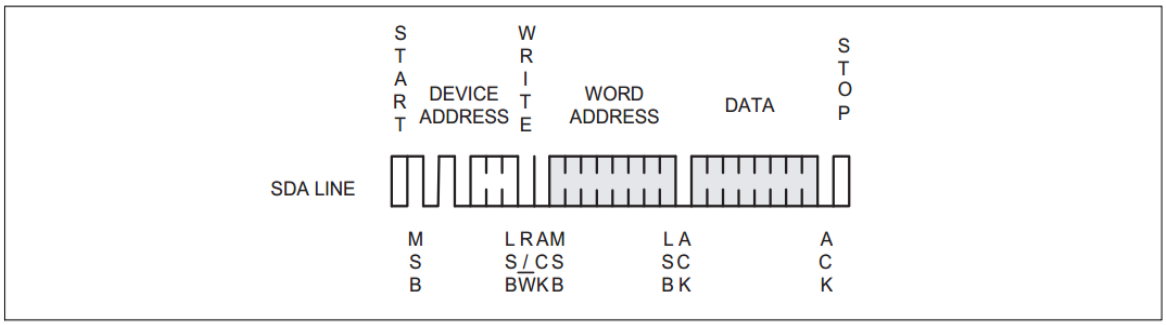


Figure 6: Page Write

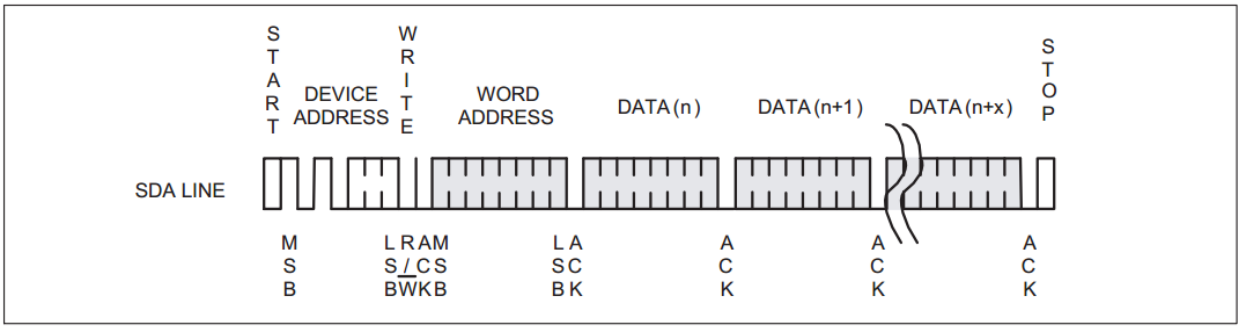


Figure 7: Current Address Read

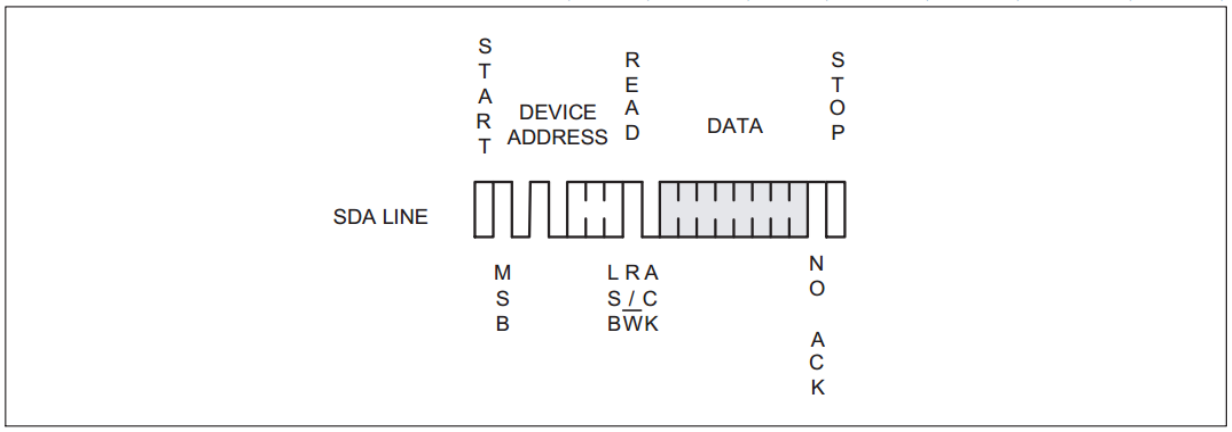


Figure 8: Random Read

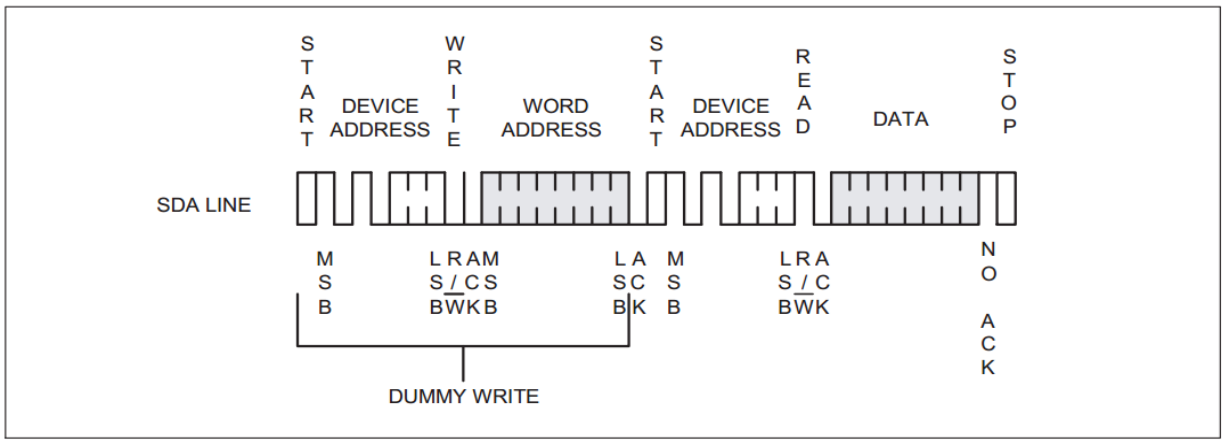
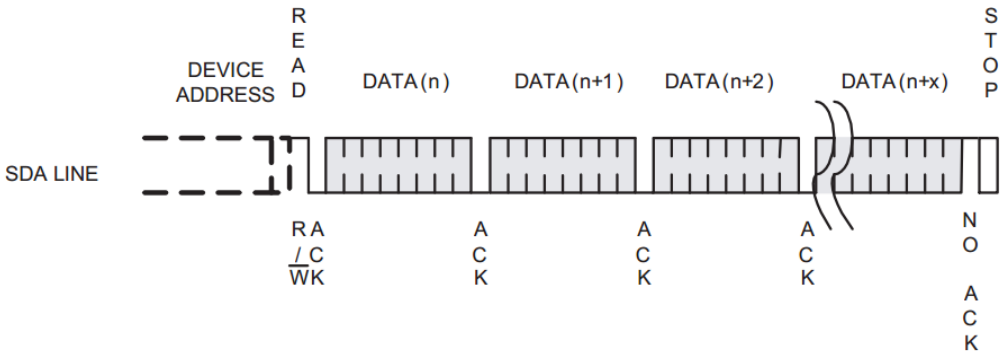


Figure 9: Sequential Read



Electrical Characteristics

Absolute Maximum Stress Ratings

DC Supply Voltage……..-0.3V to +6.5V

Input / Output Voltage ……...GND-0.3V to VCC+0.3V

Operating Ambient Temperature . . . . . -40℃ to +85℃

Storage Temperature . . . . . -65℃ to +150℃

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃,VCC = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	Vcc	1.8	—	5.5	V	
Supply Current VCC = 5.0V	I_{CC1}	—	0.4	1.0	mA	READ at 400KHz
Supply Current VCC = 5.0V	I_{CC2}	—	2.0	3.0	mA	WRITE at 400KHz
Standby Current	I_{SB}	—	—	3.0	μA	VIN=VCC or GND
Input Leakage Current	I_{LI}	—	—	3.0	μA	VIN=VCC or GND
Output Leakage Current	I_{LO}	—	0.05	3.0	μA	VOUT=VCC or GND
Input Low Level	V_{IL1}	-0.3	—	Vcc*0.3	V	Vcc=1.8V to 5.5V
Input High Level	V_{IH1}	Vcc*0.7	—	Vcc+0.3	V	Vcc=1.8V to 5.5V
Input Low Level	V_{IL2}	-0.3	—	Vcc*0.2	V	Vcc=1.7V
Input High Level	V_{IH2}	Vcc*0.7	—	Vcc+0.3	V	Vcc=1.7V
Output Low Level VCC =5.0V	V_{OL3}	—	—	0.4	V	IOL=3.0mA
Output Low Level VCC =3.0V	V_{OL2}	—	—	0.4	V	IOL=2.1mA
Output Low Level VCC =1.7V	VOL1	—	—	0.2	V	IOL=0.15mA

apac ance

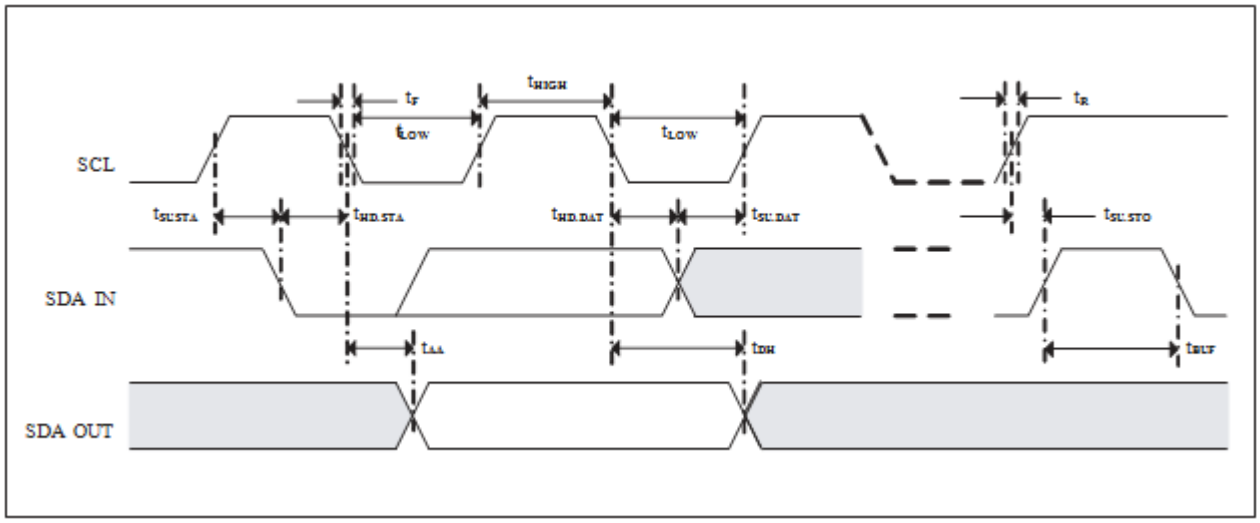
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input/Output Capacitance (SDA)	CI/O	-	-	8	pF	VI/O = 0V
Input Capacitance (A0, A1, A2, SCL)	CIN	-	-	6	pF	VIN = 0V

AC Electrical Characteristics

Parameter	Symbol	1.7v < Vcc < 2.5v			2.5v < Vcc < 5.5v			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	fSCL	-	-	400	-	-	1000	KHz
Clock Pulse Width Low	tLOW	1.2	-	-	0.6	-	-	s
Clock Pulse Width High	tHIGH	0.6	-	-	0.4	-	-	s
Noise Suppression Time	tI	-	-	50	-	-	40	ns
Clock Low to Data Out Valid	tAA	0.05	-	0.9	0.05	-	0.55	s
Time the bus must be free before a new transmission can start	tBUF	1.2	-	-	0.5	-	-	s
Start Hold Time	tHD.STA	0.6	-	-	0.25	-	-	s
Start Setup Time	tSU.STA	0.6	-	-	0.25	-	-	s
Data In Hold Time	tHD.DAT	0	-	-	0	-	-	s
Data In Setup Time	tSU.DAT	100	-	-	100	-	-	ns
Inputs Rise Time(1)	tR	-	-	0.3	-	-	0.3	s
Inputs Fall Time(1)	tF	-	-	300	-	-	100	ns
Stop Setup Time	tSU.STO	0.6	-	-	0.25	-	-	s
Data Out Hold Time	tDH	50	-	-	50	-	-	ns
Write Cycle Time	tWR	-	1.5	5	-	1.5	5	ms
5.0V, 25℃, Byte Mode	Endurance	1M	-	-	-	-	-	Write Cycles

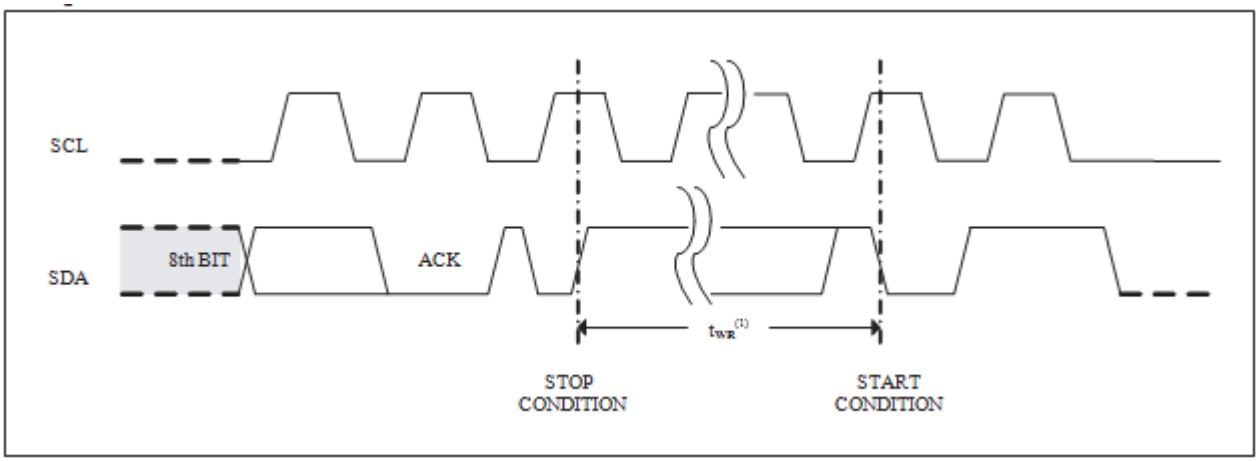
Bus Timing

Figure 10: SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

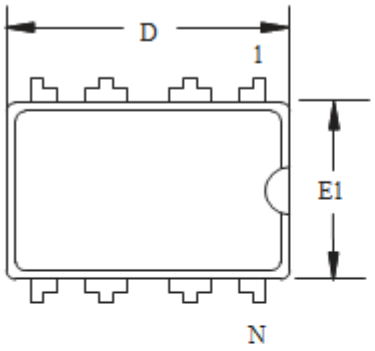
Figure 11: SCL: Serial Clock, SDA: Serial Data I/O



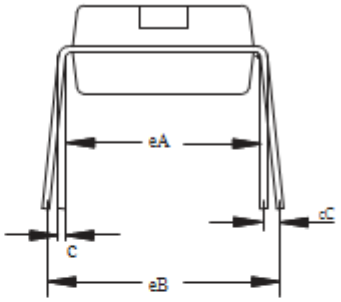
Note:

1. The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

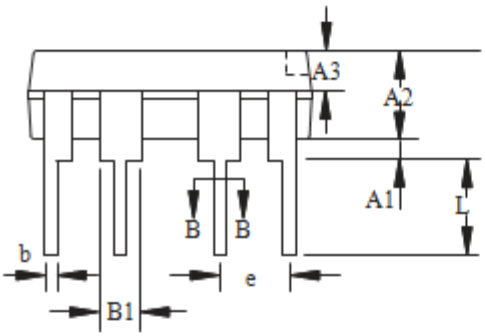
DIP8



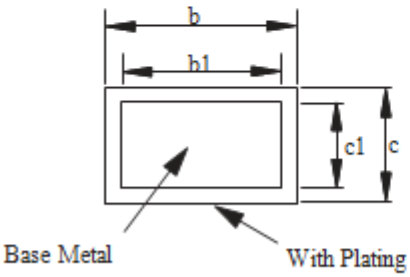
Top View



End View



Side View

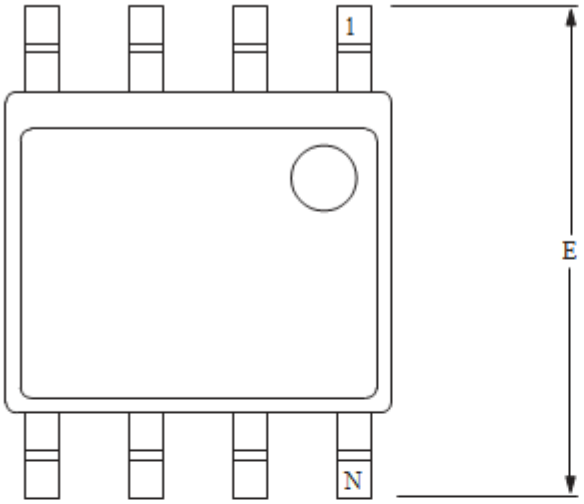


Section B-B

COMMON DIMENSIONS
(Unit of Measure=mm)

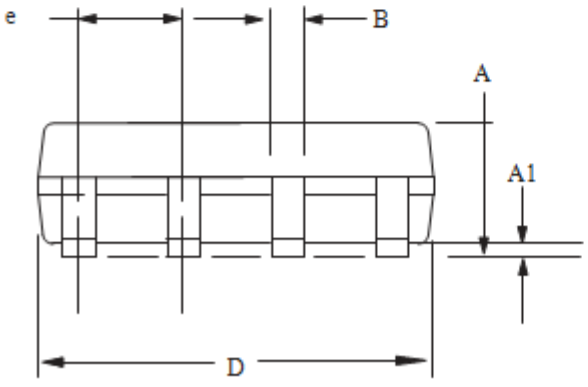
SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

SOP8



Top View

End View



Side View

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
q	0°	8°

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