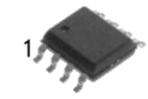
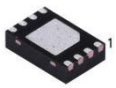
Three-wire Serial EEPROM

Features

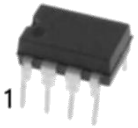
- Three-wire Serial Interface
- Low-voltage and Standard-voltage Operation 1.7V ~ 5.5V
- 2MHz (2.5V) and 1MHz (1.7V) Compatibility
- Dual organization: by word (x16) or byte (x8)
- Sequential read operation
- Programming instructions that work on: byte, word or entire memory
- Self-timed Write Cycle (5 ms max)
- READY/ BUSY signal during programming
- High Reliability
- –Endurance: 1 Million Write Cycles
- –Data Retention: 40 Years
- DIP-8, (RoHS Compliant)
- SOP-8, MSOP-8, DFN-8, SOT-23-6 Packages (RoHS Compliant and Halogen-free)


SOP-8


DFN-8 _2*3


MSOP-8


SOT-23-6


DIP-8

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG93C46AN	DIP-8	93C46A	TUBE	2000pcs/box
HG93C56AN	DIP-8	93C56A	TUBE	2000pcs/box
HG93C66AN	DIP-8	93C66A	TUBE	2000pcs/box
HG93C46AM/TR	SOP-8	93C46A	REEL	2500pcs/Reel
HG93C56AM/TR	SOP-8	93C56A	REEL	2500pcs/Reel
HG93C66AM/TR	SOP-8	93C66A	REEL	2500pcs/Reel
HG93C46AMM/TR	MSOP-8	C46A	REEL	3000pcs/Reel
HG93C56AMM/TR	MSOP-8	C56A	REEL	3000pcs/Reel
HG93C66AMM/TR	MSOP-8	C66A	REEL	3000pcs/Reel
HG93C46ADQ/TR	DFN-8	C46A	REEL	2500pcs/Reel
HG93C56ADQ/TR	DFN-8	C56A	REEL	2500pcs/Reel
HG93C66ADQ/TR	DFN-8	C66A	REEL	2500pcs/Reel
HG93C66AM6/TR	SOT-23-6	C46A	REEL	3000pcs/Reel
HG93C66AM6/TR	SOT-23-6	C56A	REEL	3000pcs/Reel
HG93C66AM6/TR	SOT-23-6	C66A	REEL	3000pcs/Reel

Description

HG93C46A/56A/66A provides 1k/2k/4k bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64/128/256 words of 16 bits each (when the ORG pin is connected to VCC), and 128/256/512 words of 8bits each (when the ORG pin is connected to ground).

The HG93C46A/56A/66A is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Clock (SK). Upon receiving a read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable State. When CS is brought “high” following the initiation of a write cycle, The DO pin outputs the Ready/ Busy status of the part.

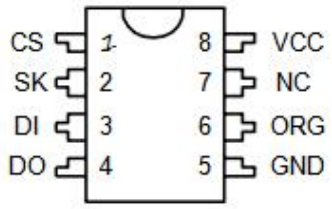
The device is the best choice for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Absolute Maximum Ratings

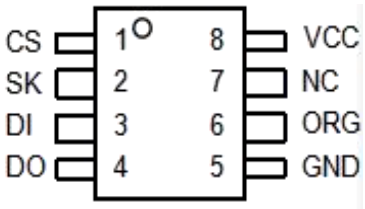
Parameter	Limits
Operating Temperature	-40 °C ~ +85 °C
Storage Temperature	-65 °C ~ +150 °C
Voltage on Any Pin with Respect to Ground	-1.0 V ~ +7.0 V
Maximum Operating Voltage	6.25 V
DC output current	5.0 mA
Lead Temperature (Soldering, 10 seconds)	245°C

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Assignment

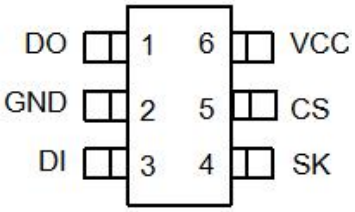


DIP-8

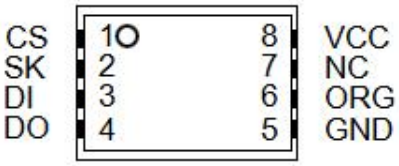


SOP-8

MSOP-8



SOT-23-6

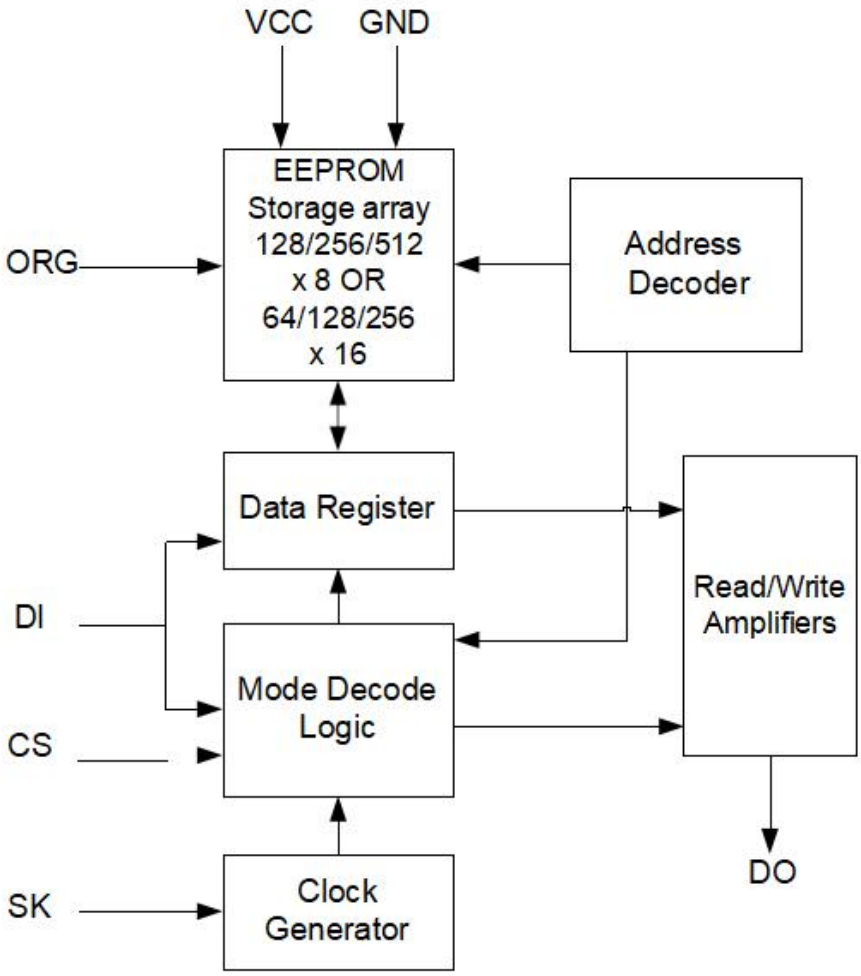


DFN-8

Pin Description

Pin Name	Function
CS	Chip Select
SK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
ORG	Organization Select
NC	No connect
VCC	Power Supply

Figure 1Block Diagram



Memory Organization

The HG93C46A/56A/66A memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to VCC) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (VSS) the x8 organization is selected. When the HG93C46A/56A/66A is in Standby mode, Organization Select (ORG) should be set either to VSS or VCC for minimum power consumption. Any voltage between VSS and VCC applied to Organization Select (ORG) may increase the Standby current.

Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
HG93C66A	4096	512	256
HG93C56A	2048	256	128
HG93C46A	1024	128	64

Instruction Set

The instruction set of the HG93C46A/56A/66A devices contains seven instructions, as summarized in the table below.

- Each instruction is preceded by a rising edge on Chip Select Input (CS) with Serial Clock (SK) being held low.
- A start bit, which is the first „1" read on Serial Data Input (DI) during the rising edge of Serial Clock (SK).
- Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SK). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the HG93C46A, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization. For the HG93C56A and HG93C66A, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization.

Instruction	Device Type	SB	Op Code	Address		Data		Comments
				x8 (1) (2)	x16 (1) (3)	x8	x16	
READ	HG93C46A	1	10	A6-A0 A8-A0	A5-A0 A7-A0			Read Address AN–A0
	HG93C56A	1	10	A8-A0	A7-A0			
	HG93C66A	1	10					
EWEN	HG93C46A	1	00	11XXXXX	11XXXX			Write Enable
	HG93C56A	1	00	11XXXXXXX	11XXXXXX			
	HG93C66A	1	00	11XXXXXXX	11XXXXXX			
ERASE	HG93C46A	1	11	A6-A0	A5-A0			Clear Address AN–A0
	HG93C56A	1	11	A8-A0 A8-A0	A7-A0 A7-A0			
	HG93C66A	1	11					
WRITE	HG93C46A	1	01	A6-A0 A8-A0	A5-A0 A7-A0	D7-D0	D15-D0	Write Address AN–A0
	HG93C56A	1	01	A8-A0	A7-A0	D7-D0	D15-D0	
	HG93C66A	1	01			D7-D0	D15-D0	
ERAL	HG93C46A	1	00	10XXXXX	10XXXX			Clear All Addresses
	HG93C56A	1	00	10XXXXXXX	10XXXXXX			
	HG93C66A	1	00	10XXXXXXX	10XXXXXX			
WRAL	HG93C46A	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses
	HG93C56A	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0	
	HG93C66A	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0	
EWDS	HG93C46A	1	00	00XXXXX	00XXXX			Write Disable
	HG93C56A	1	00	00XXXXXXX	00XXXXXX			
	HG93C66A	1	00	00XXXXXXX	00XXXXXX			

Note:

1. X = Don't Care bit.
2. Address bit A8 is not decoded by the HG93C56A.
3. Address bit A7 is not decoded by the HG93C56A.

Functional Description

The HG93C46A/56A/66A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic “1”) followed by the appropriate op code and the desired memory address location.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock (SK).. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/ Busy status cannot be obtained if the CS is brought high after the end of the selftimed programming cycle, t_{WP}.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at Vcc = 2.5V ~5.5V

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/ Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at Vcc = 2.5V ~5.5V.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

READY/ BUSY status: While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (DO=0) is returned whenever Chip Select input (CS) is driven high. (Please note, though, that there is an initial delay, of tCS, before this status information becomes available). In this state, the HG93C46A/56A/66A ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (CS) is driven high, the Ready signal (DO=1) indicates that the HG93C46A/56A/66A is ready to receive the next instruction. Serial Data Output (DO) remains set to 1 until the Chip Select Input (CS) is brought low or until a new start bit is decoded.

Timing Diagrams

Figure 2 READ Timing

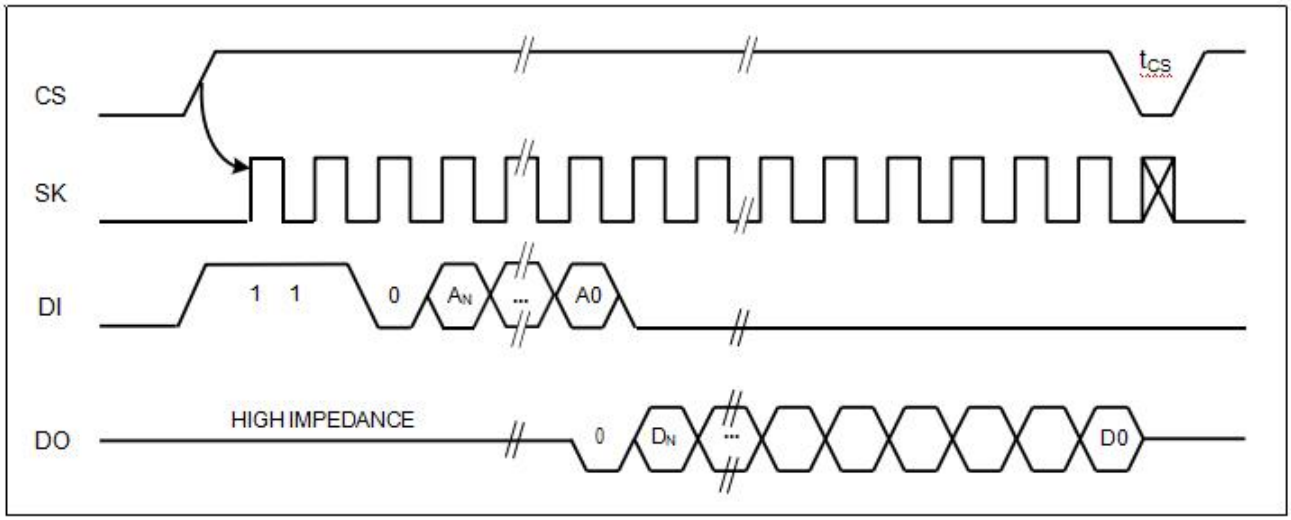


Figure 3 EWEN Timing

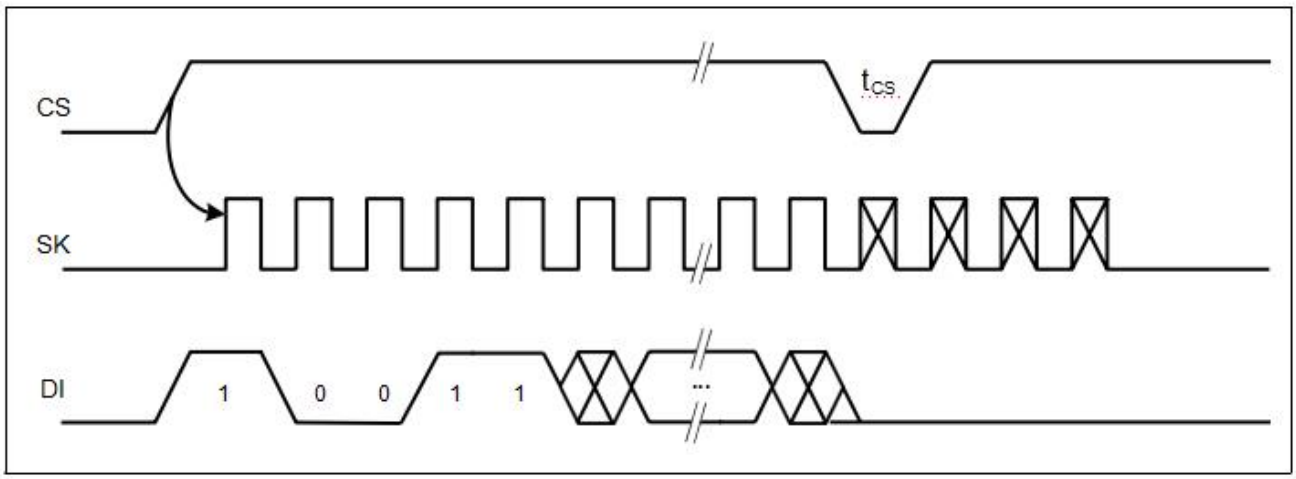


Figure 4 ERASE Timing

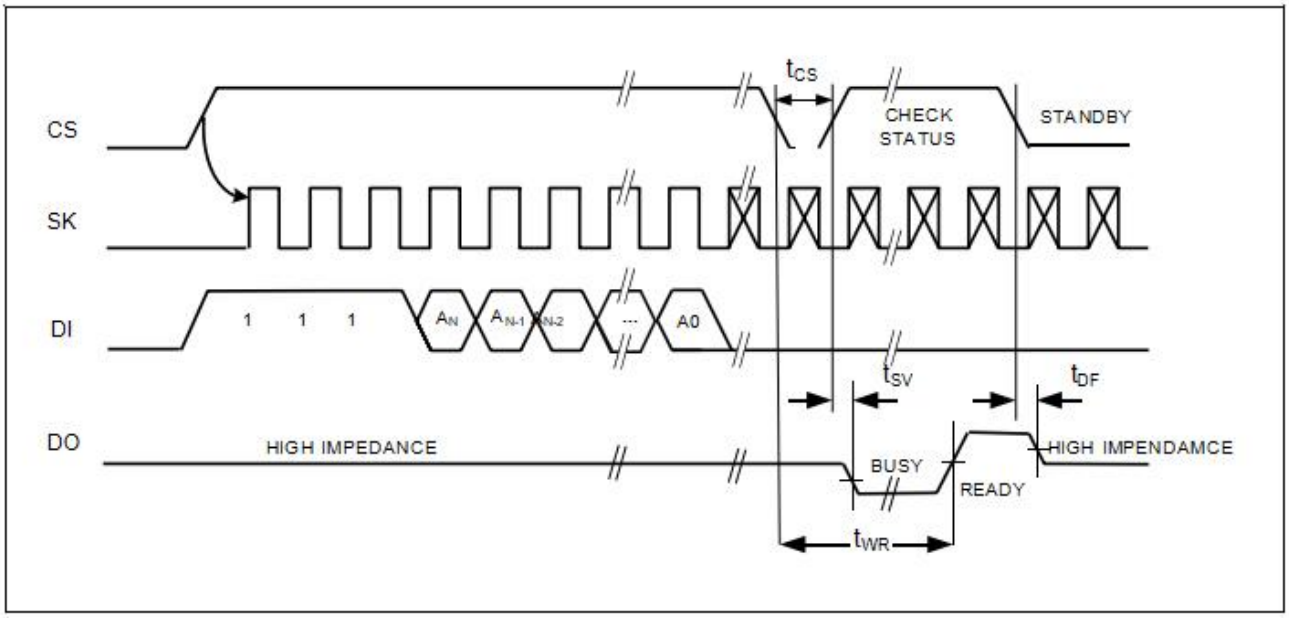


Figure 5 WRITE Timing

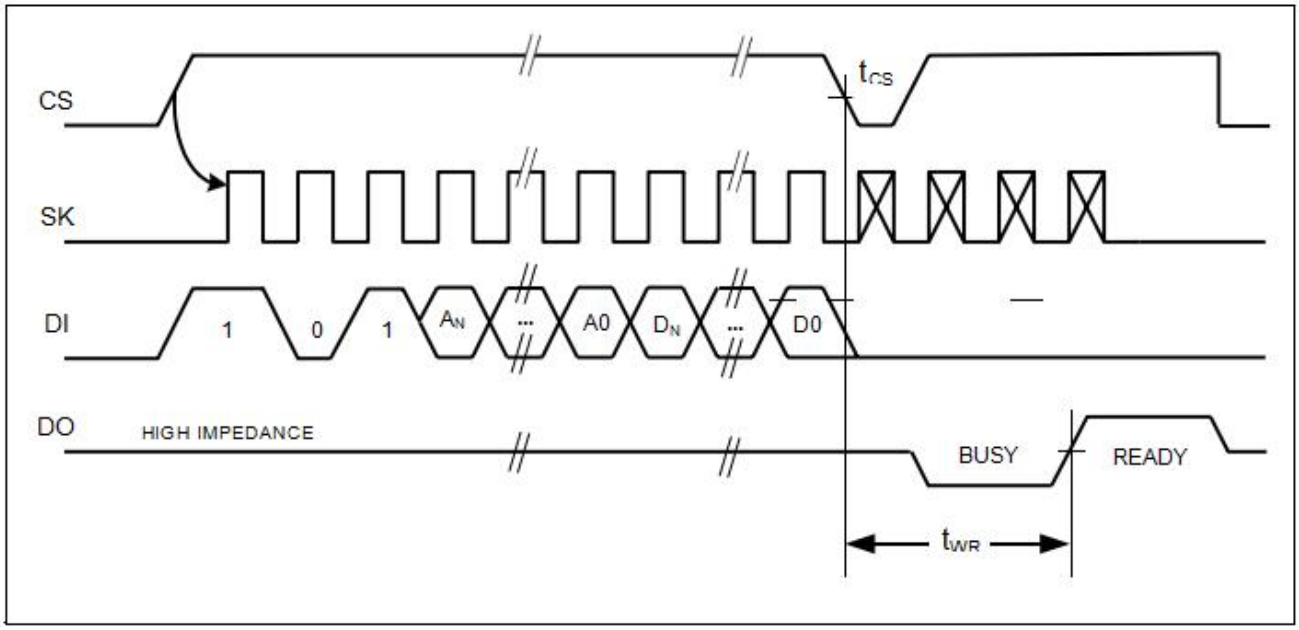


Figure 6 ERAL Timing

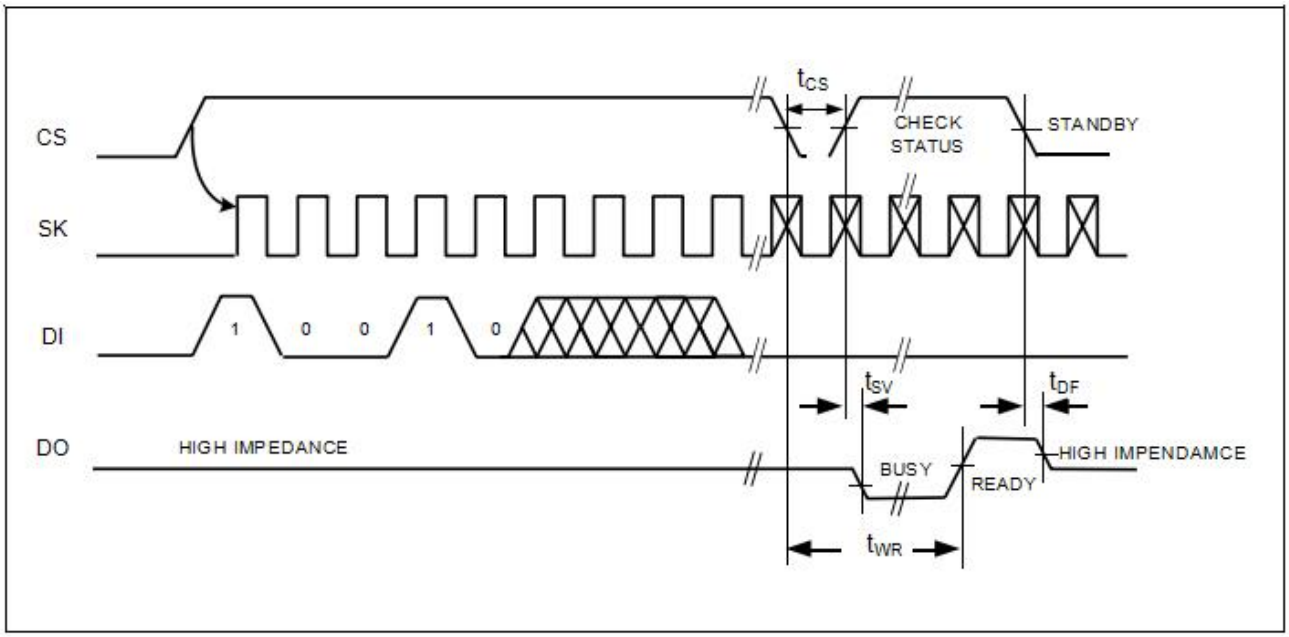


Figure 7 WRAL Timing

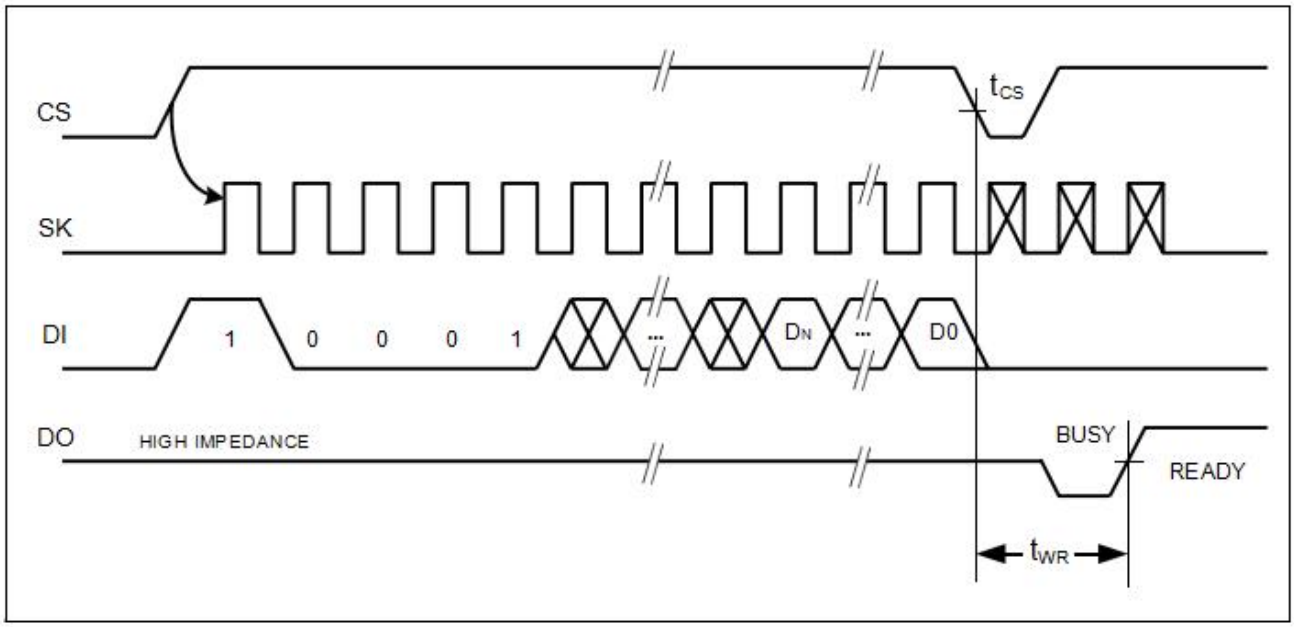


Figure 8 EWDS Timing

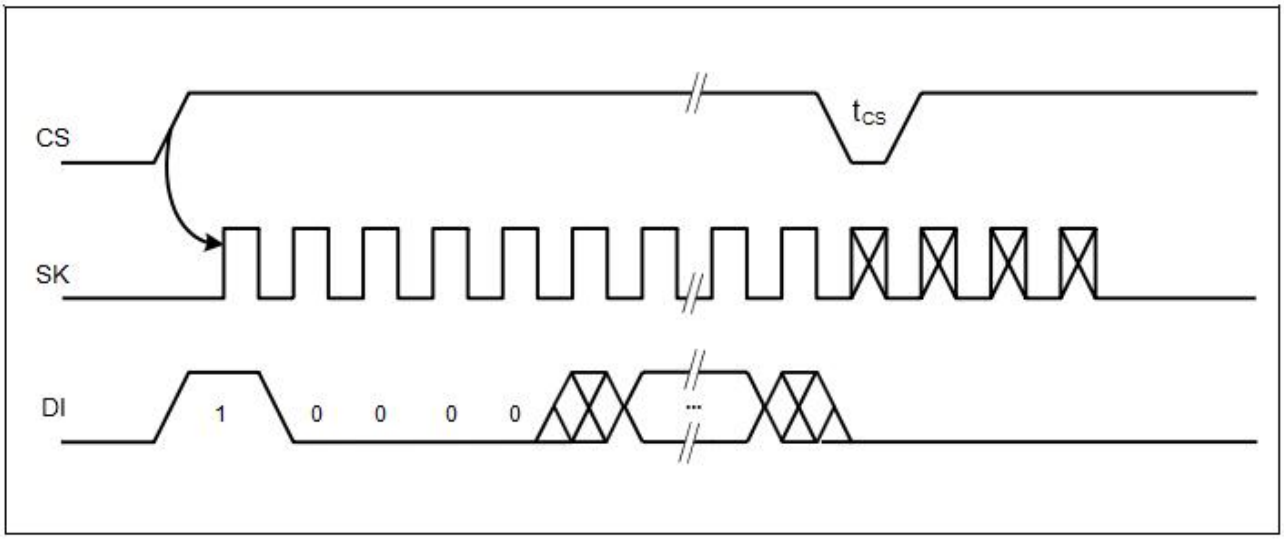
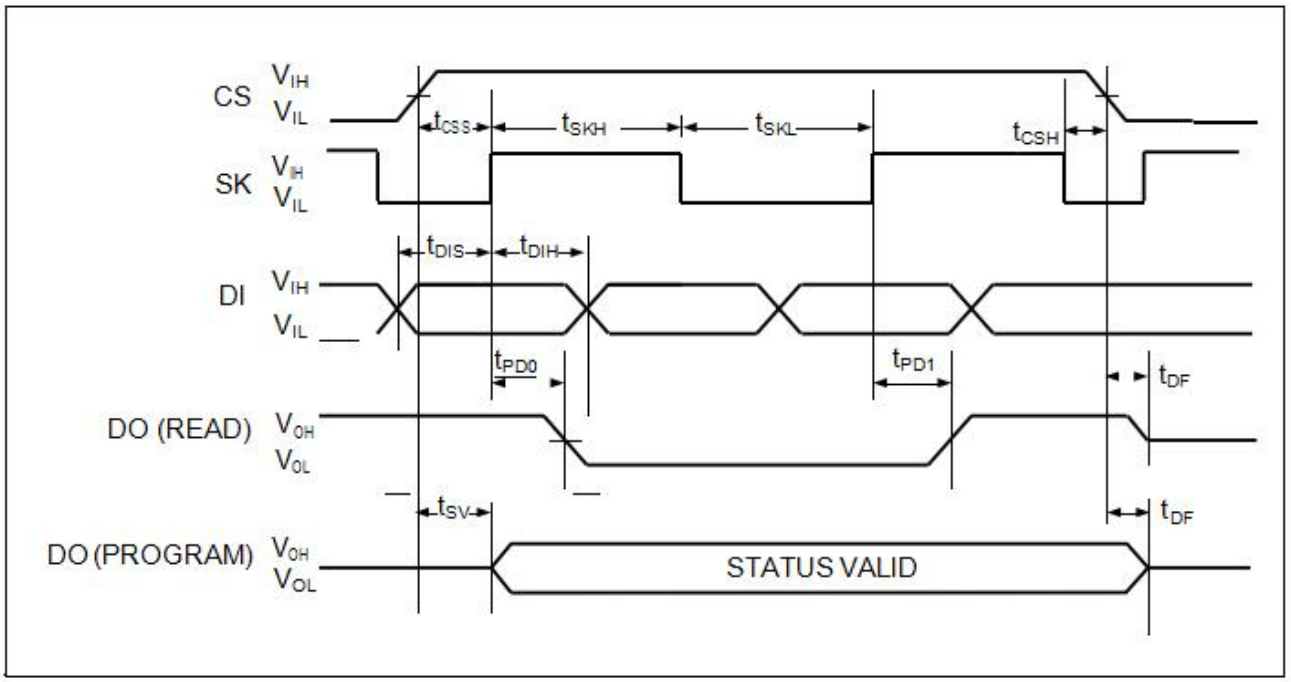


Figure 9 BUS Timing



Pin Capacitance

Symbol	Parameter	Test Condition	Max	Units
CIN (1)	Input Capacitance	VIN = 0V, f = 1 MHz	6	pF
COUT (1)	Output Capacitance	VOUT = 0V, f = 1 MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Max	Units
VCC	Supply Voltage			1.7	5.5	V
ICC	Supply	VCC = 5.0V, fsk = 2.0 MHz	CS = VIH, DO =open		2.0	mA
		VCC = 1.7V, fsk = 1.0 MHz			1.0	mA
ISB	Standby Current	VCC=5V	CS = SK = GND, ORG = VCC/GND		15.0	μA
		VCC = 1.7V			2.0	μA
ILI	Input Leakage	0V ≤ VIN ≤ Vcc		-1.0	1.0	μA
ILO	Output Leakage	0V ≤ VOUT ≤ Vcc ; DO = Hi-Z		-1.0	1.0	μA
VIL (1)	Input Low Voltage			-0.45	0.2Vcc	V
VIH (1)	Input High Voltage			0.8VCC	VCC+0.5	V
VOL	Output Low Voltage	VCC = 5V	IOL = 2.1 mA		0.4	V
		VCC = 1.7V	IOL = 100 μA		0.2	V
VOH	Output High Voltage	VCC = 5V	IOH = -400 μA	0.8Vcc		V
		VCC = 1.7V	IOH = -100 μA	VCC-0.2		V

Note: 1. VIL min and VIH max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC = 1.7V to 5.5V, CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V ≤ Vcc ≤ 2.5V		2.5V < Vcc ≤ 5.5V		Units
		Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		1		2	MHz
t_{SKL}	SK Low Time	250		200		ns
t_{SKH}	SK High Time	250		200		ns
t_{CS}	Minimum CS Low	250		200		ns
t_{CSS}	CS Setup Time	50		50		ns
t_{CSH}	CS Hold Time	0		0		ns
t_{DIS}	DI Setup Time	100		50		ns
t_{DIH}	DI Hold Time	100		50		ns
t_{PD1}	Output Delay to “1”		400		200	ns
t_{PD0}	Output Delay to “0”		400		200	ns
t_{SV}	CS to Status Valid		400		200	ns
t_{DF}	CS to DO in High		200		100	ns
t_{WR}	Write Cycle		5		5	ms
Endurance (1)	3.3V, 25°C	1,000,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

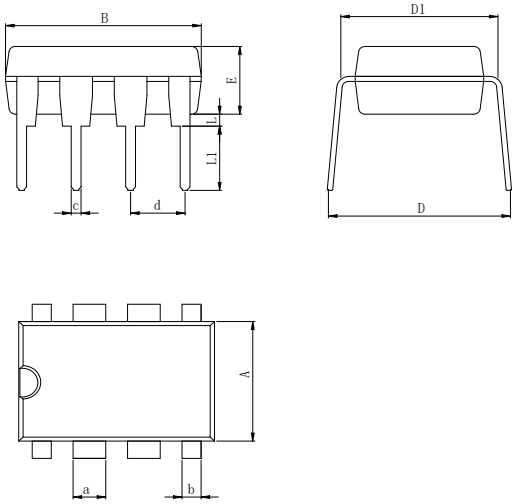
2. AC measurement conditions:

Input pulse voltages: 0.2 V_{CC} to 0.8 V_{CC} Input rise and fall times: ≤ 50ns

Input and output timing reference voltages: 0.3 V_{CC} ~ 0.7 V_{CC}

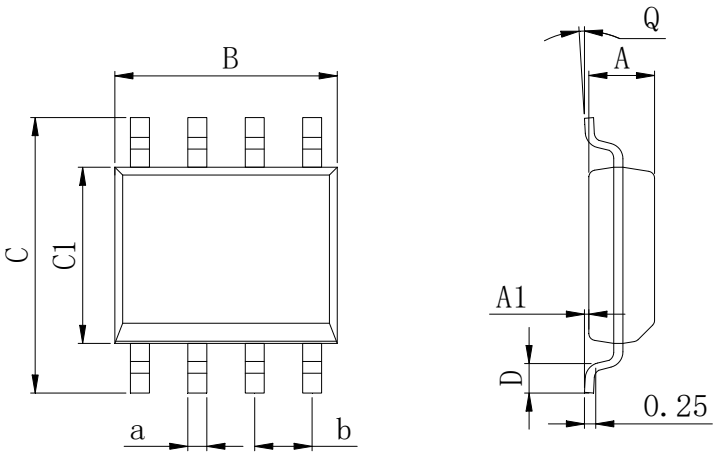
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

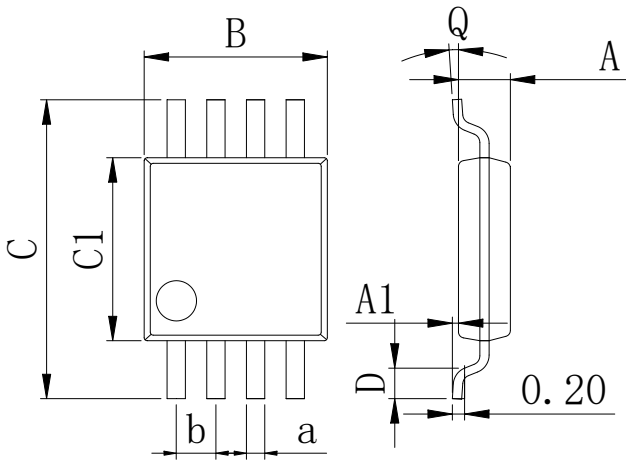
SOP-8 (150mil)



Dimensions In Millimeters(SOP8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

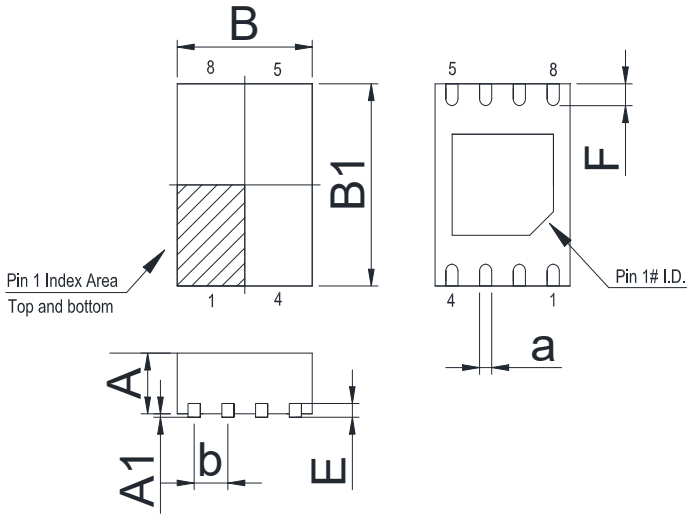
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

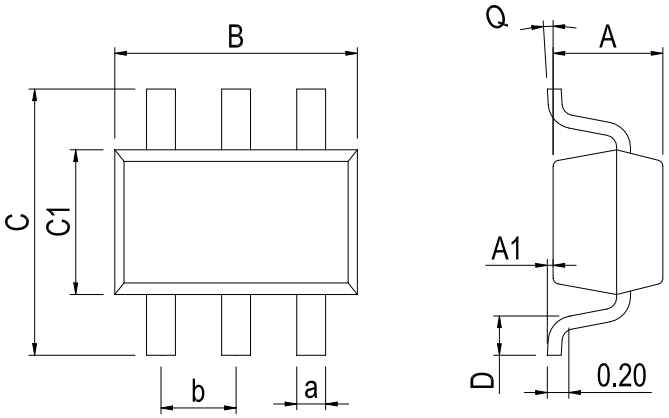
DFN-8 2*3



Dimensions In Millimeters(DFN-8 2*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	1.90	2.90	0.15	0.25	0.20	0.50TYP
Max:	0.95	0.05	2.10	3.10	0.25	0.35	0.30	

Physical Dimensions

SOT-23-6



Dimensions In Millimeters(SOT-23-6)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.05	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.40	

Revision History

DATE	REVISION	PAGE
2020-3-16	New	1-17
2023-8-30	Update encapsulation type、Update Lead Temperature、Updated DIP-8 dimension	1、2、13

IMPORTANT STATEMENT:

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