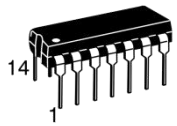
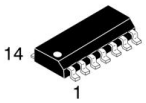
Quadruple 2-Input NAND Gates with Open-Drain Outputs

Features

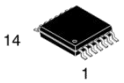
- Wide Operating Voltage Range: 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Maximum ICC
- Typical tpd = 8 ns at 5 V
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA



DIP-14



SOP-14



TSSOP-14

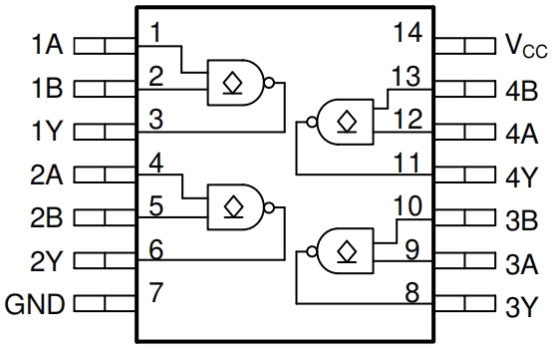
Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC03N	DIP-14	74HC03	TUBE	1000pcs/Box
74HC03M/TR	SOP-14	74HC03	REEL	2500pcs/Reel
74HC03MT/TR	TSSOP-14	HC03	REEL	2500pcs/Reel

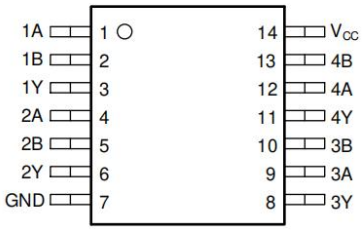
Description

This device contains four independent 2-input NAND Gates with open-drain outputs. Each gate performs the Boolean function Y = A ● B in positive logic

Functional pinout



Pin Configuration



DIP-14/SOP-14/TSSOP-14

Pin Functions

PIN		I/O	DESCRIPTION
NAME	DIP/SOP/TSSOP		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
VCC	14	—	Positive Supply

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VCC	Supply voltage		–0.5	7	V
IIK	Input clamp current(2)	VI < 0 or VI > VCC	-	±20	mA
IOK	Output clamp current(2)	VO < 0 or VO > VCC	-	±20	mA
IO	Continuous output current	VO = 0 to VCC	-	±25	mA
	Continuous current through VCC or GND		-	±50	mA
TJ	Junction temperature(3)		-	150	°C
Tstg	Storage temperature		–65	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)		-	245	°C

1. Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. Guaranteed by design.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	V
VIH	High-level input voltage	VCC = 2 V	1.5			V
		VCC = 4.5 V	3.15			
		VCC = 6 V	4.2			
VIL	Low-level input voltage	VCC = 2 V			0.5	V
		VCC = 4.5 V			1.35	
		VCC = 6 V			1.8	
VI	Input voltage		0		VCC	V
VO	Output voltage		0		VCC	V
Δt/Δv	Input transition rise and fall rate	VCC = 2 V			1000	ns
		VCC = 4.5 V			500	
		VCC = 6 V			400	
TA	Operating free-air temperature	74HC03	–40		85	°C

Thermal Information

THERMAL METRIC(1)		74HC03 (SOP) 14 PINS	74HC03 (DIP) 14 PINS	74HC03 (TSSOP) 14 PINS	UNIT
RθJA	Junction-to-ambient thermal resistance	133.6	66.0	151.7	°C/W
RθJC(top)	Junction-to-case (top) thermal resistance	89	53.7	79.4	°C/W
RθJB	Junction-to-board thermal resistance	89.5	45.7	94.7	°C/W
ΨJT	Junction-to-top characterization parameter	45.5	33.3	25.2	°C/W
ΨJB	Junction-to-board characterization parameter	89.1	45.5	94.1	°C/W
RθJC(bot)	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		VCC	Operating free-air temperature (TA) 25°C MIN	25°C TYP	25°C MAX	-40°C to 85°C MIN	-40°C to 85°C TYP	-40°C to 85°C MAX	UNIT
IOH	Output voltage	VI = VIH or VIL	VO = VCC	6 V		0.01	0.5			5	μA
VOL	Low-level output voltage	VI = VIH or VIL	IOL = 20 μA	2 V		0.002	0.1			0.1	V
				4.5 V		0.001	0.1			0.1	
				6 V		0.001	0.1			0.1	
			IOL = 4 mA	4.5 V		0.17	0.26			0.33	
			IOL = 5.2 mA	6 V		0.15	0.26			0.33	
II	Input leakage current	VI = VCC or 0		6 V			±0.1			±1	μA
ICC	Supply current	VI = VCC or 0	IO = 0	6 V			2			20	μA
Ci	Input capacitance			2 V to 6 V		3	10			10	pF

(1) VCCI is the VCC associated with the input port.

(2) VCCO is the VCC associated with the output port.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	VCC	Operating free-air temperature (TA)						UNIT
					25°C			–40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
tplh	Propagation delay, low-to-high	A or B	Y	2 V		60	105			131	ns
				4.5 V		13	25			31	
				6 V		10	23			27	
tphl	Propagation delay high-to-low	A or B	Y	2 V		50	100			125	ns
				4.5 V		10	20			25	
				6 V		8	17			21	
tt	Transition-time		Y	2 V		38	75			95	ns
				4.5 V		8	15			19	
				6 V		6	13			16	

Operating Characteristics

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
Cpd	Power dissipation capacitance per gate	No load	2 V to 6 V		20		pF

Typical Characteristics(TA = 25°C)

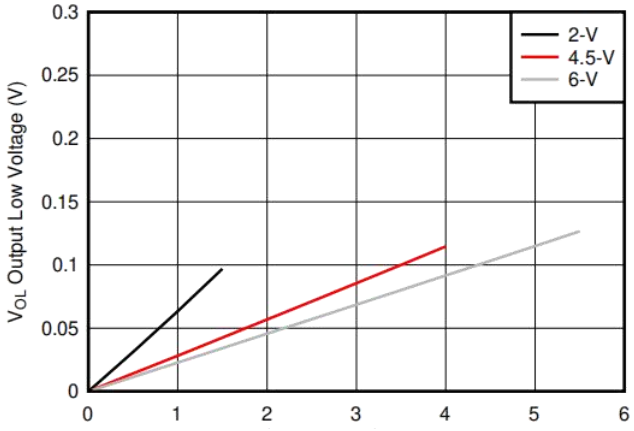
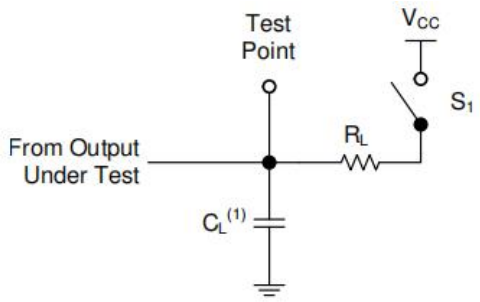


Figure 5-1. Typical output voltage in the low state (VOL)

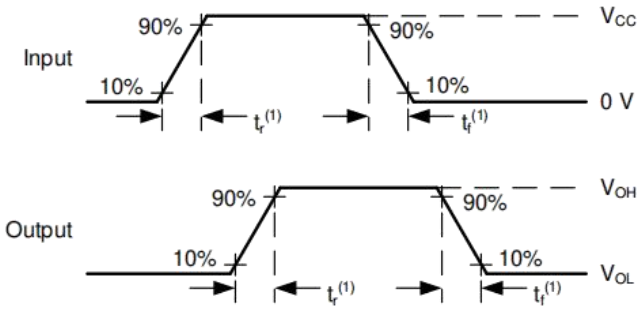
Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω, tt < 6 ns.
The outputs are measured one at a time, with one input transition per measurement



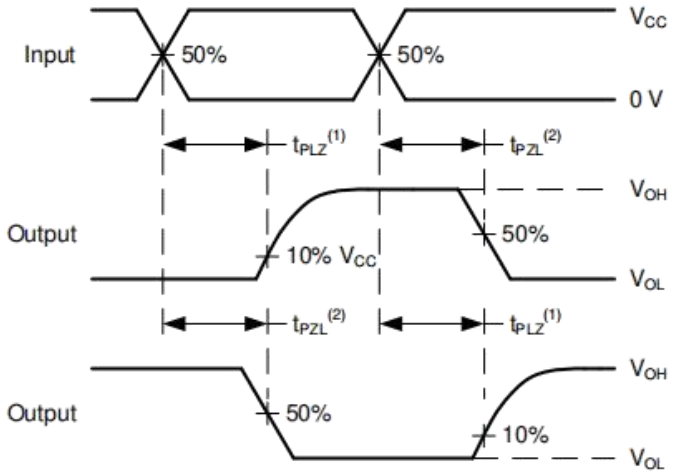
A. CL= 50 pF and includes probe and jig capacitance

Figure 6-1. Load Circuit



A. tt is the greater of tr and tf.

Figure 6-2. Voltage Wave forms Transition Times



A. The maximum between tPLH and tPHL is used for tpd.

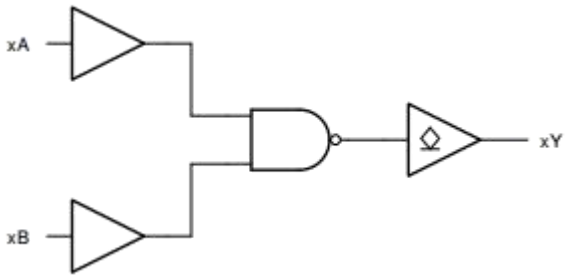
Figure 6-3. Voltage Wave forms Propagation Delays

Detailed Description

Overview

This device contains four independent 2-input NAND gates with open-drain outputs. Each gate performs the Boolean function Y = A ● B in positive logic.

Functional Block Diagram



Feature Description

CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from VCC. When the output is not actively pulling the line low, it will go into a high impedance state. This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pull-up resistor.

The current drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the Absolute Maximum Ratingsmust be followed at all times.

The 74HC03 can drive a load with a total capacitance less than or equal to the maximum load listed in the Switching Characteristics connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the Absolute Maximum Ratings.

Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the Electrical Characteristics, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the Recommended Operating Conditions to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Sch mitt -trigger input should be used to condition the input signal prior to the standard CMOS input.

Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

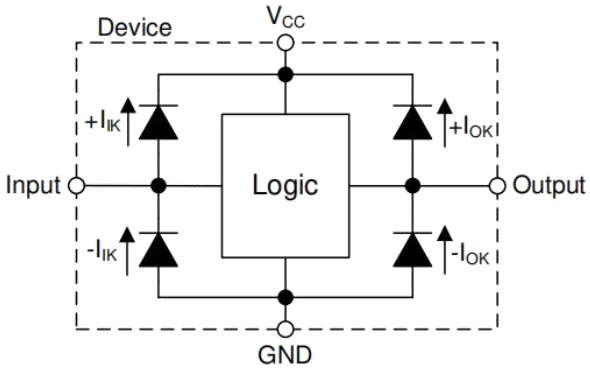


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

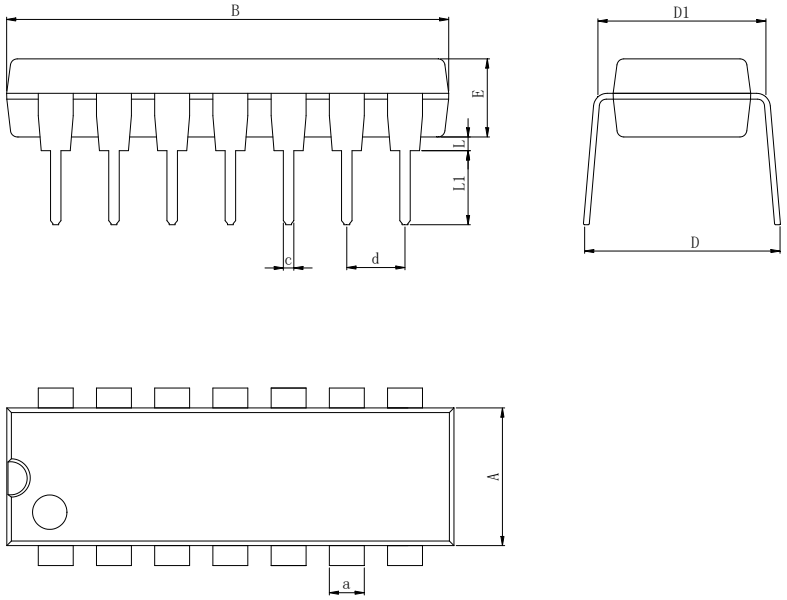
Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	Z
X	L	Z

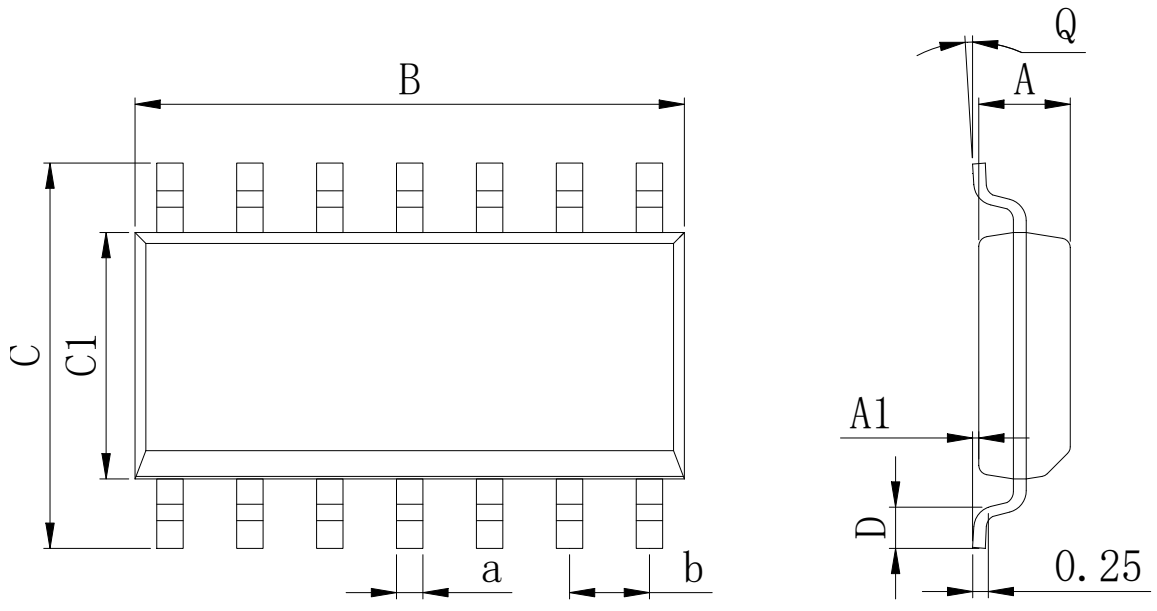
Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

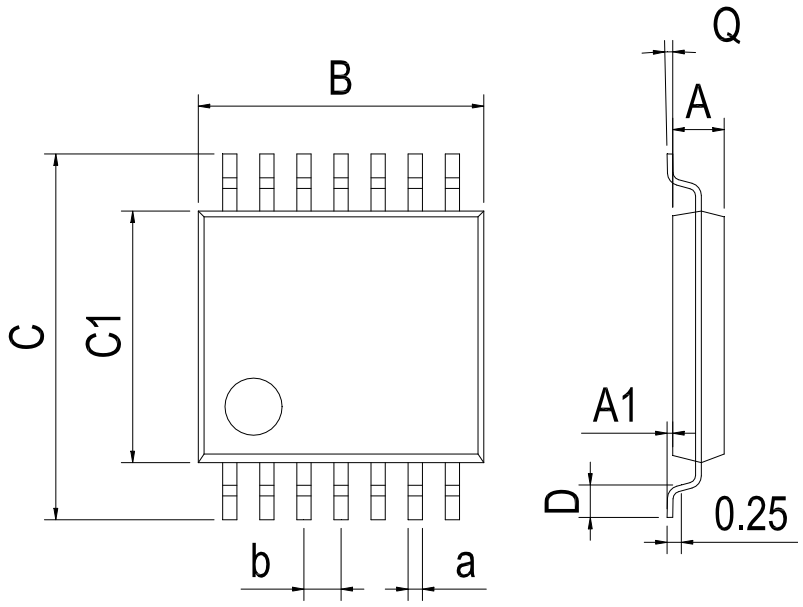
SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2020-3-8	New	1-12
2023-8-31	Update encapsulation type、Update Lead Temperature、Updated DIP-14 dimension	1、3、9

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