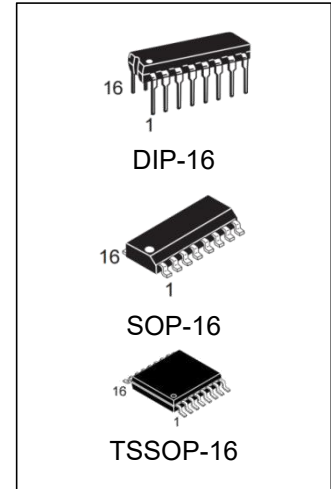


Micro power Phase-Locked Loop

Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic: 70 μ W (typ.) at
power consumption: $f_o = 10$ kHz, $V_{DD} = 5$ V
- VCO frequency: 1.3 MHz (typ.) at $V_{DD} = 10$ V
- Low frequency drift: 0.06%/°C at $V_{DD} = 10$ V with temperature
- High VCO linearity: 1% (typ.)



Ordering Information

| DEVICE | Package Type | MARKING | Packing | Packing Qty |
|-----------------------|--------------|---------|---------|--------------|
| CD4046BE/ CD4046BN | DIP-16 | CD4046B | TUBE | 1000pcs/box |
| CD4046BM/TR | SOP-16 | CD4046B | REEL | 2500pcs/reel |
| CD4046BMT/TR | TSSOP-16 | CD4046B | REEL | 2500pcs/reel |

General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal. Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency. Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin C1_A, C1_B, R1 and R2. The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more. The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

Block & Connection Diagrams

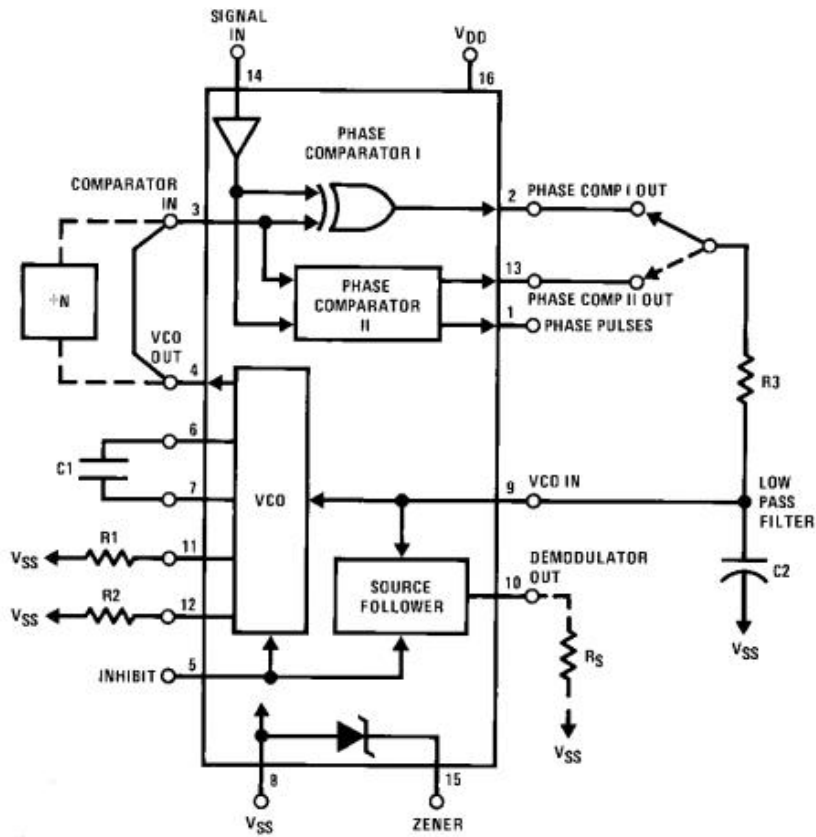
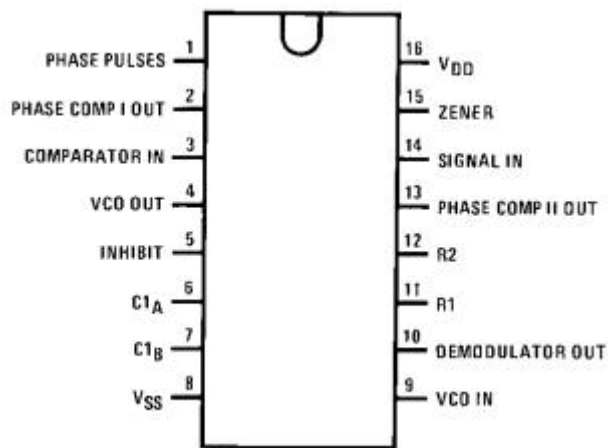


FIGURE 1

Dual-In-Line Package



Top View

Order Number CD4046B

Absolute Maximum Ratings (Notes 1 & 2)

| Condition | Min | Max | UNITS |
|---------------------------------------------------|------|------|-------|
| DC Supply Voltage (V_{DD}) | -0.5 | +18 | V |
| Input Voltage (V_{IN}) | -0.5 | +0.5 | V |
| Storage Temperature Range (T_S) | -65 | 150 | °C |
| Power Dissipation (P_D) | - | - | - |
| Dual-In-Line | - | 700 | mW |
| Small Outline | - | 500 | mW |
| Lead Temperature (T_L)(Soldering, 10 seconds) | - | 245 | °C |

Recommended Operating Conditions (Note 2)

| Condition | Min | Max | UNITS |
|---------------------------------------|---------------|-----|-------|
| DC Supply Voltage (V_{DD}) | +3 | +15 | V |
| Input Voltage (V_{IN}) | 0 to V_{DD} | | V |
| Operating Temperature Range (T_A) | -40 | +85 | °C |

DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Conditions | -40°C | | +25°C | | | +85°C | | Units |
|-----------------|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|-------------------|------|-------|------|-------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I _{DD} | Quiescent Device Current | Pin 5 = V _{DD} , Pin 14 = V _{DD} , Pin 3, 9 = V _{SS} V _{DD} = 5V | | 20 | | 0.005 | 20 | | 150 | μA |
| | | V _{DD} = 10V | | 40 | | 0.01 | 40 | | 300 | μA |
| | | V _{DD} = 15V | | 80 | | 0.015 | 80 | | 600 | μA |
| | | Pin 5 = V _{DD} , Pin 14 = Open, Pin 3, 9 = V _{SS} V _{DD} = 5V | | 70 | | 5 | 55 | | 205 | μA |
| | | V _{DD} = 10V | | 530 | | 20 | 410 | | 710 | μA |
| | | V _{DD} = 15V | | 1500 | | 50 | 1200 | | 1800 | μA |
| V _{OL} | Low Level Output Voltage | V _{DD} = 5V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | V _{DD} = 10V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | V _{DD} = 15V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| V _{OH} | High Level Output Voltage | V _{DD} = 5V | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | V _{DD} = 10V | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | V _{DD} = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| V _{IL} | Low Level Input Voltage Comparator and Signal In | V _{DD} = 5V, V _O = 0.5V or 4.5V | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | V _{DD} = 10V, V _O = 1V or 9V | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | V _{DD} = 15V, V _O = 1.5V or 13.5V | | 4.0 | | 6.25 | 4.0 | | 4.0 | V |
| V _{IH} | High Level Input Voltage Comparator and Signal In | V _{DD} = 5V, V _O = 0.5V or 4.5V | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | V _{DD} = 10V, V _O = 1V or 9V | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | V _{DD} = 15V, V _O = 1.5V or 13.5V | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| I _{OL} | Low Level Output Current (Note 4) | V _{DD} = 5V, V _O = 0.4V | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | V _{DD} = 10V, V _O = 0.5V | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | V _{DD} = 15V, V _O = 1.5V | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| I _{OH} | High Level Output Current (Note 4) | V _{DD} = 5V, V _O = 4.6V | -0.52 | | -0.44 | -0.88 | | -0.36 | | mA |
| | | V _{DD} = 10V, V _O = 9.5V | -1.3 | | -1.1 | -2.25 | | -0.9 | | mA |
| | | V _{DD} = 15V, V _O = 13.5V | -3.6 | | -3.0 | -8.8 | | -2.4 | | mA |
| I _{IN} | Input Current | All Inputs Except Signal Input V _{DD} = 15V, V _{IN} = 0V | | -0.3 | | -10 ⁻⁵ | -0.3 | | -1.0 | μA |
| | | V _{DD} = 15V, V _{IN} = 15V | | 0.3 | | 10 ⁻⁵ | 0.3 | | 1.0 | μA |
| C _{IN} | Input Capacitance | Any Input (Note 3) | | | | | 7.5 | | | pF |
| P _T | Total Power Dissipation | f _o = 10 kHz, R ₁ = 1 MΩ R ₂ = ∞, V _{COIN} = V _{DD} /2 V _{DD} = 5V | | | | 0.07 | | | | mW |
| | | V _{DD} = 10V | | | | 0.6 | | | | mW |
| | | V _{DD} = 15V | | | | 2.4 | | | | mW |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* TA = 25°C, CL = 50 pF

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------------|-------------|----------------|
| VCO SECTION | | | | | | |
| I _{DD} | Operating Current | fo = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO _{IN} = V _{DD} /2 V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V | | 20 90 200 | | μA μA μA |
| f _{MAX} | Maximum Operating Frequency | C1 = 50 pF, R1 = 10 kΩ, R2 = ∞, VCO _{IN} = V _{DD} V _{DD} = 5V | 0.4 | 0.8 | | MHz |
| | | V _{DD} = 10V | 0.6 | 1.2 | | MHz |
| | | V _{DD} = 15V | 1.0 | 1.6 | | MHz |
| | Linearity | VCO _{IN} = 2.5V ± 0.3V, R1 ≥ 10 kΩ, V _{DD} = 5V VCO _{IN} = 5V ± 2.5V, R1 ≥ 400 kΩ, V _{DD} = 10V VCO _{IN} = 7.5V ± 5V, R1 ≥ 1 MΩ, V _{DD} = 15V | | | 1 1 1 | |
| Temperature-Frequency Stability No Frequency Offset, f _{MIN} = 0 | | %/°C ∞ 1/f. V _{DD} R2 = ∞ V _{DD} = 5V | | | 0.12 - 0.24 | %/°C |
| | | V _{DD} = 10V | | | 0.04 - 0.08 | %/°C |
| | V _{DD} = 15V | | | 0.015 - 0.03 | %/°C | |
| Frequency Offset, f _{MIN} ≠ 0 | V _{DD} = 5V | | | 0.06 - 0.12 | | %/°C |
| | V _{DD} = 10V | | | 0.05 - 0.1 | | %/°C |
| | V _{DD} = 15V | | | 0.03 - 0.06 | | %/°C |
| VCO _{IN} | Input Resistance | V _{DD} = 5V | | 10 ⁶ | | MΩ |
| | | V _{DD} = 10V | | 10 ⁶ | | MΩ |
| | | V _{DD} = 15V | | 10 ⁶ | | MΩ |
| VCO | Output Duty Cycle | V _{DD} = 5V | | 50 | | % |
| | | V _{DD} = 10V | | 50 | | % |
| | | V _{DD} = 15V | | 50 | | % |
| t _{THL} t _{THL} | VCO Output Transition Time | V _{DD} = 5V | | 90 | 200 | ns |
| | | V _{DD} = 10V | | 50 | 100 | ns |
| | | V _{DD} = 15V | | 45 | 80 | ns |

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* TA e 25°C, CL = 50 pF (Continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|------------------------------------------------|-----------------------------------------------------|----------------------------------------------------|-----|------|------|-------|----|
| PHASE COMPARATORS SECTION | | | | | | | |
| R _{IN} | Input Resistance Signal Input | V _{DD} = 5V | 1 | 3 | | MΩ | |
| | | V _{DD} = 10V | 0.2 | 0.7 | | MΩ | |
| | | V _{DD} = 15V | 0.1 | 0.3 | | MΩ | |
| | Comparator Input | V _{DD} = 5V | | | 106 | | MΩ |
| | | V _{DD} = 10V | | | 106 | | MΩ |
| | | V _{DD} = 15V | | | 106 | | MΩ |
| AC-Coupled Signal Input Voltage Sensitivity | C _{SERIES} = 1000 pF f = 50 kHz | | | | | | |
| | V _{DD} = 5V | | | 200 | 400 | mV | |
| | V _{DD} = 10V | | | 400 | 800 | mV | |
| | | V _{DD} = 15V | | 700 | 1400 | mV | |
| DEMODULATOR OUTPUT | | | | | | | |
| V _{COIN} - V _{DEM} | Offset Voltage | RS ≥ 10 kΩ, V _{DD} = 5V | | 1.50 | 2.2 | V | |
| | | RS ≥ 10 kΩ, V _{DD} = 10V | | 1.50 | 2.2 | V | |
| | | RS ≥ 50 kΩ, V _{DD} = 15V | | 1.50 | 2.2 | V | |
| Linearity | RS ≥ 50 kΩ | | | | | | |
| | V _{COIN} = 2.5V±0.3V, V _{DD} = 5V | | | 0.1 | | % | |
| | V _{COIN} = 5V±2.5V, V _{DD} = 10V | | | 0.6 | | % | |
| | | V _{COIN} = 7.5V±5V, V _{DD} = 15V | | 0.8 | | % | |
| ZENER DIODE | | | | | | | |
| V _Z | Zener Diode Voltage | I _Z = 50 μA | 6.3 | 7.0 | 7.7 | V | |
| R _Z | Zener Dynamic Resistance | I _Z = 1 mA | | 100 | | Ω | |

*AC Parameters are guaranteed by DC correlated testing.

Phase Comparator State Diagrams

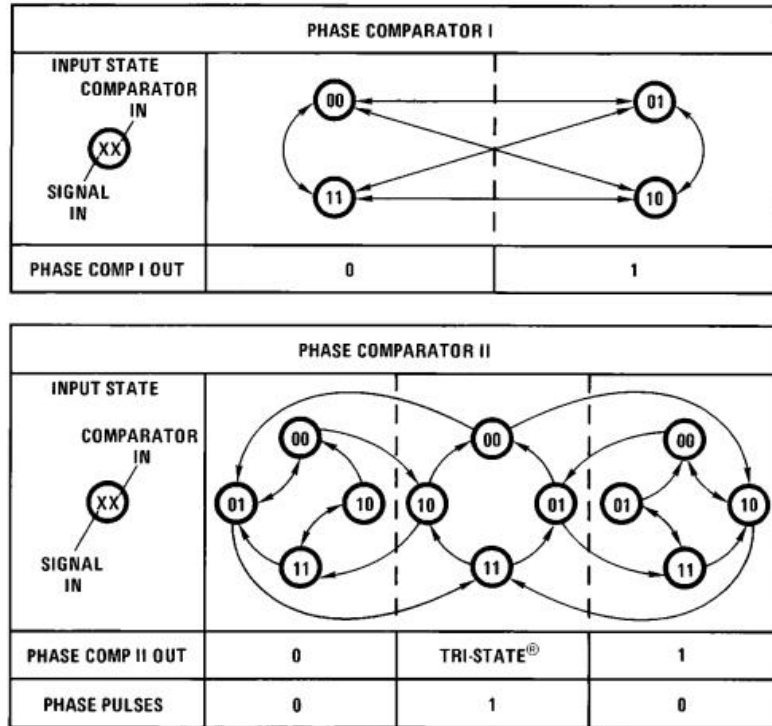


FIGURE 2

Typical Waveforms

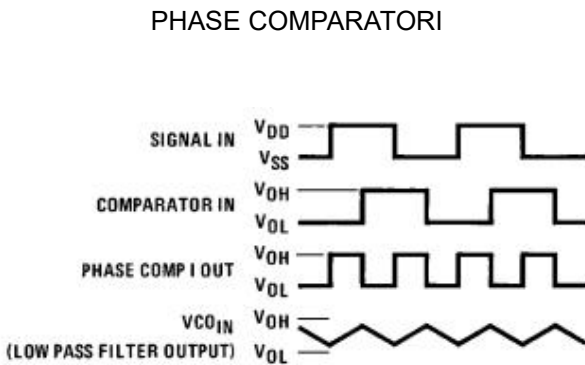


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

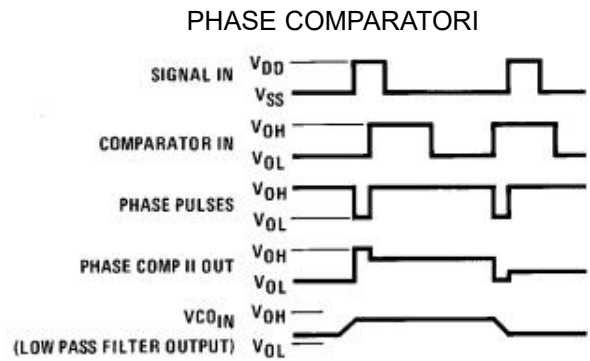


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

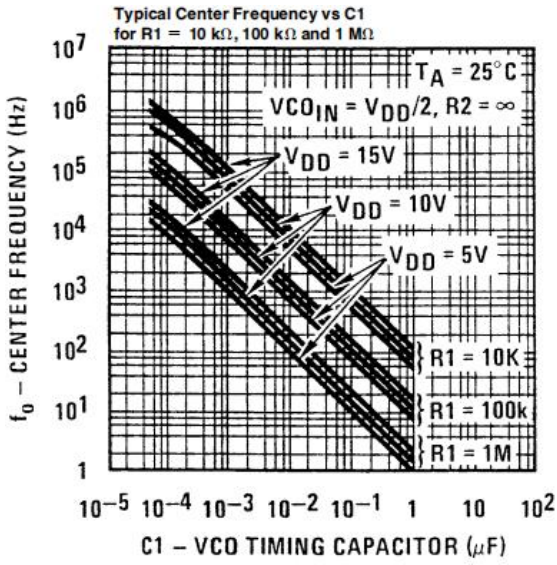


FIGURE 5a

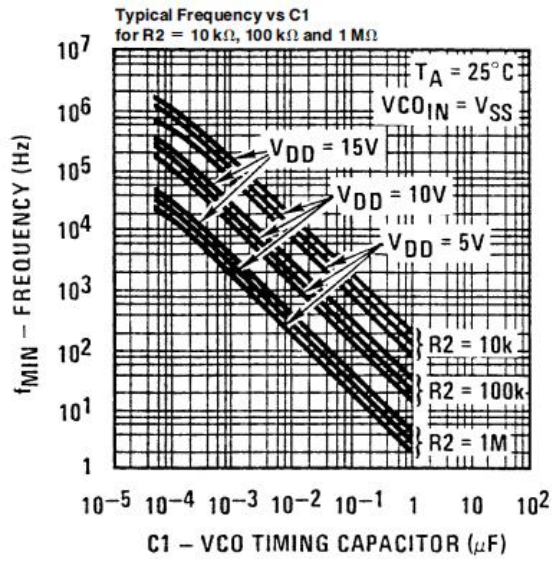


FIGURE 5b

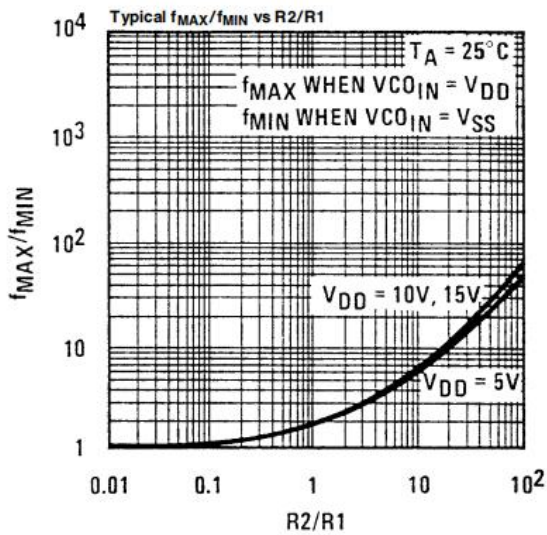


FIGURE 5c

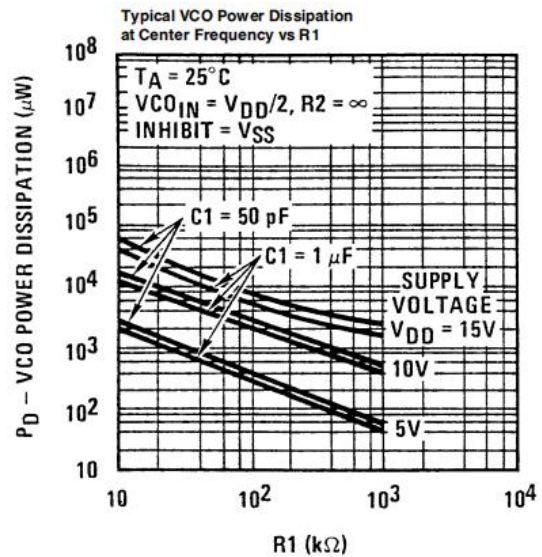


FIGURE 6a

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, $PD(Total) - PD(f_0) + PD(f_{MIN}) + PD(RS)$; Phas - Comparator II, $PD(Total) - PD(f_{MIN})$.

Typical Performance Characteristics (Continued)

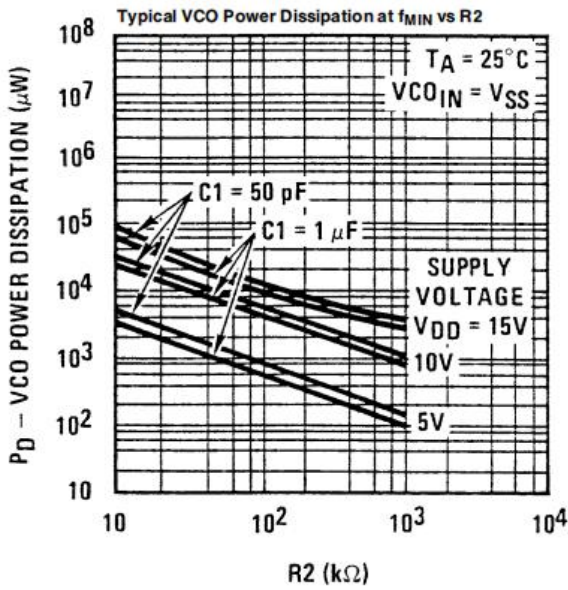


FIGURE 6b

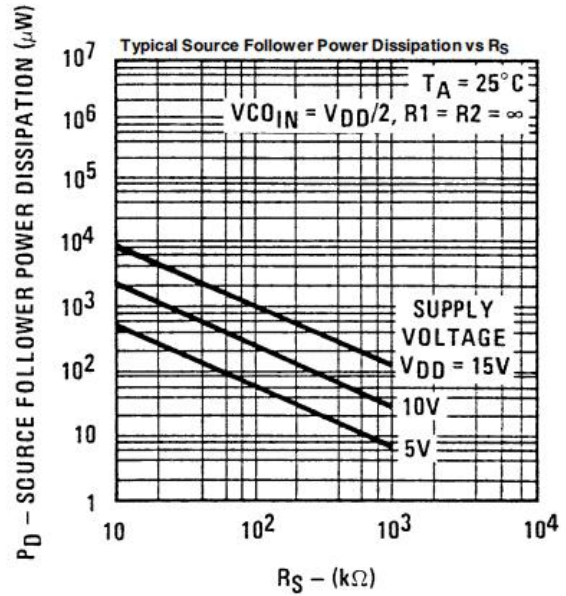


FIGURE 6c

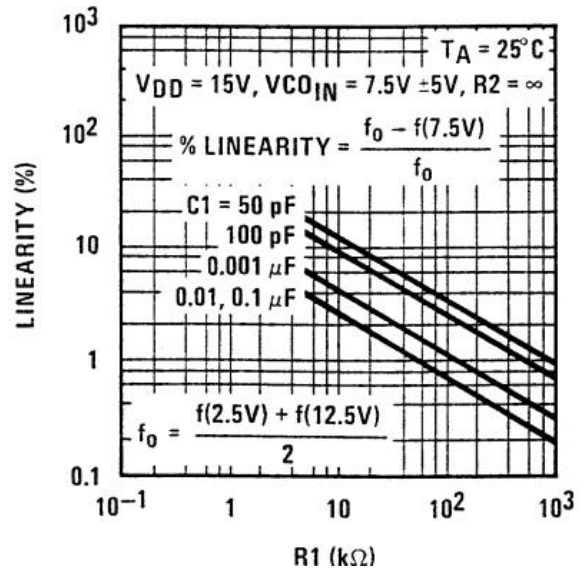
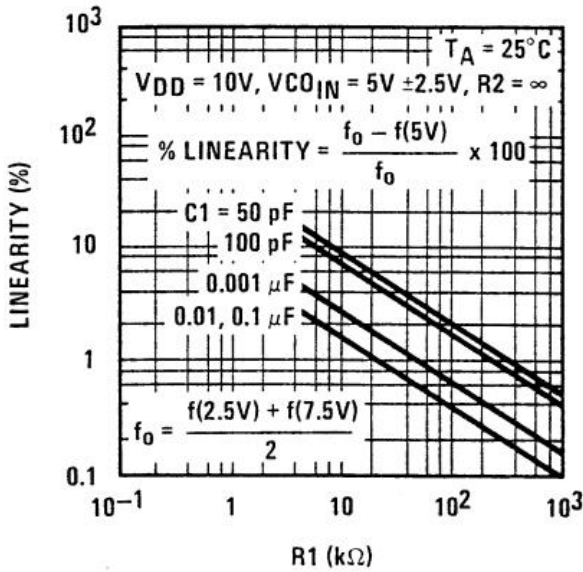
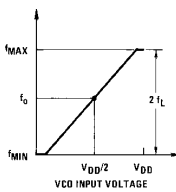
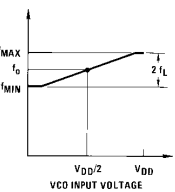
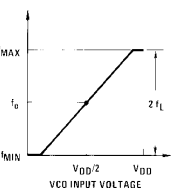
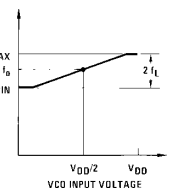
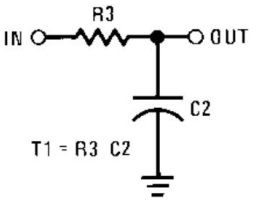
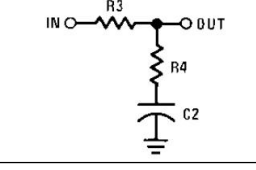


FIGURE 7. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) - P_D (fo) + P_D (fMIN) + P_D (RS); Phase Comparator II, P_D (Total) - P_D (fMIN).

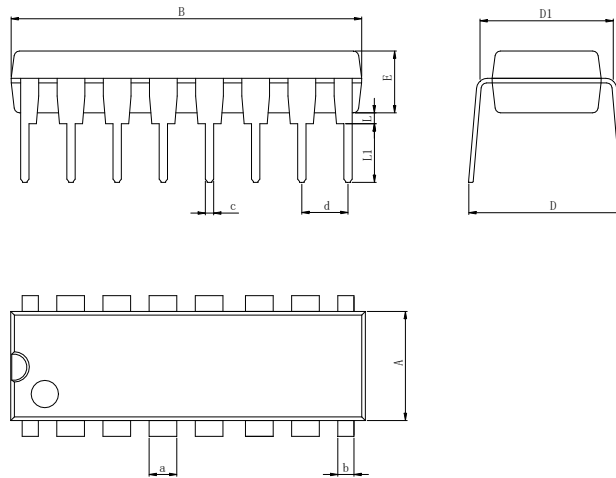
Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: $R_1, R_2 \geq 10 \text{ k}\Omega$, $R_S \geq 10 \text{ k}\Omega$, $C_1 \geq 50 \text{ pF}$. In addition to the given design information, refer to Figure 5 for R_1, R_2 and C_1 component selections.

| Characteristics | Using Phase Comparator I | | Using Phase Comparator II | |
|-------------------------------------------|-----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | VCO Without Offset $R_2 = \infty$ | VCO With Offset | VCO Without Offset $R_2 = \infty$ | VCO With Offset |
| VCO Frequency |  |  |  |  |
| For No Signal Input | VCO in PLL system will adjust to center frequency, f_o | | VCO in PLL system will adjust to lowest operating frequency, f_{min} | |
| Frequency Lock Range, $2f_L$ | $2f_L = \text{full VCO frequency range } 2f_L = f_{max} - f_{min}$ | | | |
| Frequency Capture Range, $2f_C$ |  | $2f_C \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{\pi C_2}}$ | $f_C = f_L$ | |
| Loop Filter Component Selection |  | For $2f_C$, see Ref. | | |
| Phase Angle Between Single and Comparator | 90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$) | | Always 0° in lock | |
| Locks on Harmonics of Center Frequency | Yes | | No | |
| Signal Input Noise Rejection | High | | Low | |
| VCO Component Selection | Given: f_o . Use f_o with Figure 5a to determine R_1 and C_1 . | Given: f_o and f_L . Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with Figure 5b to determine R_2 and C_1 . Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ Use $\frac{f_{max}}{f_{min}}$ with Figure 5c to determine ratio R_2/R_1 to obtain R_1 . | Given: f_{max} . Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ Use f_o with Figure 5a to determine R_1 and C_1 . | Given: f_{min} and f_{max} . Use f_{min} with Figure 5b to determine $\frac{f_{max}}{f_{min}}$. Use $\frac{f_{max}}{f_{min}}$ with Figure 5c to determine ratio R_2/R_1 to obtain R_1 . |

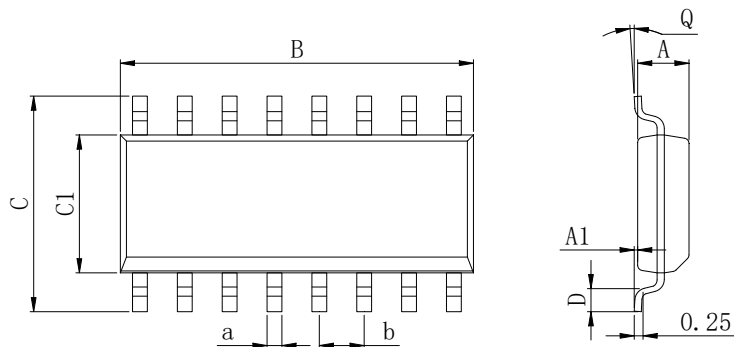
Physical Dimensions

DIP-16



| Dimensions In Millimeters(DIP-16) | | | | | | | | | | | |
|-----------------------------------|------|-------|------|------|------|------|------|------|------|------|----------|
| Symbol: | A | B | D | D1 | E | L | L1 | a | b | c | d |
| Min: | 6.10 | 18.94 | 8.10 | 7.42 | 3.10 | 0.50 | 3.00 | 1.50 | 0.85 | 0.40 | 2.54 BSC |
| Max: | 6.68 | 19.56 | 10.9 | 7.82 | 3.55 | 0.70 | 3.60 | 1.55 | 0.90 | 0.50 | |

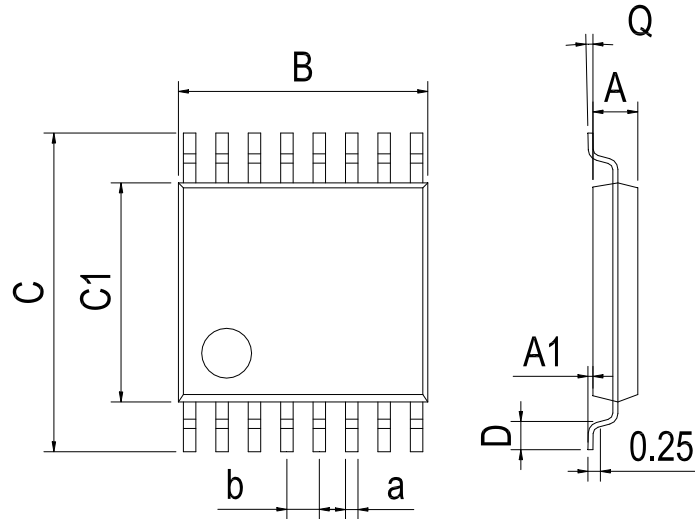
SOP-16



| Dimensions In Millimeters(SOP-16) | | | | | | | | | |
|-----------------------------------|------|------|------|------|------|------|----|------|----------|
| Symbol: | A | A1 | B | C | C1 | D | Q | a | b |
| Min: | 1.35 | 0.05 | 9.80 | 5.80 | 3.80 | 0.40 | 0° | 0.35 | 1.27 BSC |
| Max: | 1.55 | 0.20 | 10.0 | 6.20 | 4.00 | 0.80 | 8° | 0.45 | |

Physical Dimensions

TSSOP-16



| Dimensions In Millimeters(TSSOP-16) | | | | | | | | | |
|-------------------------------------|------|------|------|------|------|------|----|------|----------|
| Symbol: | A | A1 | B | C | C1 | D | Q | a | b |
| Min: | 0.85 | 0.05 | 4.90 | 6.20 | 4.30 | 0.40 | 0° | 0.20 | 0.65 BSC |
| Max: | 0.95 | 0.20 | 5.10 | 6.60 | 4.50 | 0.80 | 8° | 0.25 | |

Revision History

| DATE | REVISION | PAGE |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| 2014-6-9 | New | 1-15 |
| 2023-11-14 | Modify the package dimension diagram TSSOP-16、 Update encapsulation type、 Update Lead Temperature、 Updated DIP-16 dimension、 Add annotation for Maximum Ratings、 Update DIP Package New Model | 1、 4、 12、 13 |

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