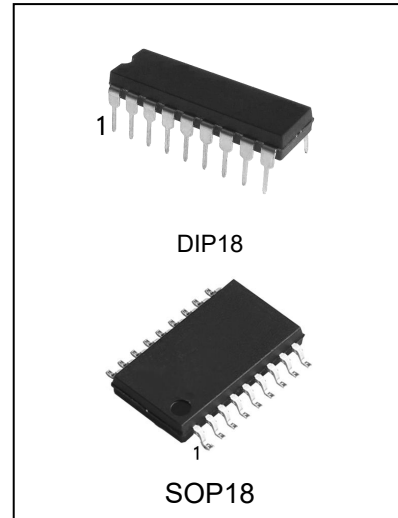


Pulse Width Modulation Control Circuit

Features

- 8.0V to 35V Operation
- 5.0V \pm 1% Trimmed Reference
- 1.0Hz to 400KHz Oscillator Range
- Dual Source/Sink Current Outputs: \pm 100mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage-Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization



ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
SG3526N	DIP18	SG3526	TUBE	800pcs/box
SG3526M/TR	SOP18	SG3526	REEL	2500pcs/reel

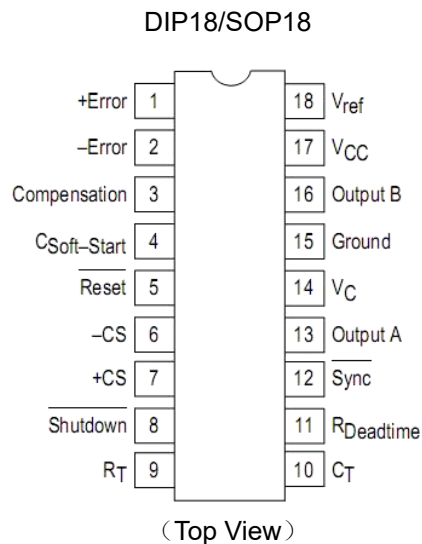
General Description

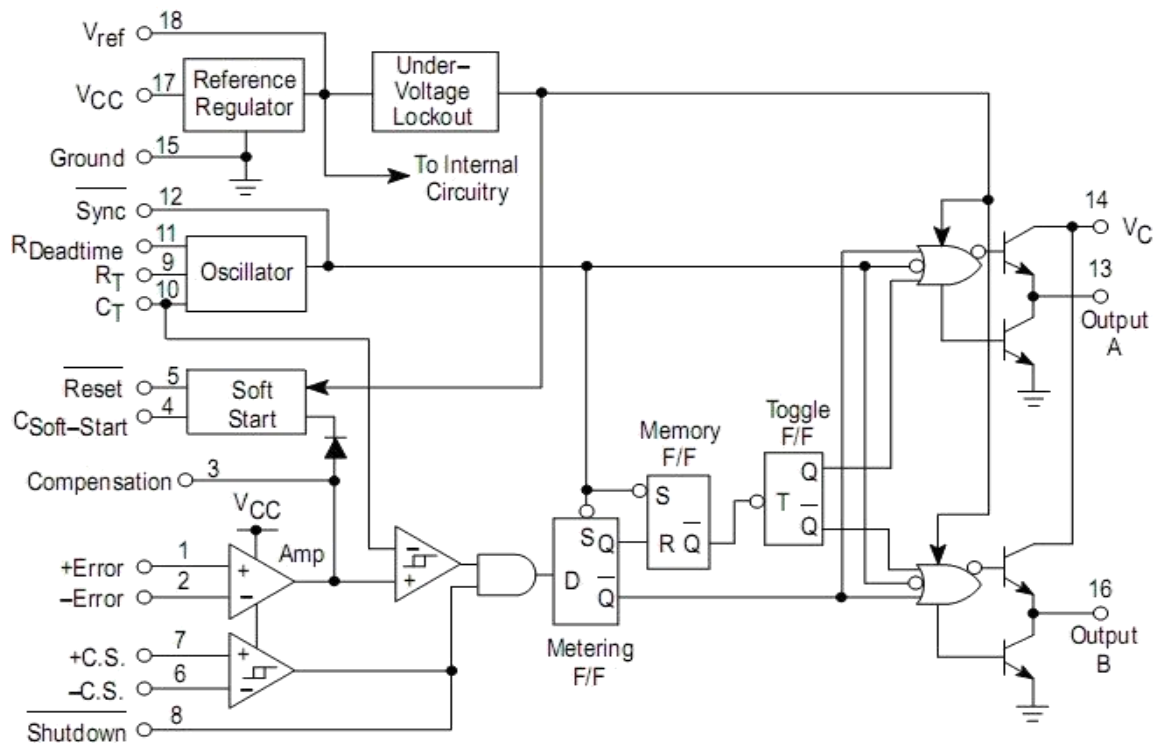
The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable deadtime and a data latch for single pulse metering;. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation or transformer coupled.

Pin Configuration



Representative Block Diagram

Maximum Ratings (Note1)

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	+40	Vdc
Collector Supply Voltage	Vc	+40	Vdc
Logic Inputs		-0.3 to + 5.5	V
Analog Inputs		-0.3 to +5.5	V
Output Current,Source or Sink	Io	±200	mA
Reference Load Current(Vcc=40V Note2)	Iref	50	mA
Logic Sink Current		15	mA
Power Dissipation Ta=+25°C (note3)	Pd	1000	mW
Operating Temperature Range	Ta	0~70	°C
Storage Temperature Range	Tstg	-65 to +150	°C
Lead Temperature(Soldering, 10Seconds)	Tsolder	±300	°C

NOTES:

1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.

Recommended Operating Conditions

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	Vcc	8.0	35	Vdc
Collector Supply Voltage	Vc	4.5	35	Vdc
Output Sink/Source Current(Each Output)	Io	0	±100	mA
Reference Load Current	Iref	0	20	mA
Oscillator Frequency Range	Fosc	0.001	400	Khz
Oscillator Timing Resistor	Rt	2.0	150	KΩ
Oscillator Timing Capacitor	Ct	0.001	20	uF
Available Deadtime Range(40Khz)	-	3.0	50	%
Operating Junction Temperature Range	Tj	0	+125	°C

ELECTRICAL CHARACTERISTICS

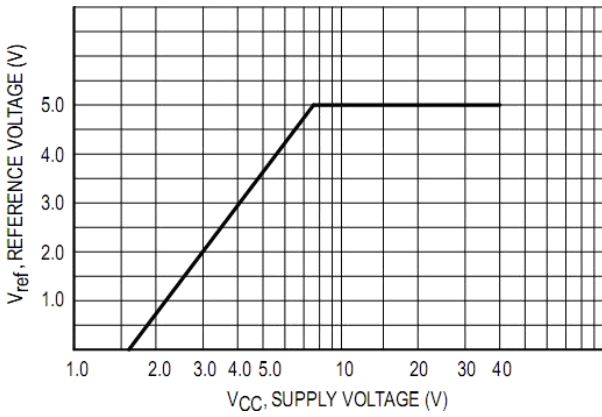
(VCC = +15 Vdc, TJ = Tlow to Thigh [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Reference Section					
Reference Output Voltage(Tj=+25°C)	Vref	4.90	5.00	5.10	V
Line Regulation(+8.0V ≤Vcc≤+35V)	Regline	-	10	30	mV
Load Regulation (0mA≤IL≤20mA)	Regload	-	10	50	mV
Short Circuit Current(Vref=0V)	Isc	25	80	125	mA
Undervoltage Lockout					
Reset Output Voltage(Vref=+3.8V)		-	0.2	0.4	V
Reset Output Voltage(Vref=+4.8V)		2.4	4.8	-	V
Oscillator Section(Note5)					
Initial Accuracy(Tj=+25°C)		-	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0V ≤Vcc≤+35V)	$\Delta f_{osc}/\Delta V_{CC}$	-	0.5	1.0	%
Minimum Frequency (Rt=150Kohm,Ct=20uF)	Fmin	-	0.5	-	Hz
Maximum Frequency (Rt=2.0Kohm,Ct=0.001uF)	Fmax	400	-	-	KHz
Sawtooth Peak Voltage (Vcc=35V)	Vosc(p)	-	3.0	3.5	V
Sawtooth Valley Voltage(Vcc=8.0V)	Vosc(V)	0.45	0.8	-	V
Error Amplifier Section (note6)					
Input Offset Voltage	Vio	-	2.0	10	mV
Input Bias Current	Iib	-	-350	-2000	nA
Input Offset Current	Iio	-	35	200	nA
Characteristics	Symbol	Min	Typ	Max	Unit

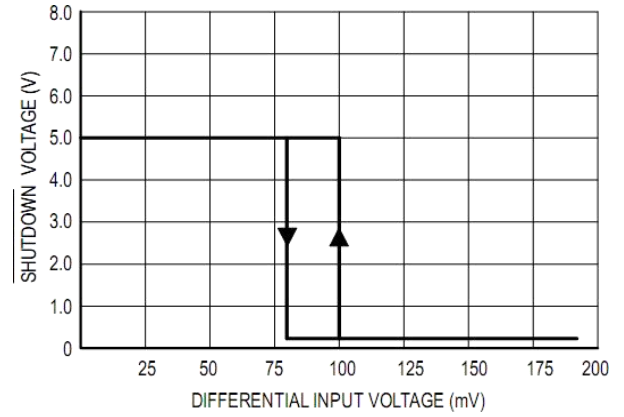
DC Open Loop Gain($R_l \geq 10\text{Mohm}$)	A_v	60	72	-	dB
High Output Voltage ($V_{pin1}-V_{pin2} \geq +150\text{mV}$, $I_{source}=100\mu\text{A}$)	V_{oh}	3.6	4.2	-	V
Low Output Voltage ($V_{pin2}-V_{pin1} \geq +150\text{mV}$, $I_{sink}=100\mu\text{A}$)	V_{ol}	-	0.2	0.4	V
Common Mode Rejection Ratio($R_s \leq 2.0\text{Kohm}$)	CMRR	70	94	-	dB
Power Supply Rejection Ration($+12\text{V} \leq V_{cc} \leq +18\text{V}$)	PSRR	66	80	-	dB
PWM Comparator Section(Note5)					
Minimum Duty Cycle ($V_{compensation} = +0.4\text{V}$)	D_{cmin}	-	-	0	%
Maximum Duty Cycle ($V_{compensation} = +3.6\text{V}$)	D_{cmax}	45	49	-	%
Digital Ports(SYNC,SHUTDOWN,RESET)					
Output Voltage (High Logic Level) ($I_{source}=40\mu\text{A}$) (Low Logic Level) ($I_{sink}=3.6\text{mA}$)	V_{oh} V_{ol}	2.4 -	4.0 0.2	- 0.4	V
Input Current-High Logic Level (High Logic Level) ($V_{ih}=+2.4\text{V}$) (Low Logic Level) ($V_{il} = +0.4\text{V}$)	I_{ih} I_{il}	- -	-125 -225	-200 -360	μA
Current Limit Comparator Section(note7)					
Sense Voltage($R_s \leq 50 \Omega$)	V_{sense}	80	100	120	mA
Input Bias Current	I_{ib}	-	-3.0	-10	μA
Soft-Start Section					
Error Clamp Voltage(Reset=+0.4V)		-	0.1	0.4	V
Csoft-Start Charging Current(Reset=+2.4V)	I_{cs}	50	100	150	μA
Output Drivers (each output, $V_c = +15\text{Vdc}$) Unless otherwise noted.					
Output High Level $I_{source} = 20\text{mA}$ $I_{source} = 100\text{mA}$	V_{oh}	12.5 12	13.5 13	- -	V
Output Low Level $I_{sink} = 20 \text{mA}$ $I_{sink} = 100\text{mA}$	V_{ol}	- -	0.2 1.2	0.3 2.0	V
Collector Leakage, $V_c = +40\text{V}$	$I_c(\text{Leak})$	-	50	150	μA
Rise Time($C_L = 1000\text{pF}$)	T_r	-	0.3	0.6	μs
Fall Time ($C_L = 1000\text{pF}$)	T_f	-	0.1	0.2	μs
Supply Current (Shutdown = +0.4V, $V_{cc} = +35\text{V}$, $R_t = 4.12\text{K} \Omega$)	I_{cc}	-	18	30	mA

Notes:

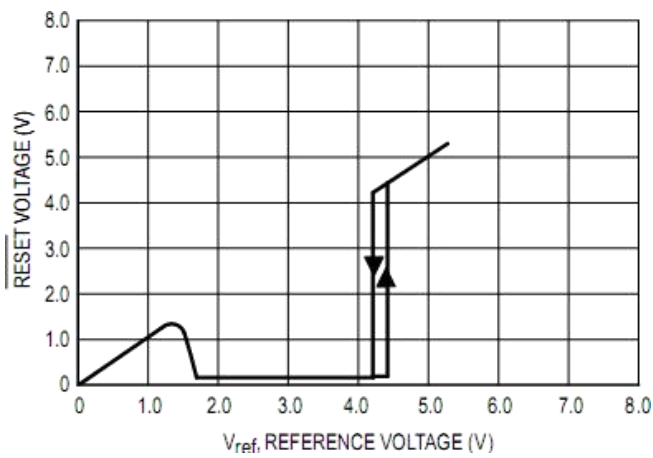
- $T_{low} = 0^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$
- $f_{osc} = 40\text{KHz}$ ($R_t = 4.12\text{k} \Omega \pm 1\%$, $C_T = 0.01\mu\text{F} \pm 1\%$, $R_D = 0 \Omega$)
- $0\text{V} \leq V_{CM} \leq +5.2\text{V}$
- $0\text{V} \leq V_{CM} \leq +12\text{V}$



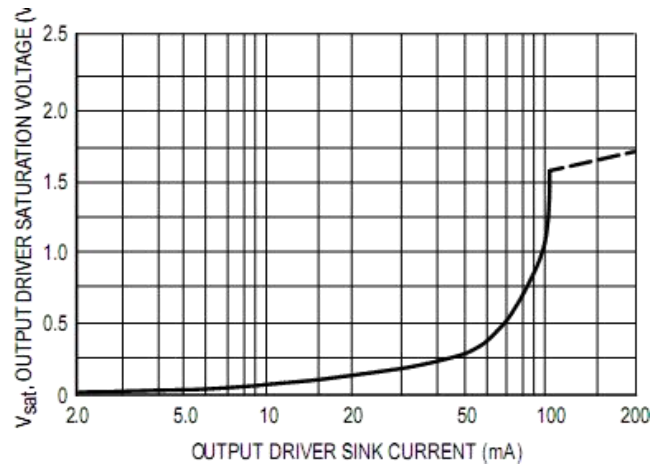
Reference Voltage as a Function Supply Votage



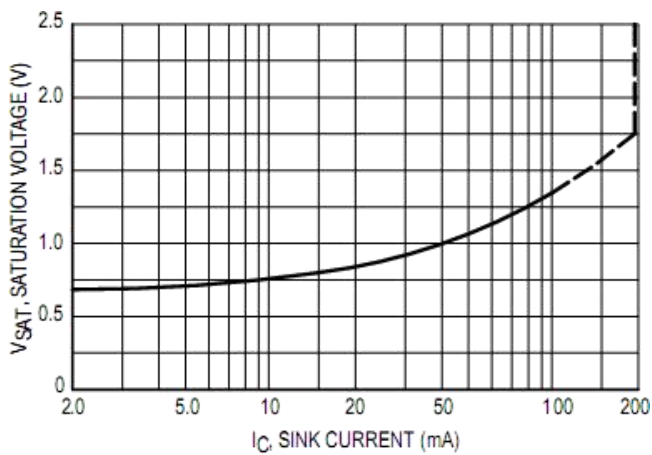
Current Limit Comparator Threshold



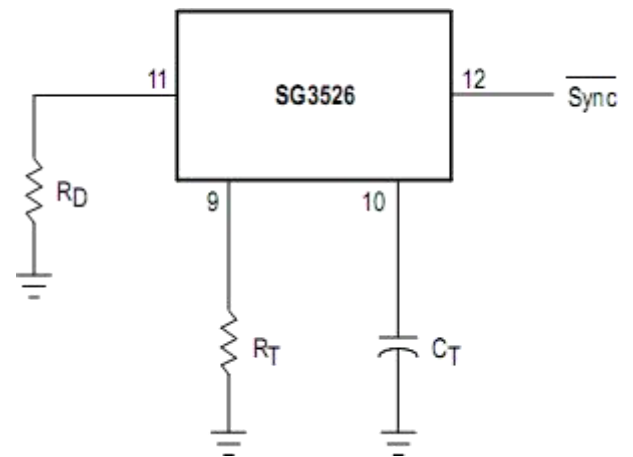
UnderVoltage Lockout Characteristic



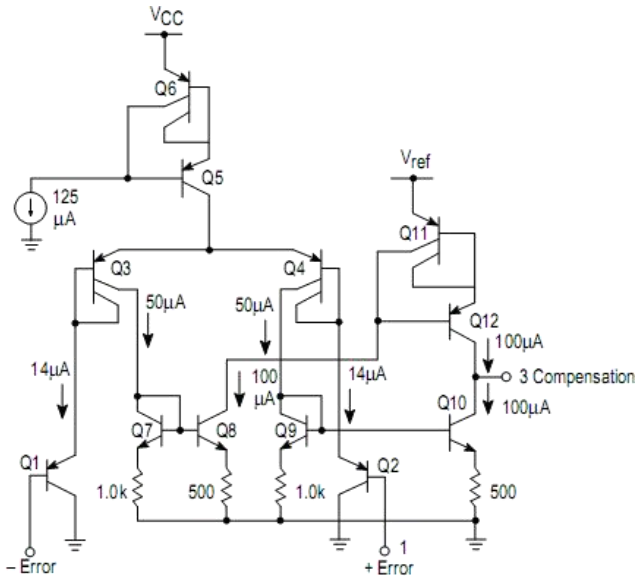
Output Driver Saturation Voltage as a Function of Sink Current



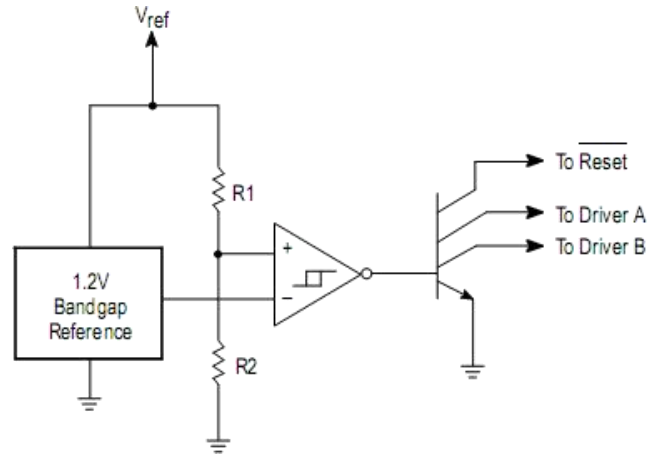
Vc Saturation Voltage as a Function of Sink Current



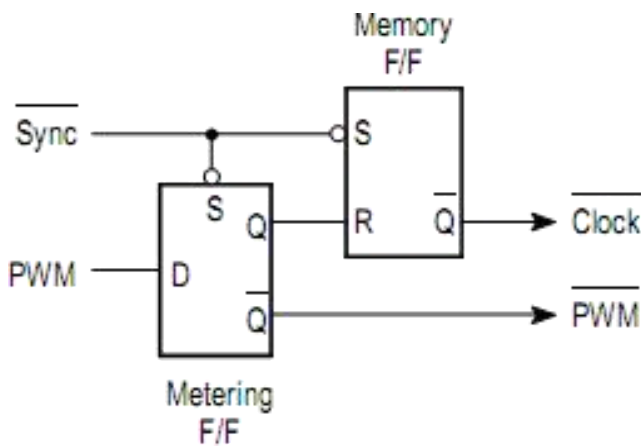
Oscillator Connections



Error Amplifier



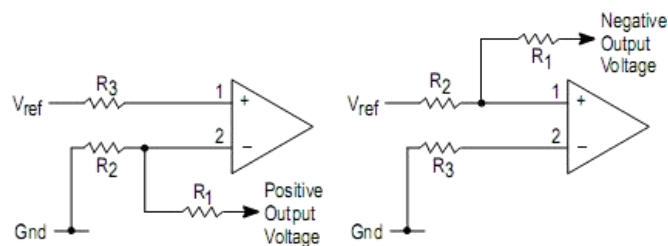
Undervoltage Lockout



Pulse Processing Logic

The metering Flip-Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip-Flop prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

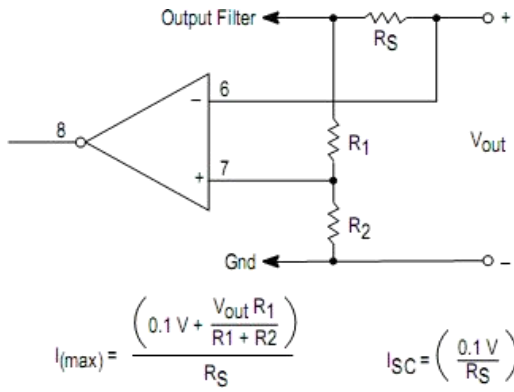


$$V_{out} = V_{ref} \left(\frac{R_1 + R_2}{R_2} \right)$$

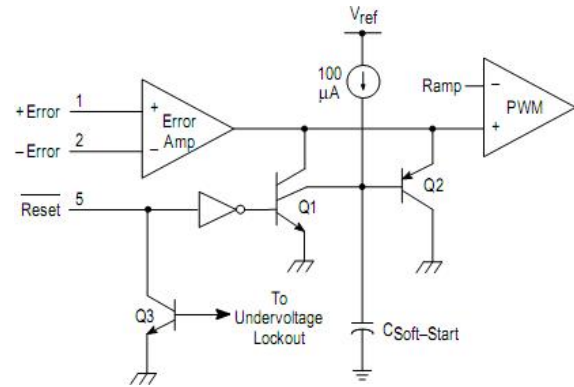
$$V_{out} = V_{ref} \left(\frac{R_1}{R_2} \right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2} \right)$$

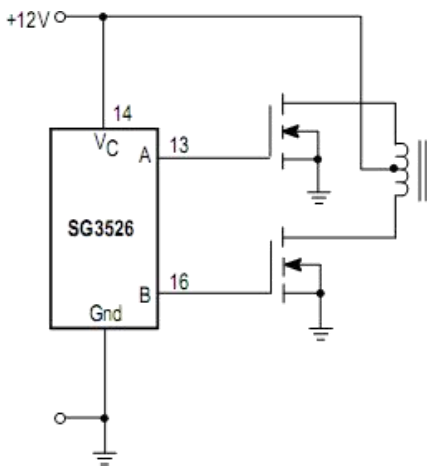
Error Amplifier Connects



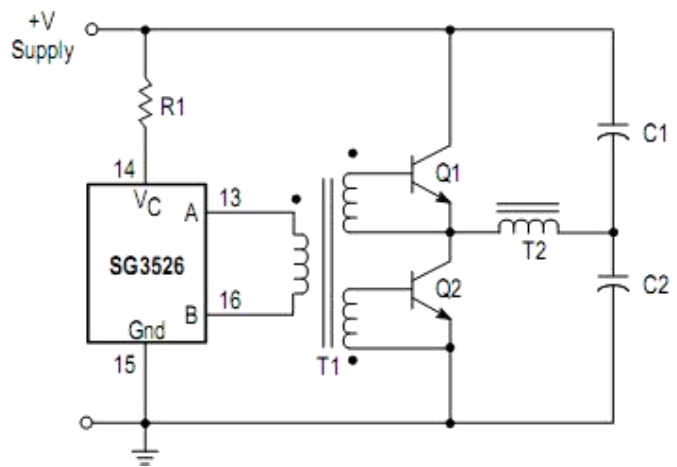
Foldback Current Limiting



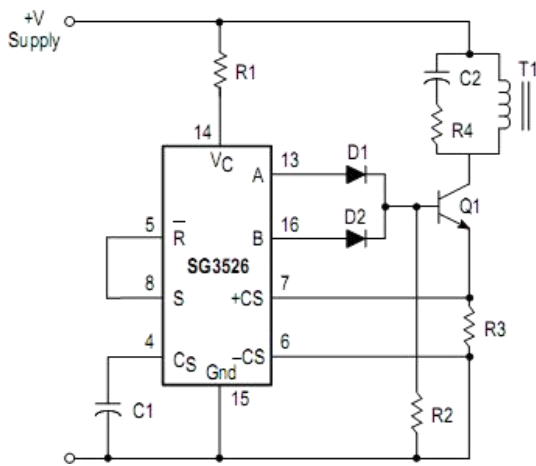
Soft-Start Circuitry



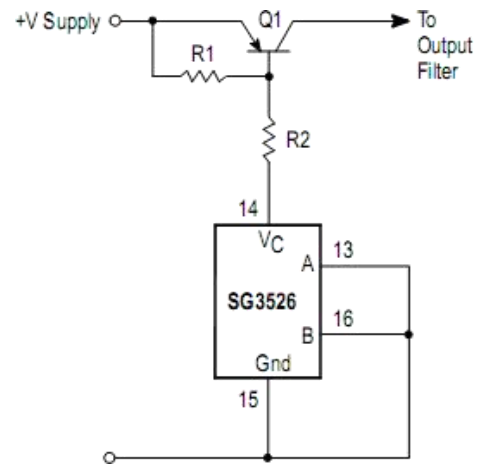
Driving VMOS Power FETs



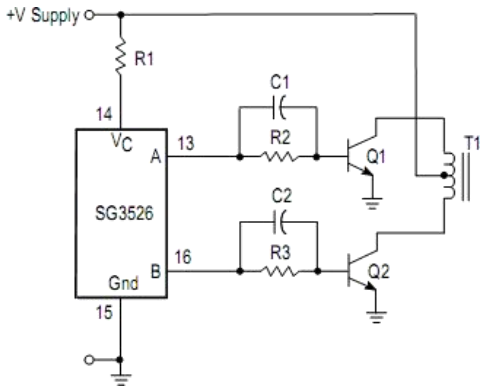
Half-Bridge Configuration



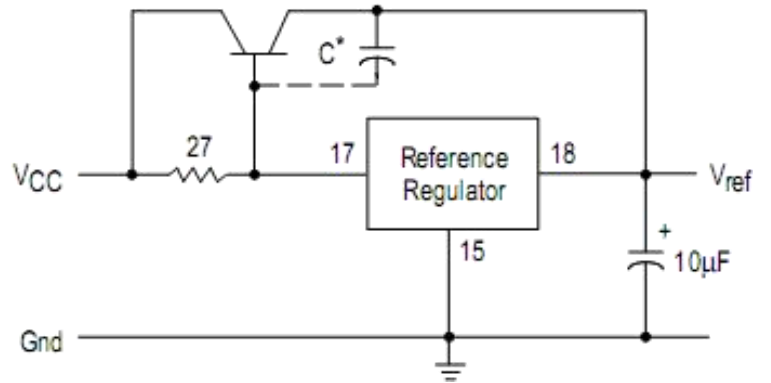
Flyback Converter with Current Limiting



Single-Ended Configuration



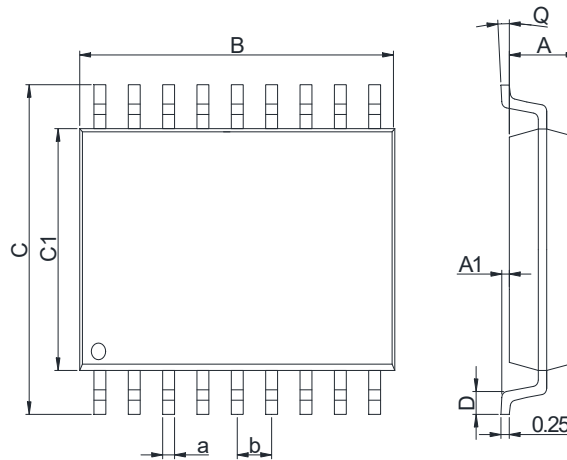
Push-Pull Configuration



Extending Reference Output Current Capability

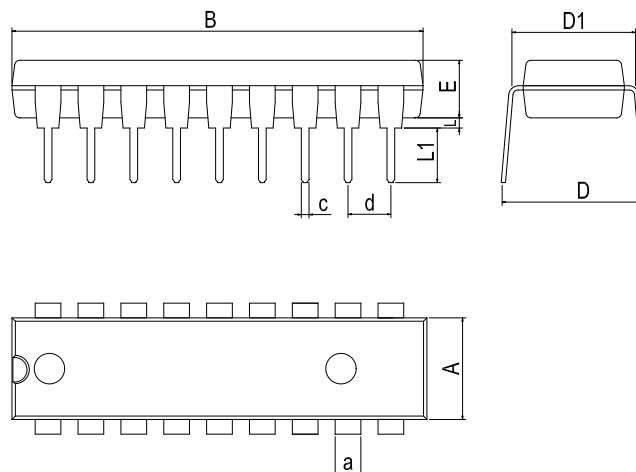
Package Information

SOP18



Dimensions In Millimeters(SOP18L)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.08	11.25	10.10	7.30	0.7	0°	0.35	1.27 BSC
Max:	2.50	0.28	11.65	10.50	7.70	1	8°	0.44	

DIP18



Dimensions In Millimeters(DIP18)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	22.24	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	23.24	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

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