Quad 2−Input NOR Gate
High−Performance Silicon−Gate CMOS

FEATURES

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance:

  HBM 2000 V;

  Machine Model 200 V
- Chip Complexity: 40 FETs or 10 Equivalent Gates
- These are Pb−Free Devices

DIP-14

SOP-14

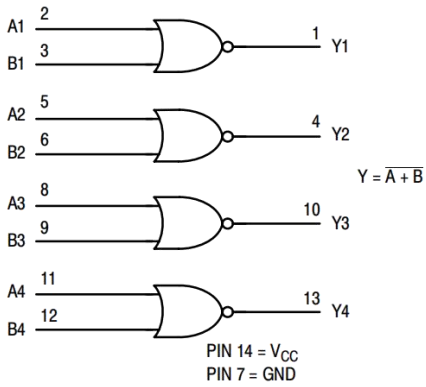
TSSOP-14

QFN-16 3*3

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC02N	DIP-14	74HC02	TUBE	1000pcs/box
74HC02M/TR	SOP-14	74HC02	REEL	2500pcs/reel
74HC02MT/TR	TSSOP-14	HC02	REEL	2500pcs/reel
74HC02LQ/TR	QFN-16 3*3	HC02	REEL	5000pcs/reel

LOGIC DIAGRAM

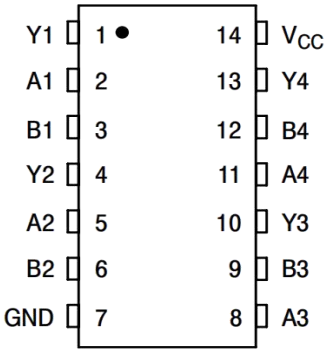


FUNCTION TABLE

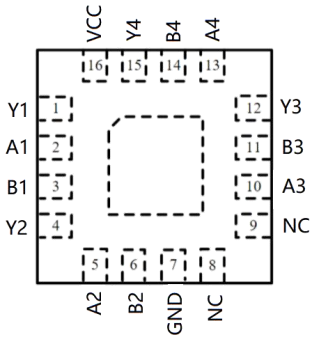
Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

PIN ASSIGNMENT

DIP-14/SOP-14/TSSOP-14



QFN-16 3*3



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	20	mA
I_{out}	DC Output Current, per Pin	25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	50	mA
P_D	Power Dissipation in Still Air, SOP Package TSSOP Package	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOP or TSSOP Package	245	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance cir- cuit. For proper operation, Vin and Vout should be constrained to the range GND ≤ (Vin or Vout) ≤ VCC. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC).Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not im- plied. Extended exposure to stresses above the Recommended Operating Conditions may af- fect device reliability.

Derating SOP Package: 7 mW/°C from 65° to 125°C ； TSSOP Package: 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+ 85	°C
t_r, t_f	Input Rise and Fall Time(Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limit			Unit
				-40 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level OutputVoltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.7 5.2	
V_{OL}	Maximum Low−Level OutputVoltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	0.1	1.0	1.0	μA
I_{CC}	Maximum Quiescent SupplyCurrent (per Package)	V_{in} = V_{CC} or GND $\|I_{out}\|$ = 0 μA	6.0	2.0	20	40	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input tr = tf = 6.0 ns)

Symbol	Parameter	V_{CC} (V)	Guaranteed Limit			Unit
			-40 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	——	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25 C, V_{CC} = 5.0 V	pF
		22	

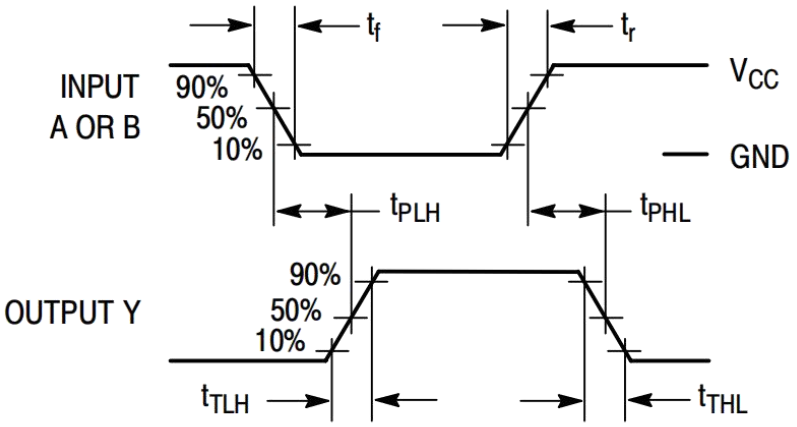
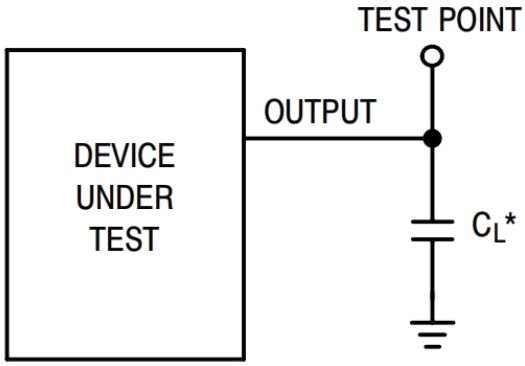


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

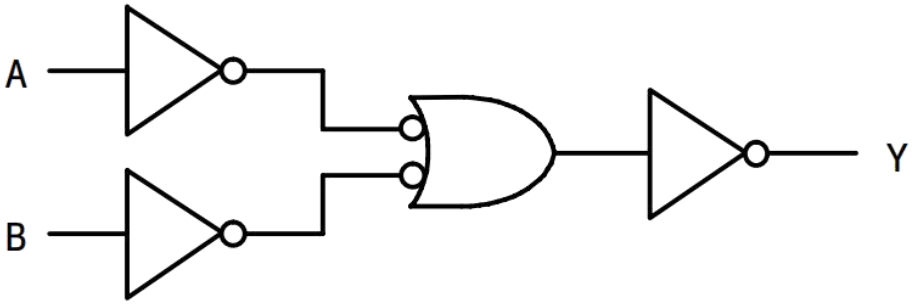
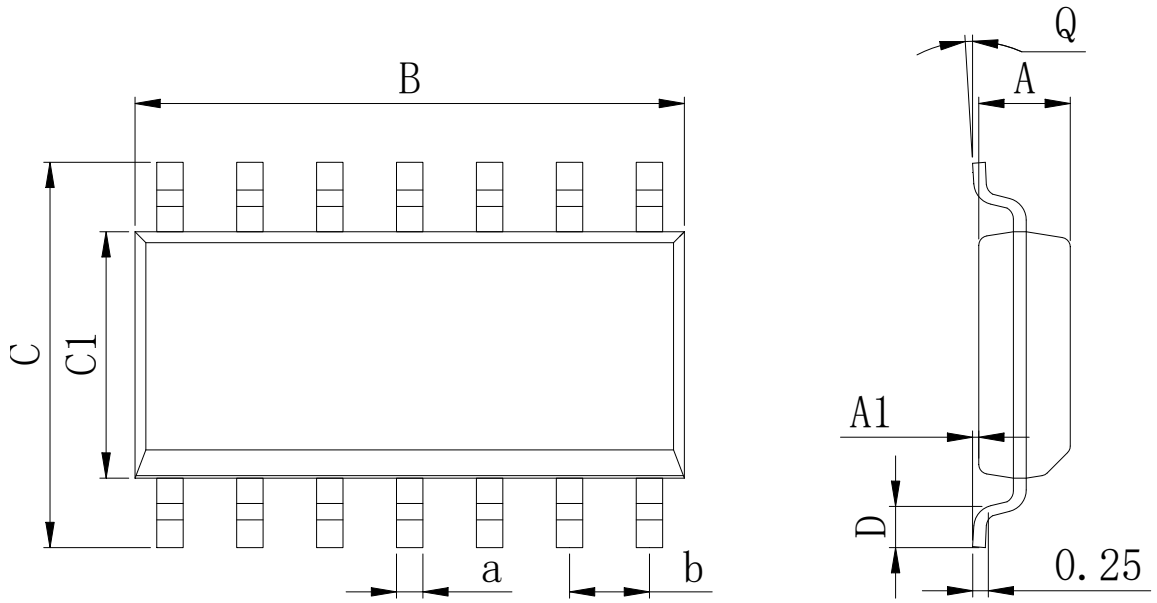


Figure 3. Expanded Logic Diagram
(1/4 of the Device)

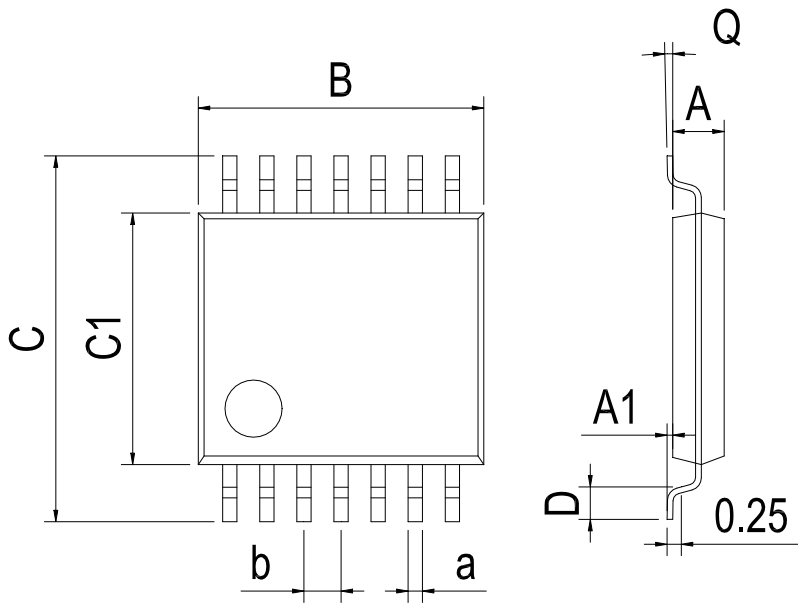
PHYSICAL DIMENSIONS

SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

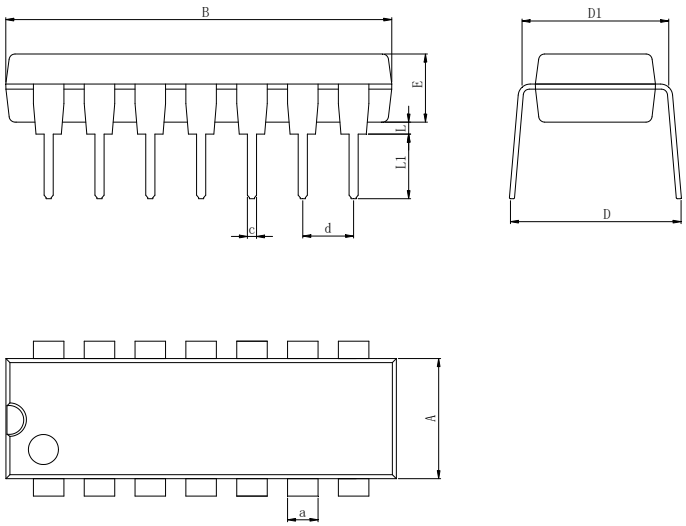
TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

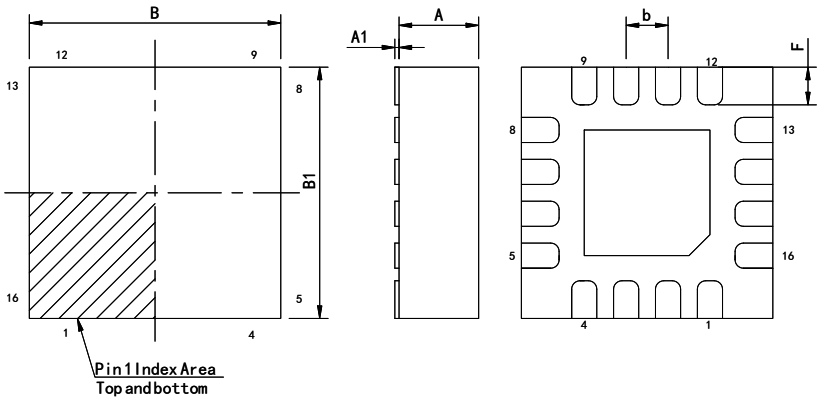
PHYSICAL DIMENSIONS

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	0.30	

REVISION HISTORY

DATE	REVISION	PAGE
2019-5-9	New	1-9
2023-8-31	Update Lead Temperature、Update encapsulation type、Updated DIP-14 dimension	1、3、7
2024-8-7	Add the QFN-16 package device	1

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