

DS34C86 Quad CMOS Differential Line Receiver

General Description

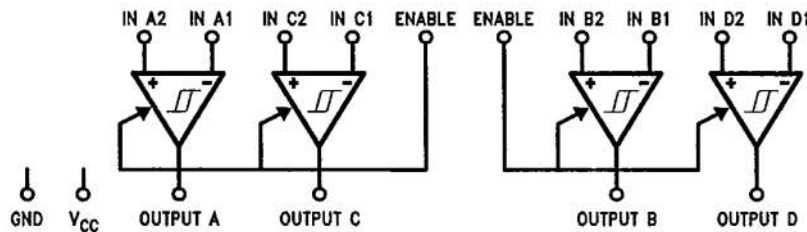
The DS34C86 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS. The DS34C86 has an input sensitivity of 200 mV over the common mode input voltage range of $\pm 7V$. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE[®] outputs have 6 mA source and sink capability. The DS34C86 is pin compatible with the DS3486.

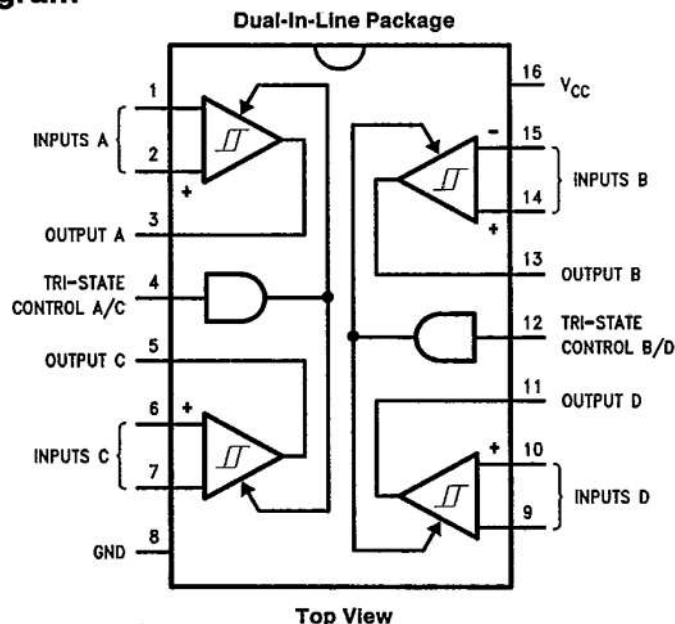
Features

- Low power CMOS design
- $\pm 0.2V$ sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Inputs won't load line when $V_{CC} = 0V$
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

Logic Diagram



Connection Diagram



Order Number DS34C86J, DS34C86M, and DS34C86N
See NS Package Number J16A, M16A and N16A

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	$\pm 14V$
Differential Input Voltage (V_{DIFF})	$\pm 14V$
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering 10 sec)	$260^{\circ}C$
Current Per Output	± 25 mA

Operating Conditions

T-75-45-05

	Min	Max	Unit
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	-40	$+85$	$^{\circ}C$
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	-0.2		$+0.2$	V
R_{IN}	Input Resistance	$-7V < V_{CM} < +7V$ (One Input AC GND)		10		k Ω
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		$+1.1$ -1.6		mA mA
V_{OH}	Minimum High Level Output Voltage	$V_{CC} = \text{Min.}$, $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	$V_{CC} = \text{Max.}$, $V_{(DIFF)} = +1V$ $I_{OUT} = 6.0$ mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		± 0.5	± 5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			± 1.0	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{(DIFF)} = +1V$		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ (unless otherwise specified) (Note 3)

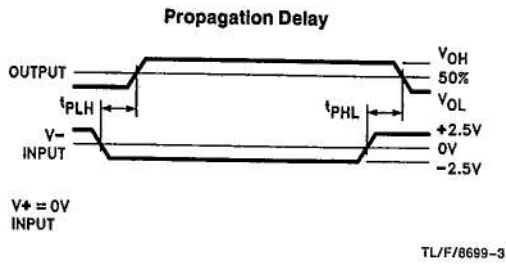
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$C_L = 50$ pF $V_{DIFF} = 2.5V$		20		ns
t_{PLZ} , t_{PHZ}	Propagation Delay TRI-STATE Control to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		12		ns
t_{pZL} , t_{pZH}	Propagation Delay TRI-STATE Control to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		14		ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

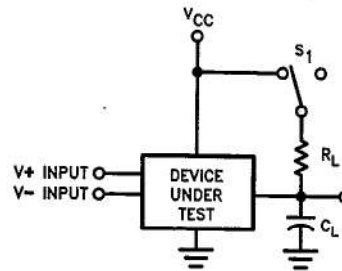
Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.

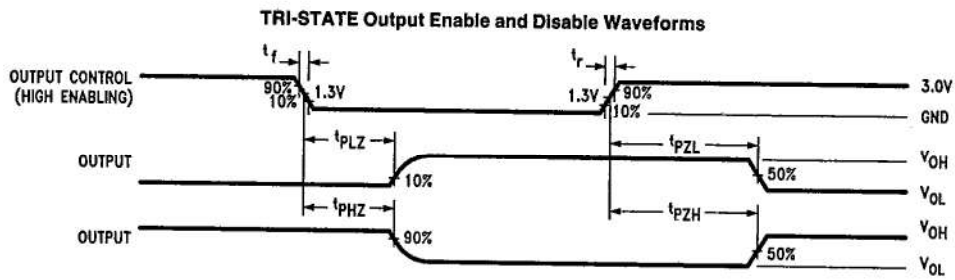
All typicals are given for $V_{CC} = 5V$ and $T_A = 25^{\circ}C$.



Test Circuit for TRI-STATE Output Tests



C_L Includes load and test jig capacitance.
S1 = VCC for t_{PZL} and t_{PLZ} measurements.
S1 = GND for t_{PZH} and t_{PHZ} measurements.



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