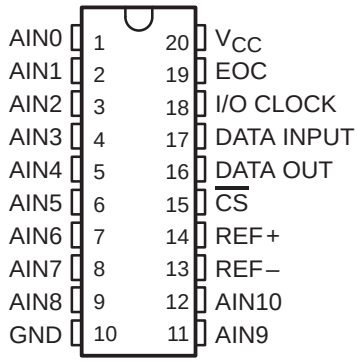
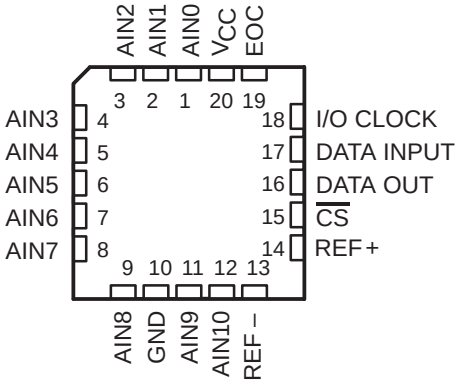
12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample-and-Hold Function**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect to 1/2 the Applied Voltage Reference)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**
- **Application Report Available†**

DB, DW, J, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



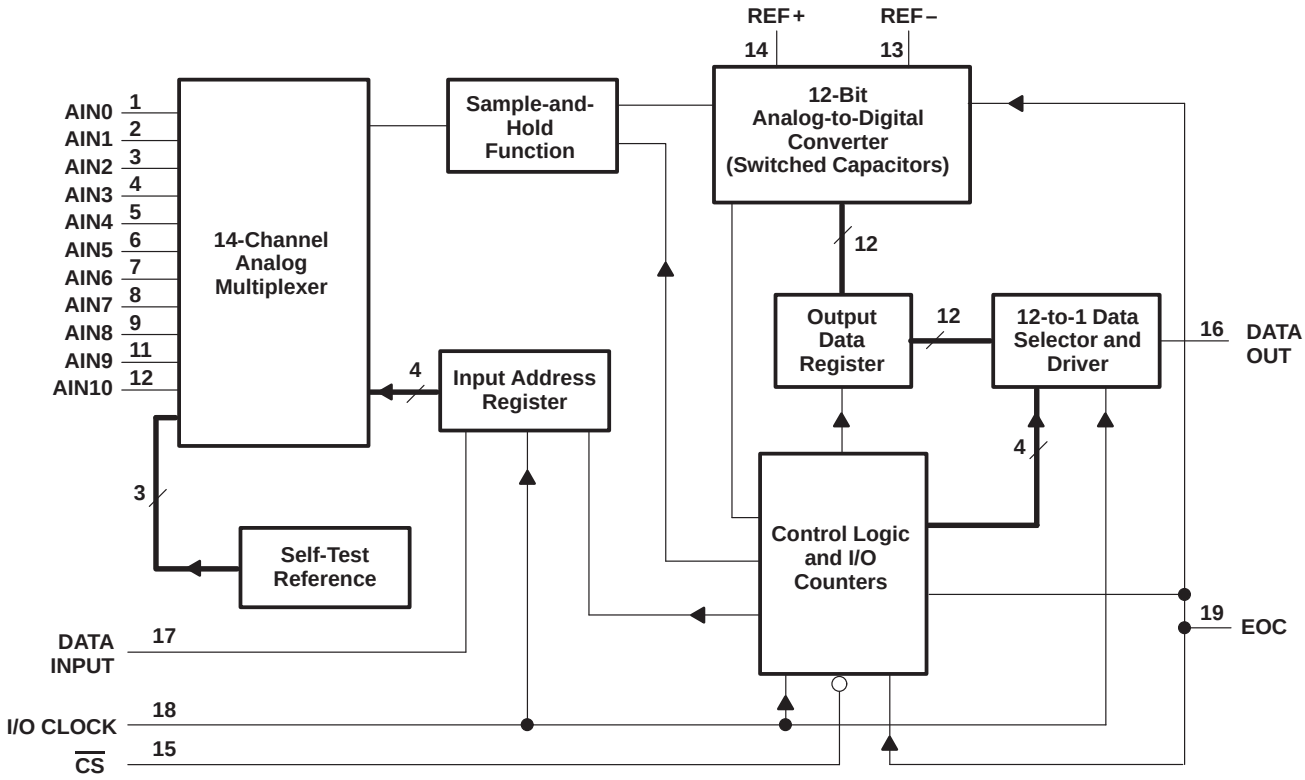
description

The TLC2543C and TLC2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters. Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLC2543C is characterized for operation from T_A = 0°C to 70°C. The TLC2543I is characterized for operation from T_A = −40°C to 85°C. The TLC2543M is characterized for operation from T_A = −55°C to 125°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AIN0 – AIN10	1–9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and be capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB† value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB / LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
GND	10		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of the I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	Positive reference voltage The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20		Positive supply voltage

† MSB/LSB = Most significant bit /least significant bit

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} . . . . . V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} . . . . . –0.1 V
Peak input current, I_I (any input) . . . . . ±20 mA
Peak total input current, I_I (all inputs) . . . . . ±30 mA
Operating free-air temperature range, T_A: TLC2543C . . . . . 0°C to 70°C
TLC2543I . . . . . –40°C to 85°C
TLC2543M . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.1	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK		0		4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 4)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 4)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 5)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 5)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		120			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		120			ns
Transition time, I/O CLOCK high to low, $t_{t(I/O)}$ (see Note 4 and Figure 6)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLC2543C	0		70	°C
	TLC2543I	–40		85	
	TLC2543M	–55		125	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).

3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, $f_{(I/O\ CLOCK)} = 4.1$ MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TLC2543C, TLC2543I			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	High-impedance off-state output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	2.5	µA
I_{IL}	Low-level input current		V_I = 0			1	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	µA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	µA
			Selected channel at 0 V, Unselected channel at V_{CC}				–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	µA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, $f_{(I/O\ CLOCK)} = 4.1$ MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TLC2543M			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	High-impedance off-state output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	10	µA
I_{IL}	Low-level input current		V_I = 0			1	–10	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	10	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	µA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			10	µA
			Selected channel at 0 V, Unselected channel at V_{CC}				–10	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	µA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

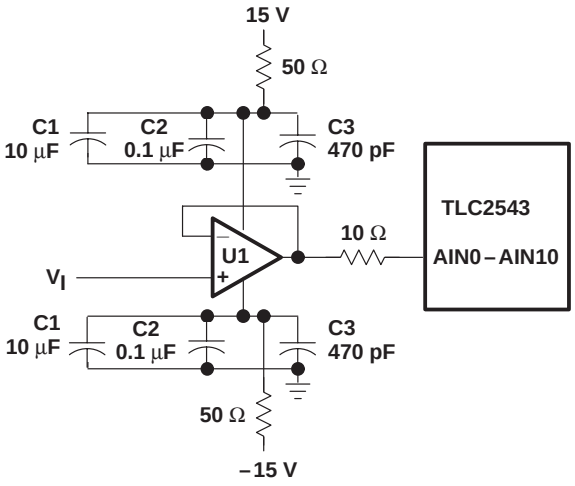
operating characteristics over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.5 V to 5.5 V, $f_{(I/O\ CLOCK)}$ = 4.1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)	See Figure 2			±1	LSB
E_D	Differential linearity error	See Figure 2			±1	LSB
E_O	Offset error (see Note 6)	See Note 2 and Figure 2			±1.5	LSB
E_G	Gain error (see Note 6)	See Note 2 and Figure 2			±1	LSB
E_T	Total unadjusted error (see Note 7)				±1.75	LSB
	Self-test output code (see Table 3 and Note 8)	DATA INPUT = 1011		2048		
		DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
t_{conv}	Conversion time	See Figures 9–14		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 9–14 and Note 9			10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 9–14 and Note 9	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			150	ns
$t_{d(I/O-EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 7		1.5	2.2	µs
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven)	See Figure 3		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 3		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 6		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 6		15	50	ns
$t_{d(I/O-CS)}$	Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)				5	µs

† All typical values are at T_A = 25°C.

NOTES:
2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
7. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.
9. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
10. Any transitions of $\overline{CS}$ are recognized as valid only when the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-μF 35-V tantalum capacitor	—
C2	0.1-μF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain Hi-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 1. Analog Input Buffer to Analog Inputs AIN0 – AIN10

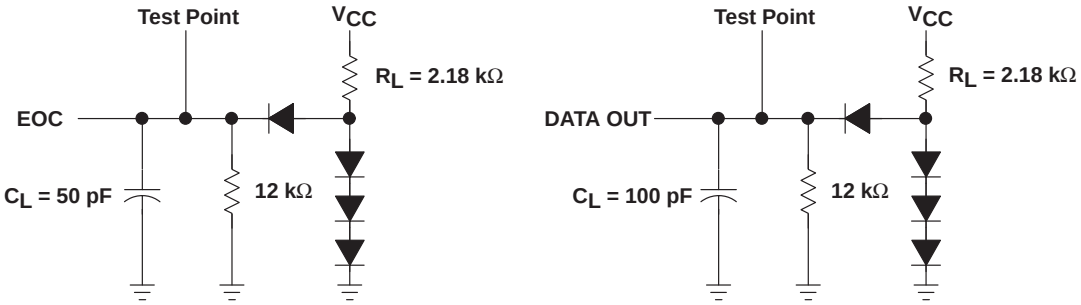


Figure 2. Load Circuits

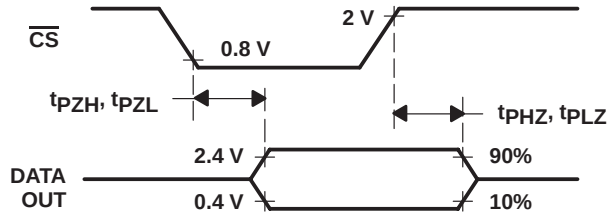


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

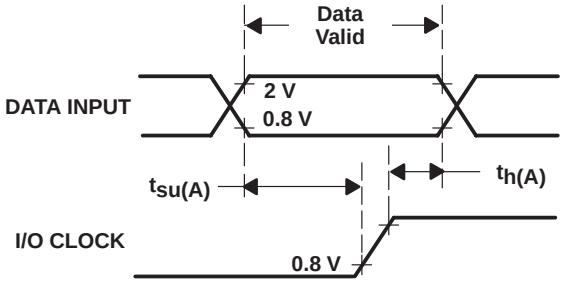
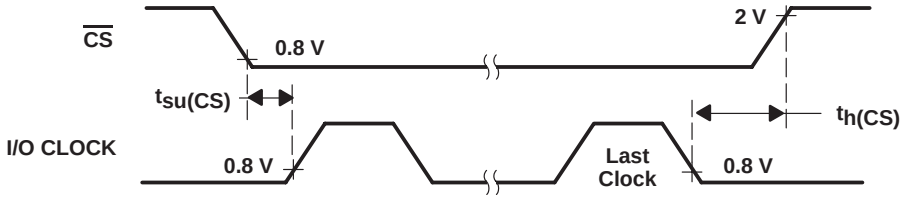


Figure 4. DATA INPUT and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

Figure 5. $\overline{CS}$ and I/O CLOCK Voltage Waveforms

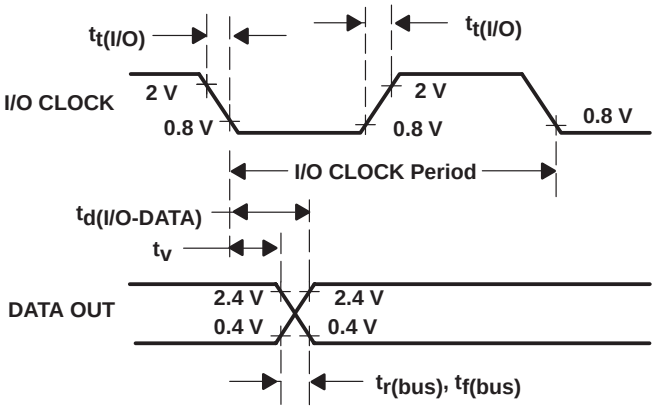


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

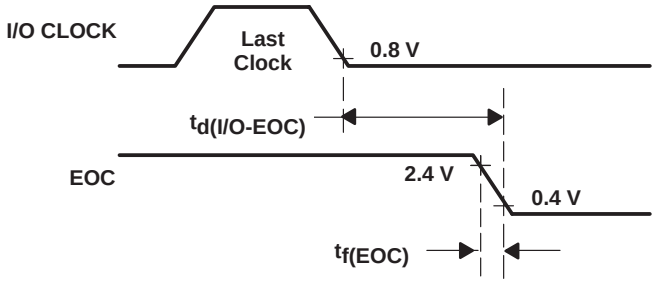


Figure 7. I/O CLOCK and EOC Voltage Waveforms

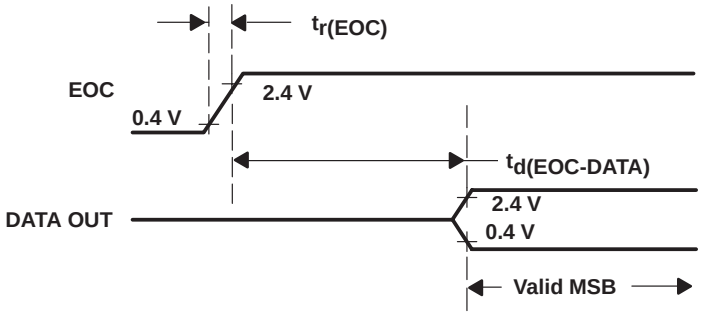
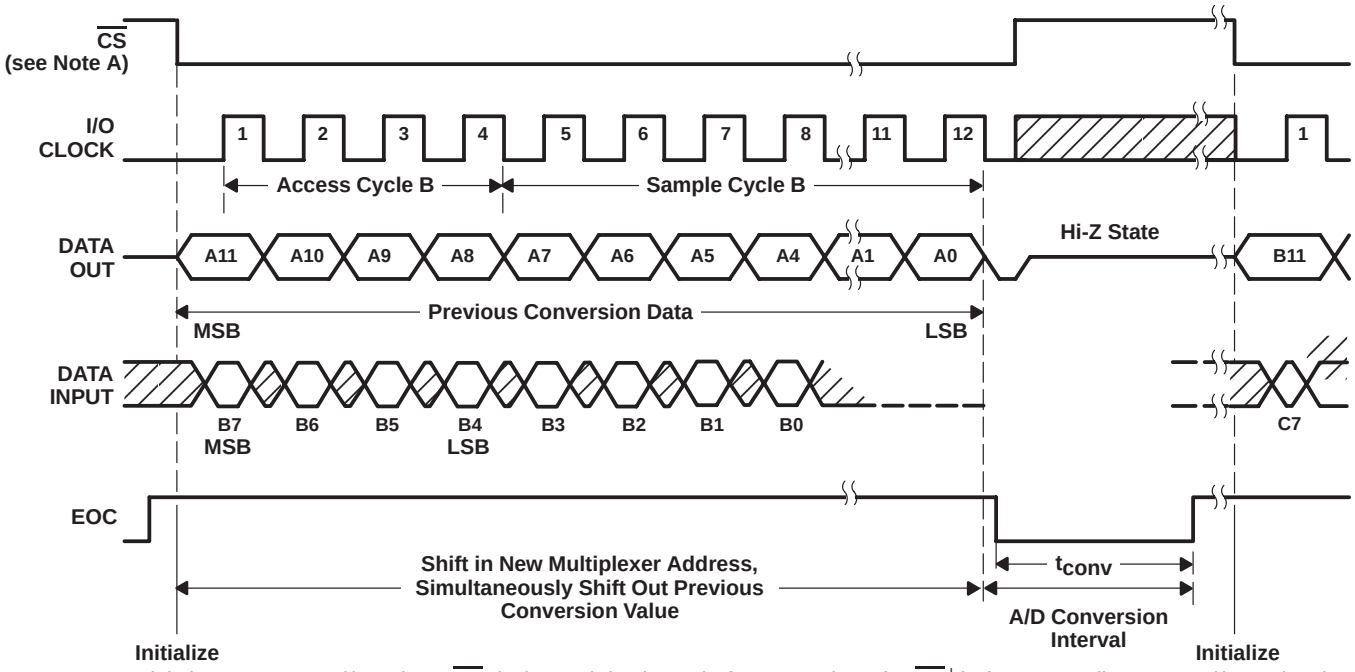


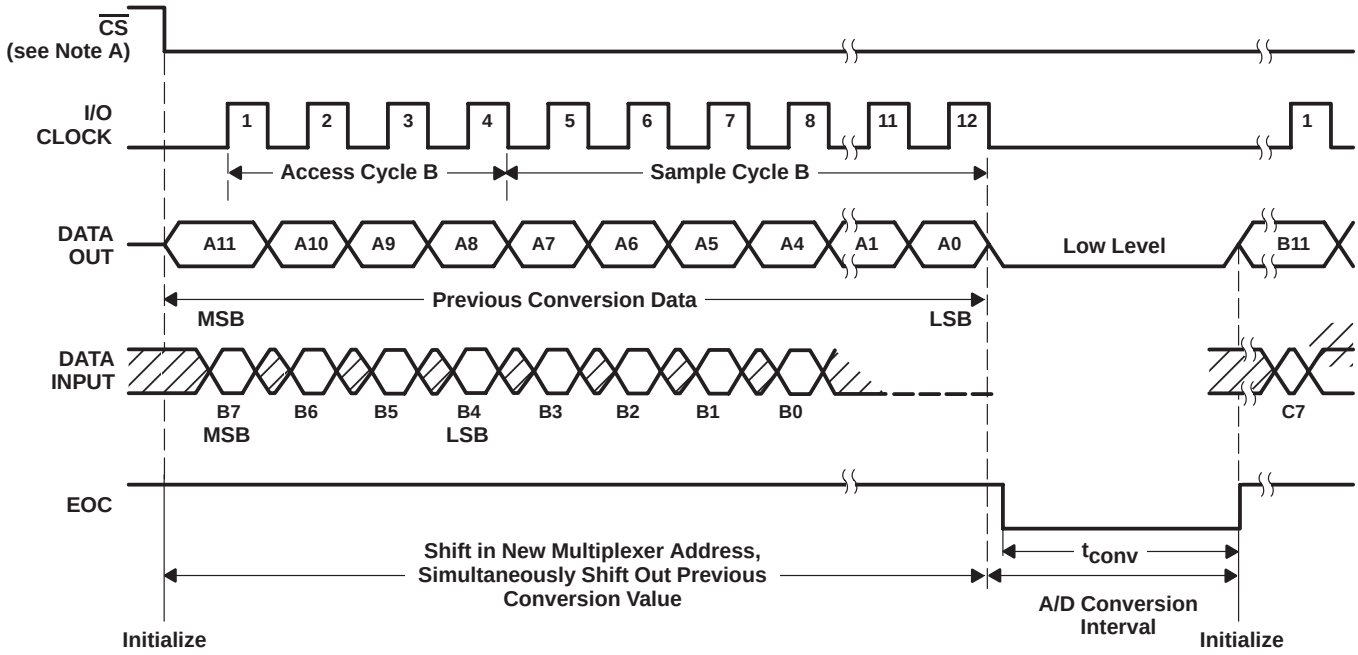
Figure 8. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

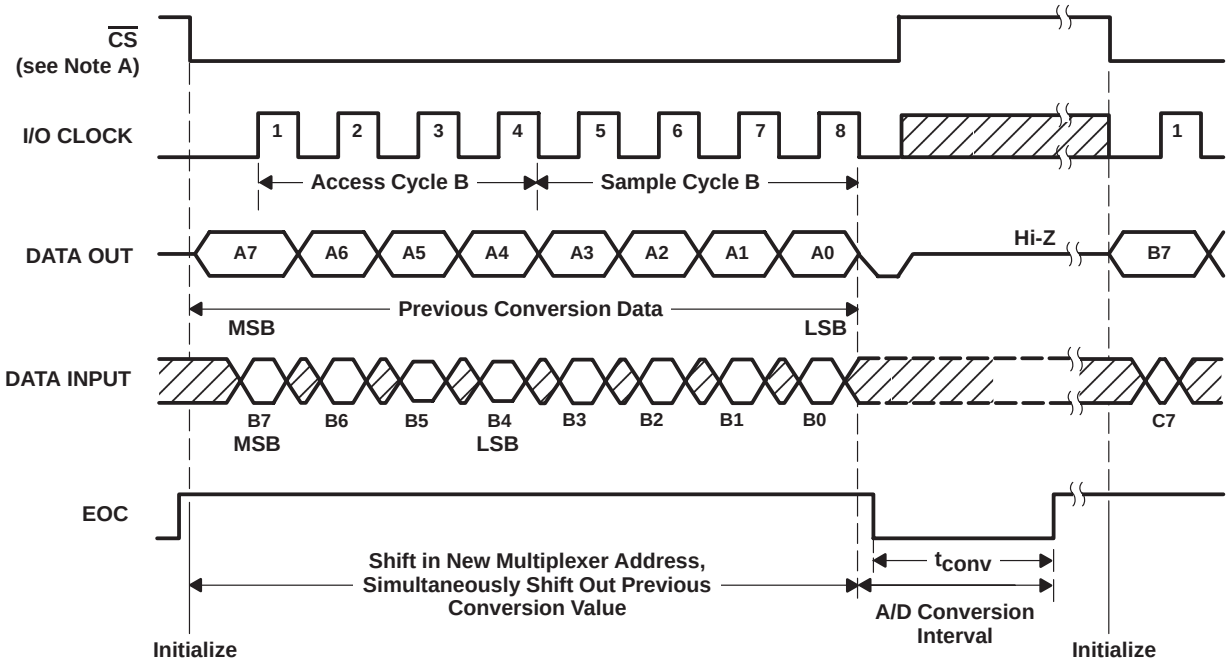
Figure 9. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

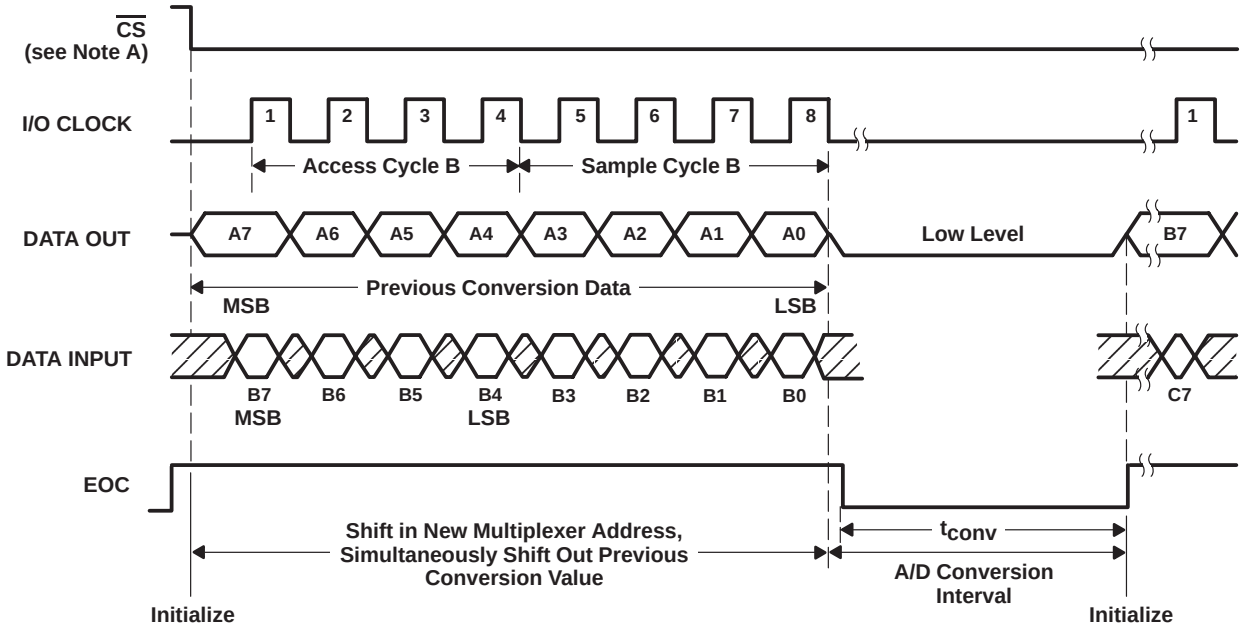
Figure 10. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

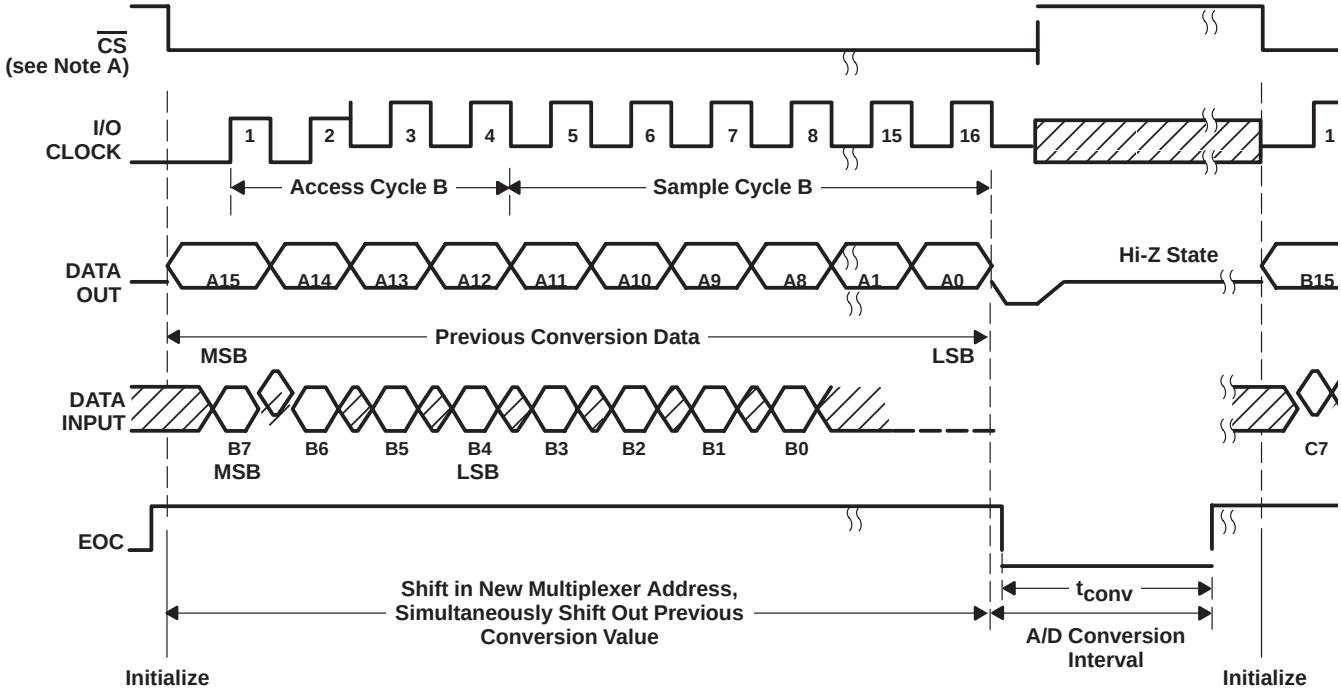
Figure 11. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

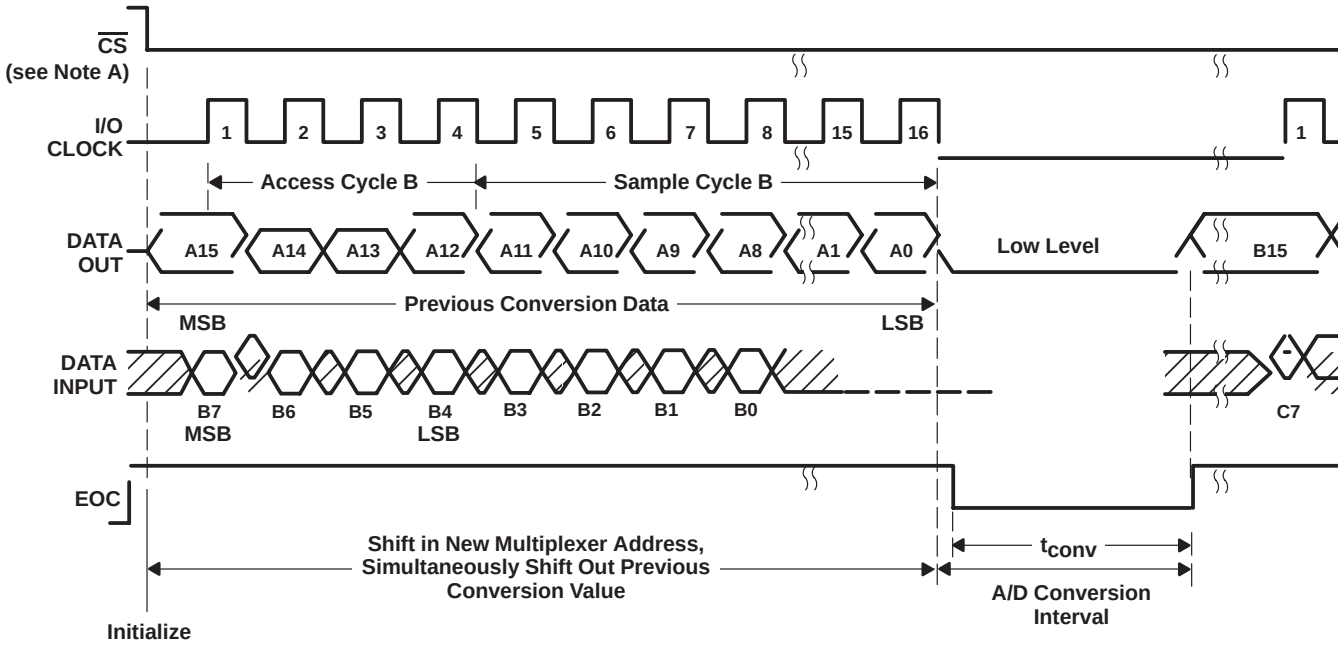
Figure 12. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First

PARAMETER MEASUREMENT INFORMATION



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 13. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

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