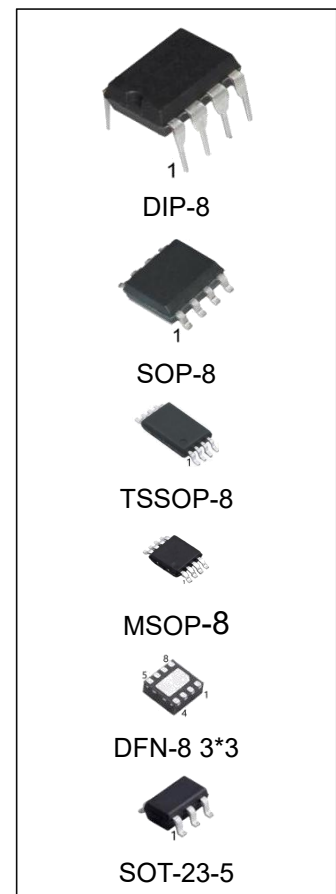


## Features

- Single supply voltage and high speed:
  - 1 MHz clock from 1.7 V to 5.5 V
- Operating Temperature range:
  - 40°C to +85°C
- Compatible with all I<sup>2</sup>C bus mode:
  - 100kHz
  - 400kHz,
  - 1MHz
- Memory Array:
  - 128Kbit EEPROM
  - 256 Pages
  - Page size: 64 byte
- Schmitt Trigger based noise filter for input noise suppression
- Current, Random and Sequential Read modes
- Write Operations:
  - Byte write within 5 ms
  - Page write within 5 ms
  - Partial Page-writes support
  - Self-Timed Write Cycle
- Hardware write protection for the whole memory array
- ESD: HBM up to 4KV
- High Reliability:
  - More than 1 million Write Endurance Cycles
  - More than 100 years Data Retention
- Package: SOP-8, TSSOP-8, DFN-8, DIP-8, MSOP-8, SOT-23-5



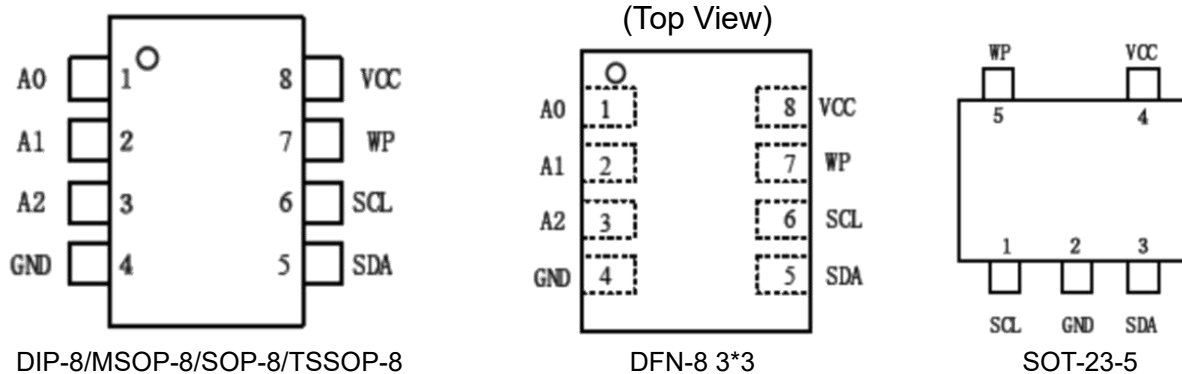
## Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG24C128BN	DIP-8	24C128B	TUBE	2000pcs/box
HG24C128BM/TR	SOP-8	24C128B	REEL	2500pcs/reel
HG24C128BMT/TR	TSSOP-8	24C128B	REEL	2500pcs/reel
HG24C128BMM/TR	MSOP-8	C128B	REEL	3000pcs/reel
HG24C128BDQ/TR	DFN-8 3*3	C128B	REEL	2500pcs/reel
HG24C128BM5/TR	SOT-23-5	C128B	REEL	3000pcs/reel

## Overview

HG24C128B is a standalone I<sup>2</sup>C compatible Serial EEPROM chip. The total memory array density is 128K bits, which is composed of 256 pages with 64bytes per page.

## Pin Description



Pin No.	Pin Name	I/O	Definition
1	A0	I	Device Address Input. Internal Pull Down.
2	A1	I	Device Address Input. Internal Pull Down.
3	A2	I	Device Address Input. Internal Pull Down.
4	GND	-	Ground
5	SDA	I/O	Serial Address, Data input and Data output (Open drain)
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input. Internal Pull Down.
8	VCC	-	Power Supply

**Table 1 Pin Definition**

**A0/A1/A2:** The device address pin are used to select the device address. This pin can be directly connected to VCC or GND in any combination. When this pin is not connected (left floating), the input is read as zero.

**SCL:** The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL.

**SDA:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer address and data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

**WP:** when the WP pin is connected to the VCC, the entire array becomes Write Protected. When this pin is not connected (left floating), the input is read as zero.

## Block Diagram

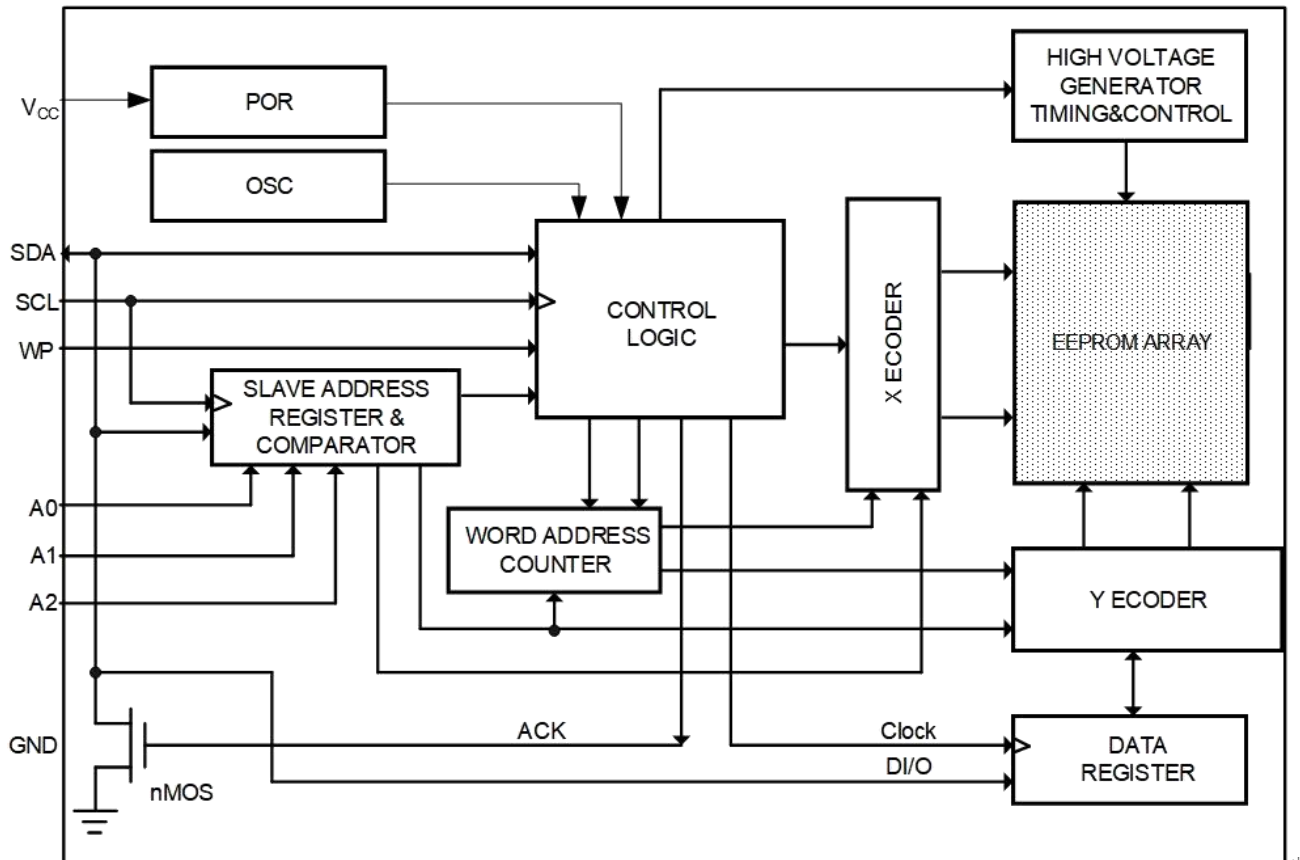


Figure 2 Function block diagram

## Device Operation

### Reset

There is an internal Power-On Reset (POR) circuit in chip to help prevent inadvertent operations during power-up and power down cycles. Before selecting the device and issuing protocol, a valid and stable supply voltage must be applied and no protocol should be issued to the device. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.

I<sup>2</sup>C Serial Interface

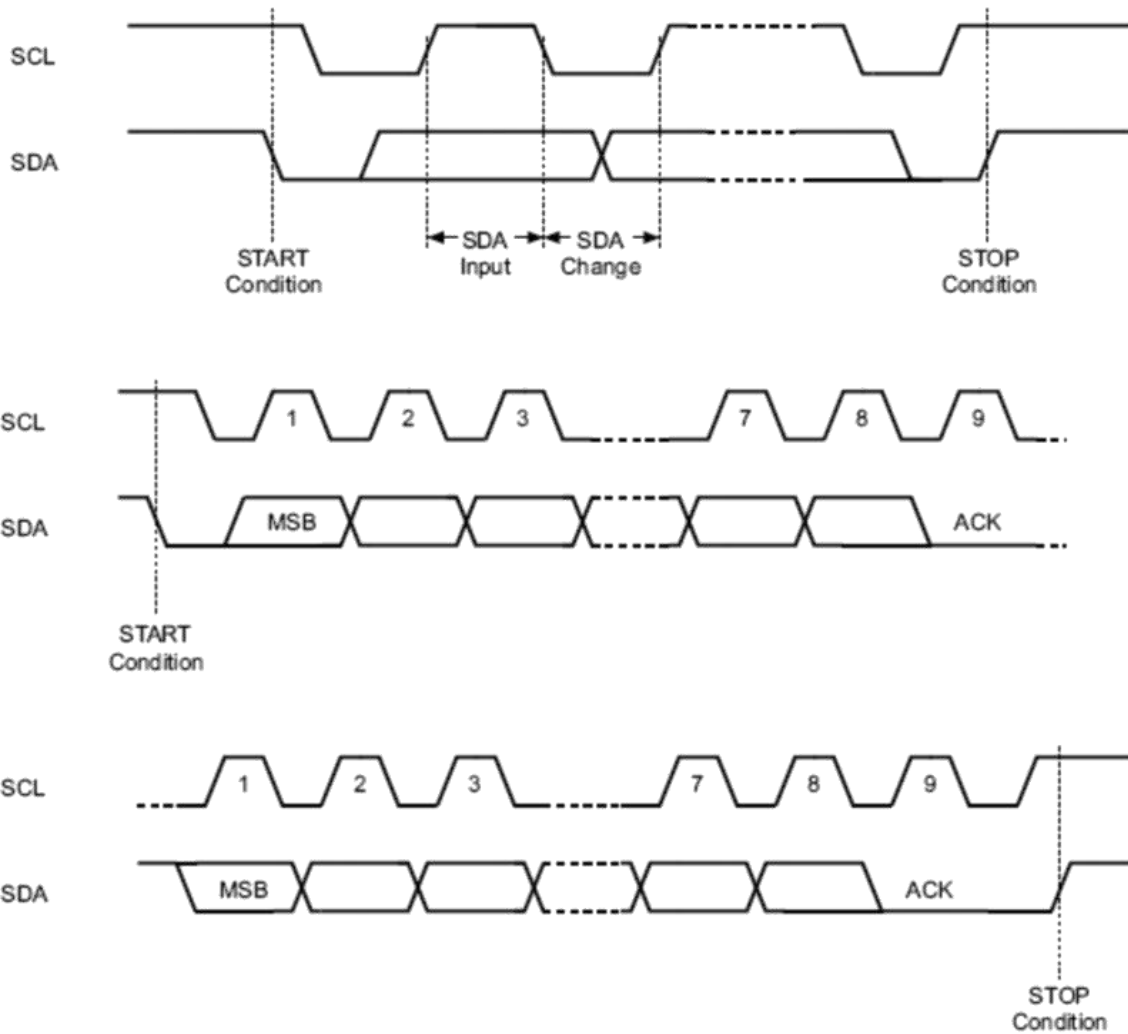


Figure 4 Serial Bus Protocol

**Start Condition**

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command..

**Data Input**

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock(SCL).

**Acknowledge**

The acknowledge bit is used to indicate a successful byte transfer. The no-acknowledge bit (NAK) is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register.

## Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven to High. A Stop condition terminates communication between the device and the bus master. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

## Standby Mode

The chip enters into standby mode during one of the following conditions:

- a) After Power-up, while no Op-code is sent;
- b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related;
- c) After the completion of any internal write operations.

## Device Address

To start communication, the bus master must initiate a Start condition. Following this, the bus master sends the device address byte with MSB first. The device address byte is comprised of a 4-bit device type identifier (DTI) followed by three software device address bits (SA2, SA1, and SA0) and a R/W bit, as described in Table 3.

Three device address bits are used to let up to eight devices can be connected on a single I<sup>2</sup>C Bus. The software device address bits must match their device address (A2, A1, A0).

If a match occurs, the corresponding device gives an acknowledgment on serial data (SDA) during the 9th bit time. If the device does not acknowledge the device select code, the device de-selects itself from the bus, and goes into standby mode (therefore will not acknowledge the device select code).

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Memory Function	Device Type Identifier				Software Device Address			(R/Wn)
Access EE Main Array	1	0	1	0	SA2	SA1	SA0	1/0
Access the Chip Configuration Register	1	0	1	0	SA2	SA1	SA0	1/0

**Table 2 Device Selection Code**

## Write Operation

The chip supports single Byte Write and Page Write operations up to the maximum page size of 64 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

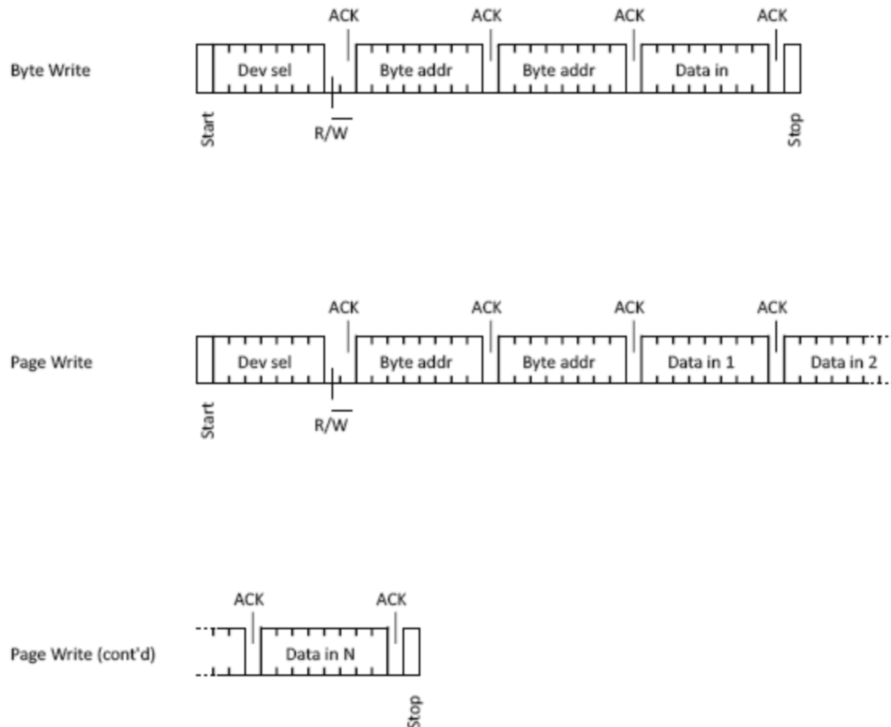


Figure 5 Write Operation Sequence

### Byte Write

Following the Start condition from the Master, the device type identifier, the device address bits and the R/W select bit (set to a Logic 0) are clocked onto the bus by the Master. The chip will respond with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the Serial EEPROM. After receiving an ACK, the Master transmits the data word to be programmed followed by an ACK from the chip. The Master ends the Write sequence with a Stop condition during the 10th clock cycle to initiate the internally self-timed write cycle. All inputs on SCL and SDA are ignored by the device during the write cycle and the device will not respond until the write cycle is complete. The Serial EEPROM will increment its internal address counter each time a byte is written.

### Page Write

A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged receipt of the first data word, the Master can transmit up to 63 more data words. The device will respond with an ACK after each data word is received. The Master must terminate the Page Write sequence with a Stop condition during the 10th clock cycle to start the write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again.

When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than one page data are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

## ACK Polling

An ACK polling routine can be implemented to optimize time sensitive applications that prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation.

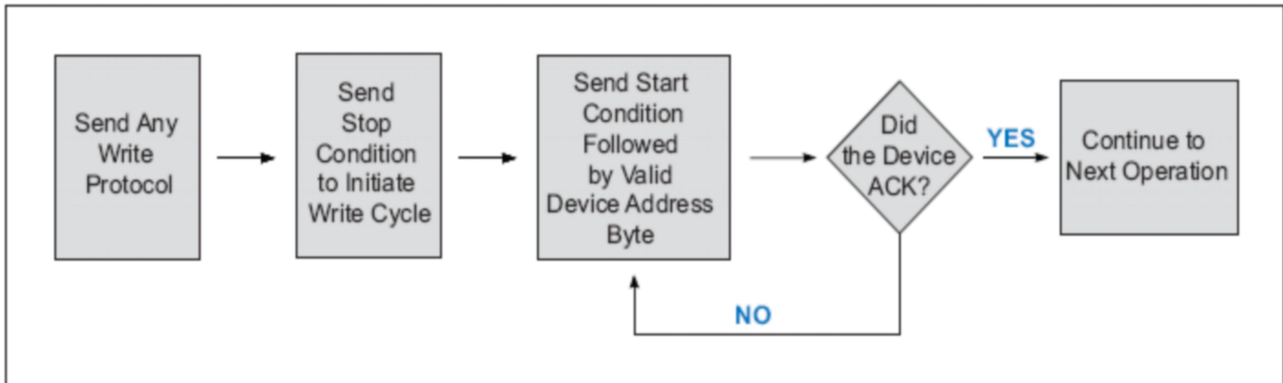


Figure 6 ACK Polling

## Write Cycle Timing

The length of the self-timed write cycle, or TWR, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the chip that it subsequently responds to with an ACK.

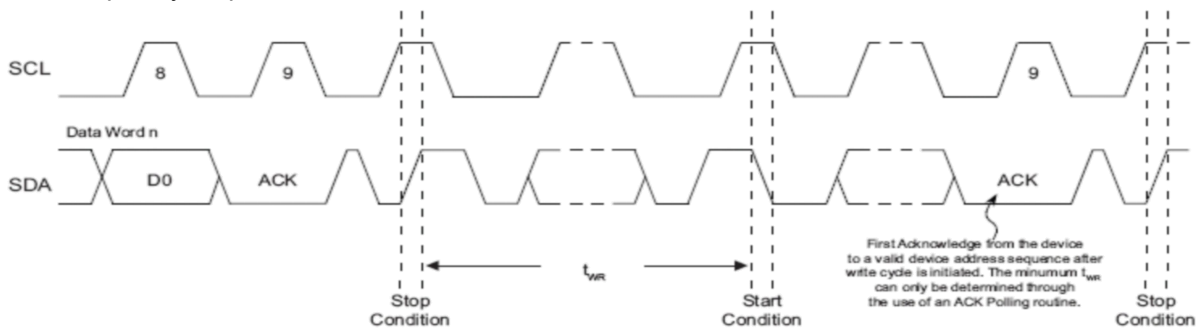


Figure 7 Write Cycle Timing

## Read Operation

All memory data Read operations are initiated by the Master transmitting a Start bit, a device type identifier of '1010', three software address bits (A2, A1, A0) that match their corresponding configurable device address (CDA2,CDA1,CDA0), and the R/W select bit with a Logic 1 state. In the following clock cycle, the device should respond with an ACK. The subsequent protocol depends on the type of Read operation desired.

Read operations are performed independent of the software protection state. The device has an internal address counter which is incremented each time a byte is read.

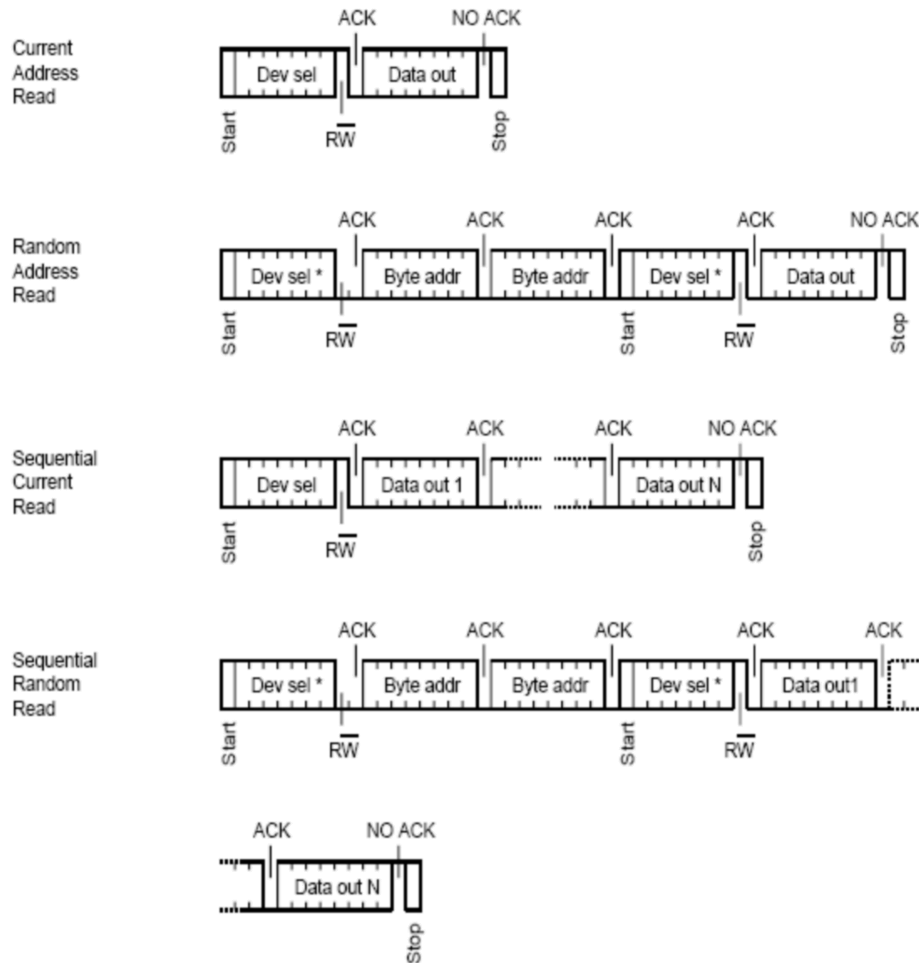


Figure 8 Read Operation Sequence

### Current Address Read

Following a Start condition, the Master only transmits the device address byte with the R/W select bit set to a Logic 1. The chip should respond with an ACK and then serially transmits the data word addressed by the internal address counter. The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as power to the device is maintained. The address roll-over during a Read is from the last byte of the last page to the first byte of the first page of the addressed 16Kbyte/8Kbyte (depends on the current address setting). To end the command, the Master does not respond with an ACK but does generate a following Stop condition.

### Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to chip as part of the dummy write sequence. Once the device address byte and data word address are clocked in and acknowledged by chip, the Master must generate another Start condition. The Master initiates a Current Address Read by sending another device address byte with the R/W select bit to a Logic 1. Then chip acknowledges the device address byte, increments its internal address counter and serially clocks out the first data word. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK and a Stop condition.



## Sequential Read

A Sequential Read operation is initiated in the same way as a Random Read operation, except after the chip transmits the first data word, the Master responds with an ACK (instead of a NACK followed by a Stop condition). As long as the chip receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words. When the internal address counter is at the last byte of the last page, the data word address will roll-over from address 0000h, and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

## Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low (NACK) during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition

## Initial Delivery State

The device is delivered with all the memory array bits set to 1.

## Electrical Characteristics

### Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to + 6.5	V
V <sub>IN</sub>	Voltage on Input Pins	-0.5 to + 6.5	V
T <sub>J(max)</sub>	Maximum Junction Temperature	150	°C
T <sub>op</sub>	Operation Temperature	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>LEAD</sub>	Update Lead Temperature	245	°C

**Table 4 Absolute Maximum Ratings**

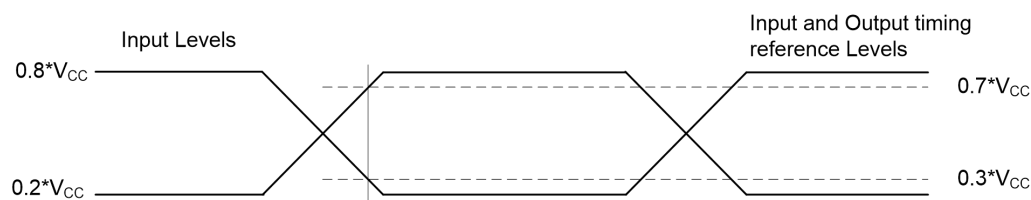
Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	--	--	6	pF
C <sub>I/O</sub>	Input / Output Capacitance	--	--	8	pF

**Table 5-Capacitance**
**AC Measurement Conditions**

Symbol	Parameter	Min	Max	Units
C <sub>L</sub>	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2*V <sub>CC</sub> to 0.8*V <sub>CC</sub>		V
	Input and output timing reference levels	0.3*V <sub>CC</sub> to 0.7*V <sub>CC</sub>		V

**Table 6 AC Measurement Conditions**

**Figure 10 AC Measurement Condition**
**DC Electrical Characteristic**

V<sub>CC</sub> = 1.7V to 5.5V, T<sub>amb</sub> = -40 °C to +85 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage current(SCL, SDA)	V <sub>IN</sub> =V <sub>CC</sub> or GND	--	2	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> =V <sub>CC</sub> or GND, SDA in Hi-Z	--	2	μA
I <sub>CC1</sub>	Write Supply current	V <sub>CC</sub> =5.5V, f <sub>c</sub> =400KHz	--	1	mA
I <sub>CC2</sub>	Read Supply current	V <sub>CC</sub> =5.5V, f <sub>c</sub> =400KHz	--	0.2	mA
I <sub>SB1</sub>	Standby supply current	V <sub>IN</sub> =V <sub>CC</sub> , V <sub>CC</sub> =3.0V	--	1	μA
V <sub>CC</sub>	Supply Voltage		1.7	5.5	V
V <sub>IH</sub>	Input High Voltage	SCL, SDA	0.7* V <sub>CC</sub>	V <sub>CC</sub> +1	V
V <sub>IL</sub>	Input Low Voltage	SCL, SDA	-0.5	0.3* V <sub>CC</sub>	V
V <sub>OL1</sub>	Output Low Voltage	V <sub>CC</sub> =1.7V, SDA, I <sub>OL</sub> =0.2mA	--	0.2	V
V <sub>OL2</sub>		V <sub>CC</sub> =3.0V, SDA I <sub>OL</sub> =2mA	--	0.4	

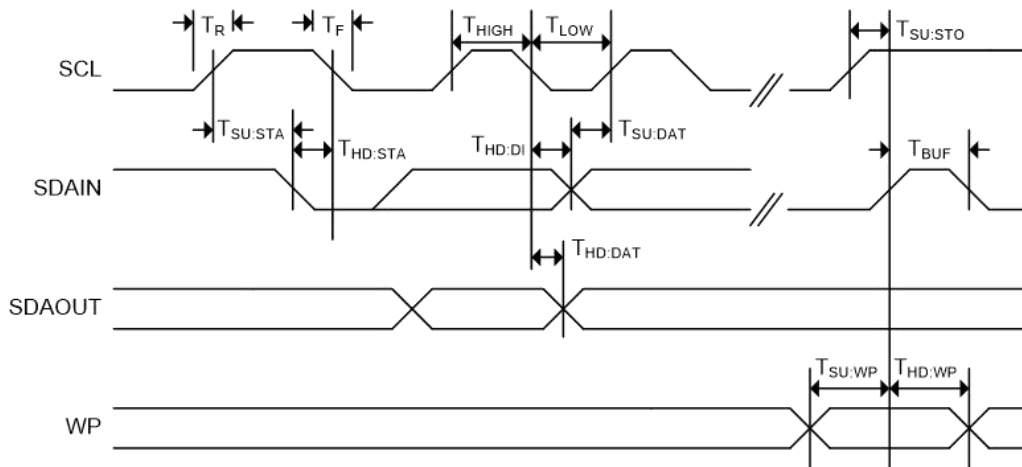
**Table 10 DC Electrical Characteristics**

**AC Electrical Characteristic**

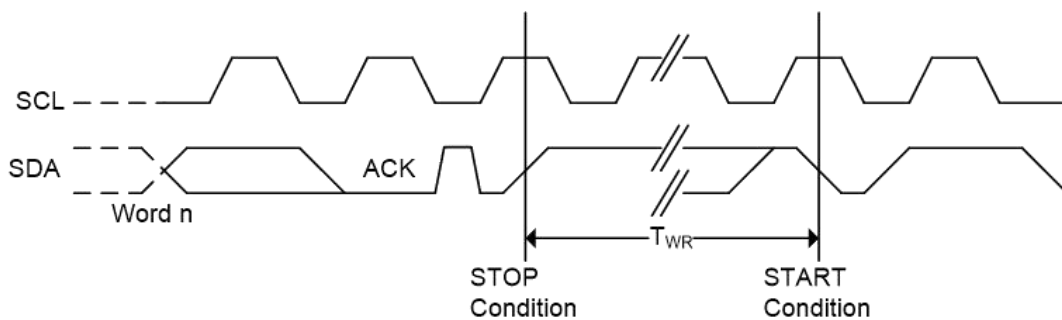
$V_{CC} = 1.7V$  to  $5.5V$ ,  $T_{amb} = -40\sim+85^{\circ}C$ , unless otherwise specified

Symbol	Parameter	$V_{CC}\geq 1.7V$				Unit
		400KHz		1000KHz		
		Min.	Max.	Min.	Max.	
$F_{SCL}$	SCL clock frequency	-	400	-	1000	kHz
$T_{LOW}$	Low period of SCL clock	1300		400		ns
$T_{HIGH}$	High period of SCL clock	600		400		ns
$T_{BUF}$	Bus free time between a Stop and a Start conditions	1300		500		ns
$T_{SU;STA}$	Start condition Setup time	600		260		ns
$T_{HD;STA}$	Start condition Hold time	600		260		ns
$T_{SU;STO}$	Stop condition Setup time	600		260		ns
$T_{SU;DAT}$	Data In Setup time	100		50		ns
$T_{HD;DI}$	Data In Hold time	0		0		ns
$T_{HD;DAT}$	Data Out Hold Time	100	-	0	-	ns
$T_W$	Write Cycle		5		5	ms
$T_R$	Rise time of SDA	-	300	--	120	ns
$T_F$	Fall time of SDA	-	300	--	120	ns
$T_N$	Noise Suppression Time	-	100	-	50	ns

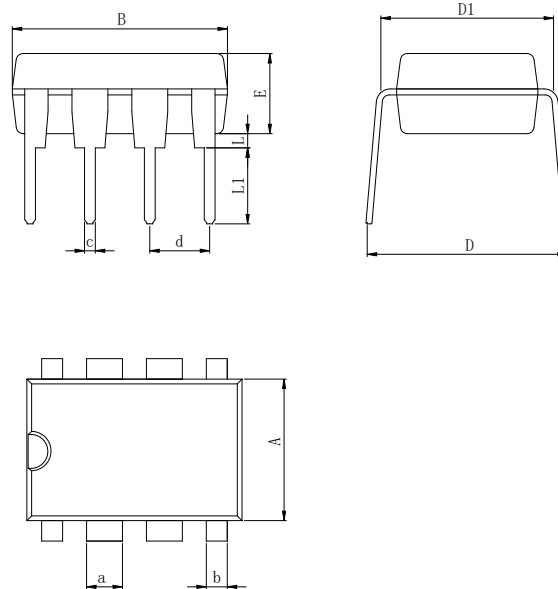
**Table 11 AC Electrical Characteristic**



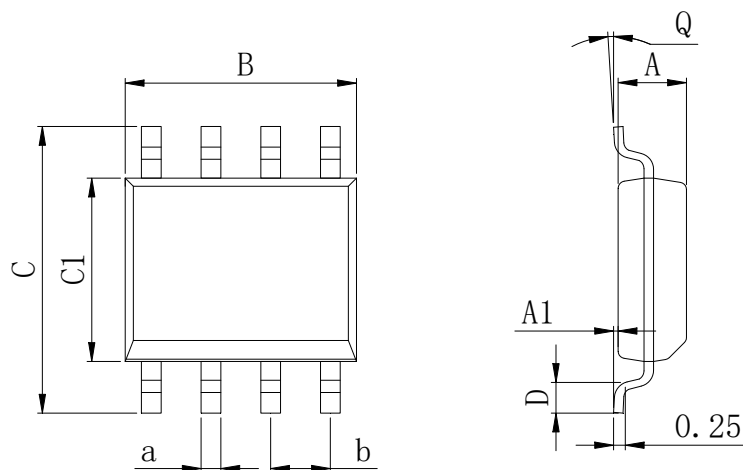
**Figure 11 Bus Timing**



**Figure 12 Write Cycle Timing**

**Physical Dimensions**
**DIP-8**

**Dimensions In Millimeters(DIP-8)**

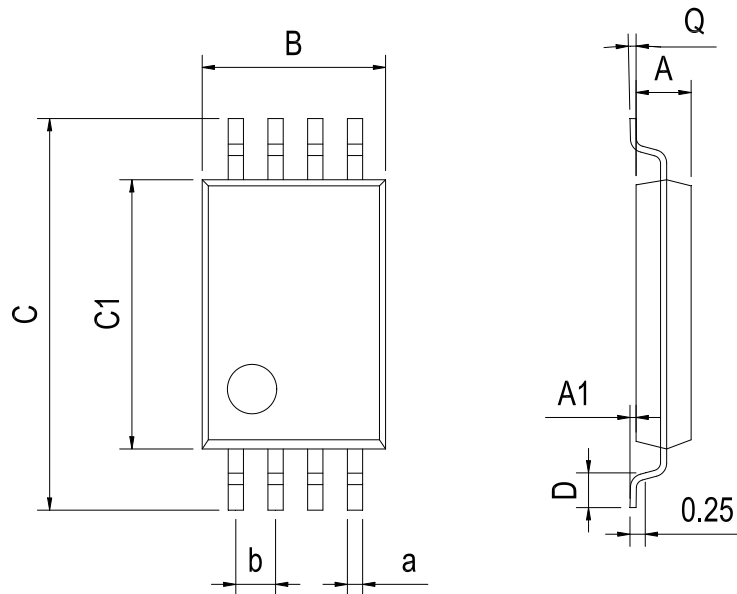
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

**SOP-8 (150mil)**

**Dimensions In Millimeters(SOP-8)**

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

## Physical Dimensions

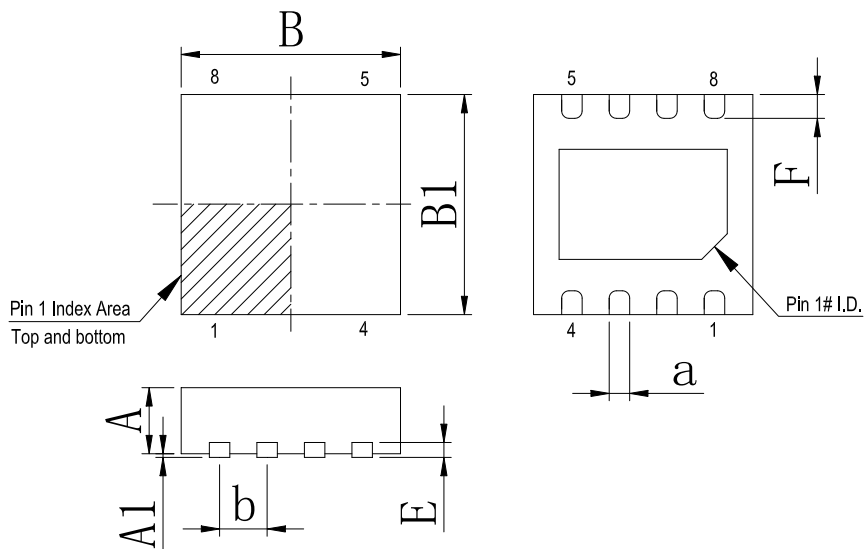
TSSOP-8 (4.4\*3.0)



Dimensions In Millimeters(TSSOP-8)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	2.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	3.10	6.60	4.50	0.80	8°	0.25	

DFN-8 3\*3

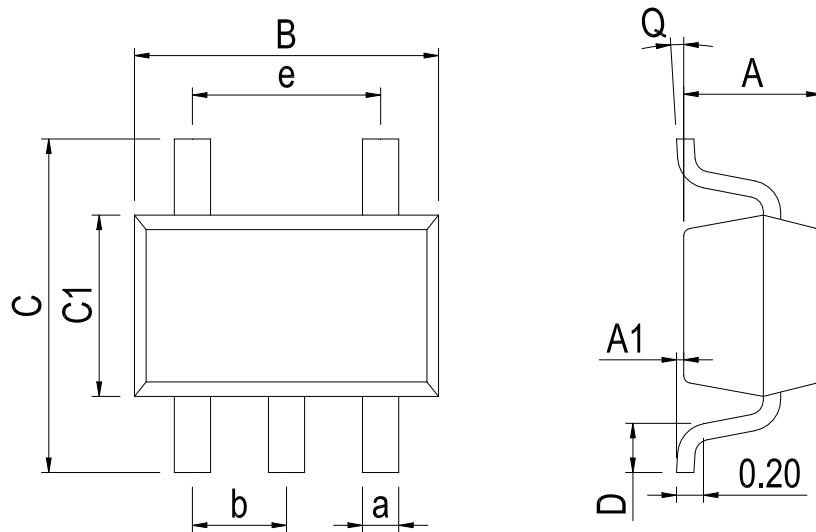


Dimensions In Millimeters(DFN-8 3\*3)

Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

## Physical Dimensions

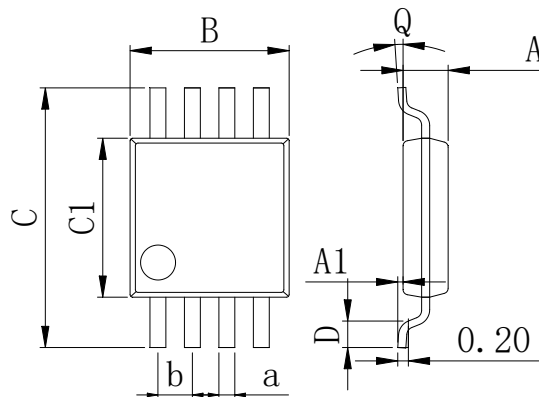
SOT-23-5



Dimensions In Millimeters(SOT-23-5)

Symbol:	A	A1	B	C	C1	D	Q	a	b	e
Min:	1.05	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC	1.90 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.40		

MSOP-8



Dimensions In Millimeters(MSOP-8)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

## Revision History

DATE	REVISION	PAGE
2015-7-8	New	1-16
2024-7-16	Document Reformatting	1-16

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