65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range

Features

- Bus-Pin Fault Protection to:
  - > ±70 V ('HVD1785, 86, 91, 92)
  - > ±30 V ('HVD1787, 93)
- Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
  - ±16 kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1 µA Typical
  - I_{CC} 5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

Applications

- Designed for RS-485 and RS-422 Networks

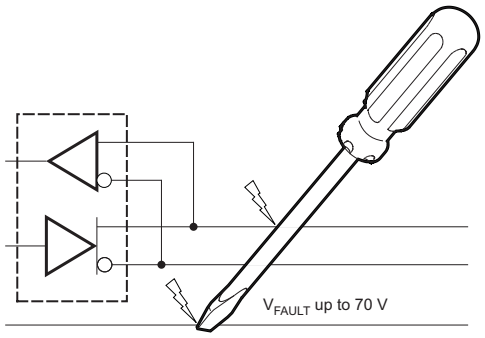
Description

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1785, 'HVD1786, and 'HVD1787, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the 'HVD1793, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. These ports feature a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 105°C.

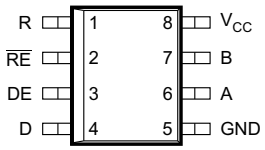
For similar features with 3.3-V supply operation, see the 65HVD1781 (SLLS877).

Example of Bus Short to Power Supply



Pin Configuration and Functions

D or P Package
8-Pin SOIC or PDIP
65HVD1785, 1786, 1787 Top View

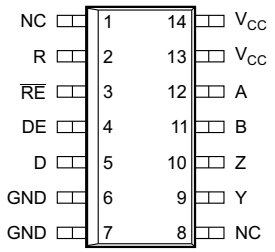


Pin Functions (65HVD1785, 65HVD1786, 65HVD1787)

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V-to-5.5-V supply

Pin Configuration and Functions

D Package
14-Pin SOIC
65VD1791, 1792, 1793 Top View



NC - No internal connection
Pins 6 and 7 are connected together internally.
Pins 13 and 14 are connected together internally.

Pin Functions (65HVD1791, 65HVD1792, 65HVD1793)

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	12	Bus input	Receiver input (complementary to B)
B	11	Bus input	Receiver input (complementary to A)
Y	9	Bus output	Driver output (complementary to Z)
Z	10	Bus output	Driver output (complementary to Y)
D	5	Digital input	Driver data input
DE	4	Digital input	Driver enable, active high
GND	6, 7	Reference potential	Local device ground
R	2	Digital output	Receive data output
$\overline{RE}$	3	Digital input	Receiver enable, active low
V_{CC}	13, 14	Supply	4.5-V to 5.5-V supply
NC	1, 8	No connect	No connect; should be left floating

Absolute Maximum Ratings(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			–0.5	7	V
	Voltage at bus pins	'HVD1785, 86, 91, 92, 93	A, B pins	–70	70	V
		'HVD1787	A, B pins	–70	30	V
		'HVD1793	Y, Z pins	–70	30	V
	Input voltage at any logic pin			–0.3	V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485			–100	100	V
	Receiver output current			–24	24	mA
T_J	Junction temperature				170	°C
T_{stg}	Storage temperature				160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1), JEDEC Standard 22, Test Method A114	Bus terminals and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2), JEDEC Standard 22, Test Method C101		±2000	
		Machine Model, JEDEC Standard 22, Test Method A115		±400	
		IEC 60749-26 ESD (human-body model)	Bus terminals and GND	±16000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–20		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD1785, HVD1791			115	kbps
		HVD1786, HVD1792			1	Mbps
		HVD1787, HVD1793			10	
T_A	Operating free-air temperature (see application section for thermal information)		–40		105	°C
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

Thermal Information

THERMAL METRIC(1)		65HVD1785, 65HVD1786, 65HVD1787		65HVD1791, 65HVD1792, 65HVD1793	UNIT
		D (SOIC)	P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138	59	95	°C/W
$R_{\theta JA\ (low\text{-}K)}$	Junction-to-case (top) thermal resistance	242	128	168	°C/W
$R_{\theta JC(top)}$	Junction-to-board thermal resistance	61	61	44	°C/W
$R_{\theta JB}$	Junction-to-top characterization parameter	62	39	40	°C/W
ψ_{JT}	Junction-to-board characterization parameter	3.4	17.6	8.2	°C/W
ψ_{JB}	Junction-to-case (bottom) thermal resistance	33.4	28.3	25	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	RS-485 with common-mode load, V_{CC} > 4.75 V, see Figure 5	T_A ≤ 85°C		1.5			V
			T_A ≤ 105°C		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			2	2.5		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–100	0	100	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, see Figure 6				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold	V_{CM} = –20 V to 25 V				–100	–10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–200	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-})				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
		I_{OH} = –400 µA			4			
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	T_A ≤ 85°C			0.2	0.4	V
			T_A ≤ 105°C			0.2	0.5	
I_I	Driver input, driver enable, and receiver enable input current				–100		100	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	85, 86, 91, 92	V_I = 12 V		75	125	µA
				V_I = –7 V	–100	–40		
			87, 93	V_I = 12 V			500	
				V_I = –7 V	–400			
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load			4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load			3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load			2	4	
		Driver and receiver disabled	DE = GND, D = open RE = V_{CC}, no load			0.5	5	µA
	Supply current (dynamic)	See *Typical Characteristics*						

Thermal Considerations

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D Power dissipation	85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated (1)	290	mW
	85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load (1)	320	
	86			
	87			
	85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load (1)	400	
	86			
	87			
T_{SD} Thermal-shutdown junction temperature			170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD1785, 1791 at 115 kbps, HVD1786 at 1 Mbps, HVD1787 at 10 Mbps)

Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (HVD1785 AND HVD1791)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7		0.4	1.7	2.6	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8 and Figure 9		0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	3	µs
		Receiver disabled			3	12	
DRIVER (HVD1786 AND HVD1792)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					25	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8 and Figure 9			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				10	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns
DRIVER (HVD1787 AND HVD1793)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7		3		30	ns
t_{PHL}, t_{PLH}	Driver propagation delay					50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8 and Figure 9			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				9	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns

Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, see Figure 10			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		85, 86, 91, 92		100	200	ns
			87, 93			70	
$t_{SK(P)}$	Receiver output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		85, 86, 91, 92		6	20	ns
			87, 93			5	
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, see Figure 11			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, see Figure 11			80	300	ns
		Driver disabled, see Figure 12			3	9	µs

Typical Characteristics

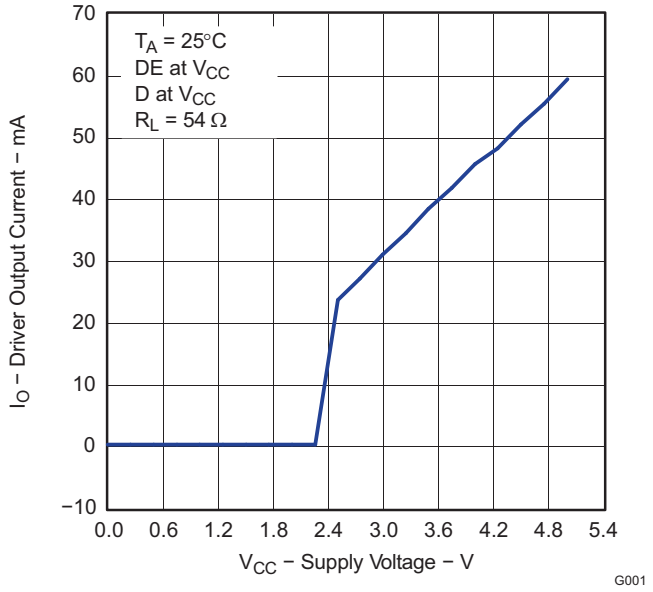


Figure 1. Driver Output Current vs Supply Voltage

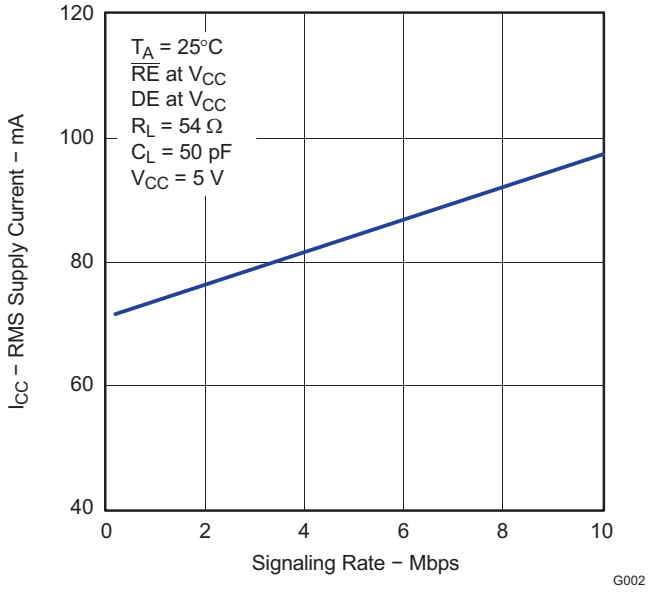


Figure 2. HVD1787 RMS Supply Current vs Signaling Rate

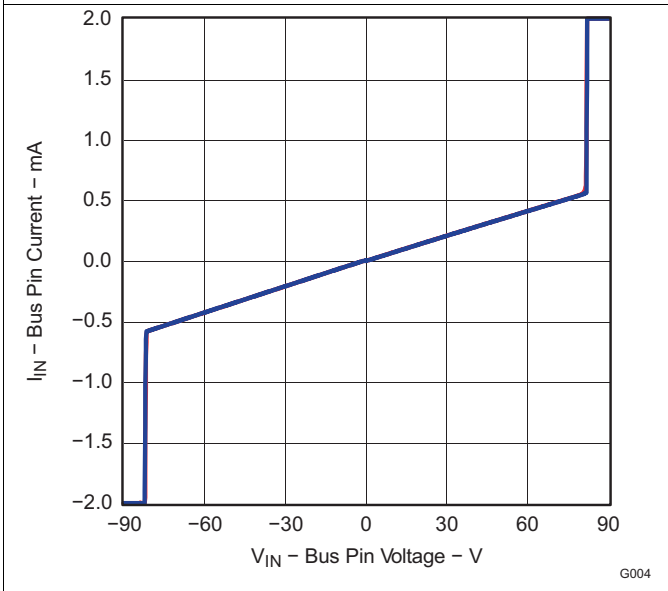


Figure 3. Bus Pin Current vs Bus Pin Voltage

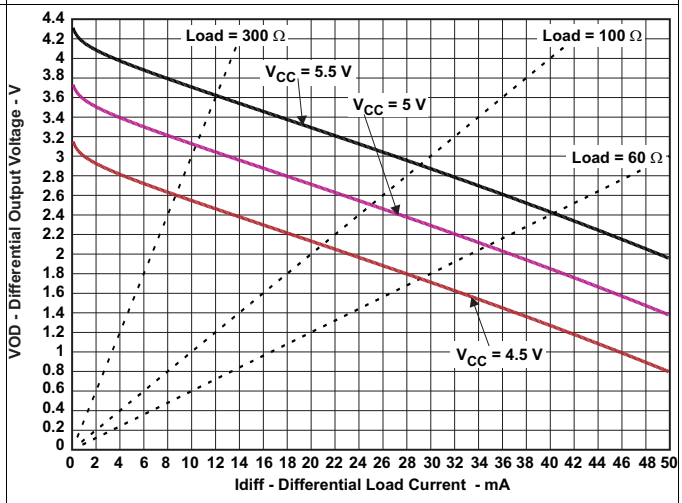


Figure 4. Differential Output Voltage vs. Differential Load Current

Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

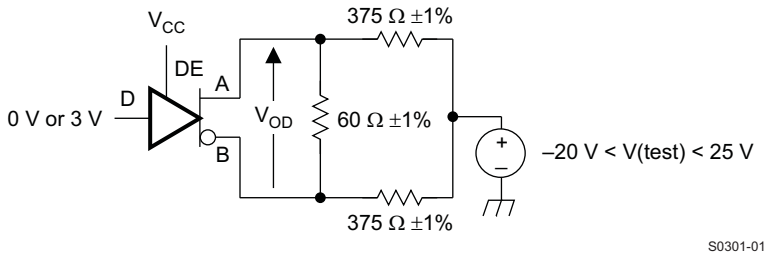


Figure 5. Measurement of Driver Differential Output Voltage With Common-Mode Load

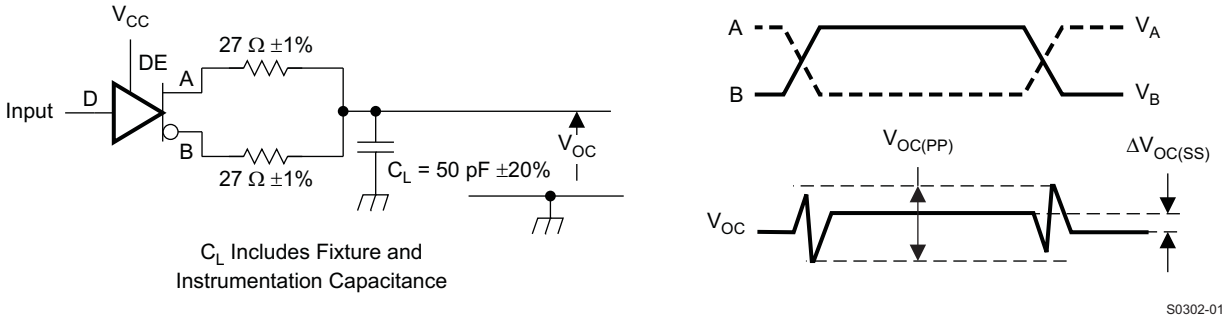


Figure 6. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

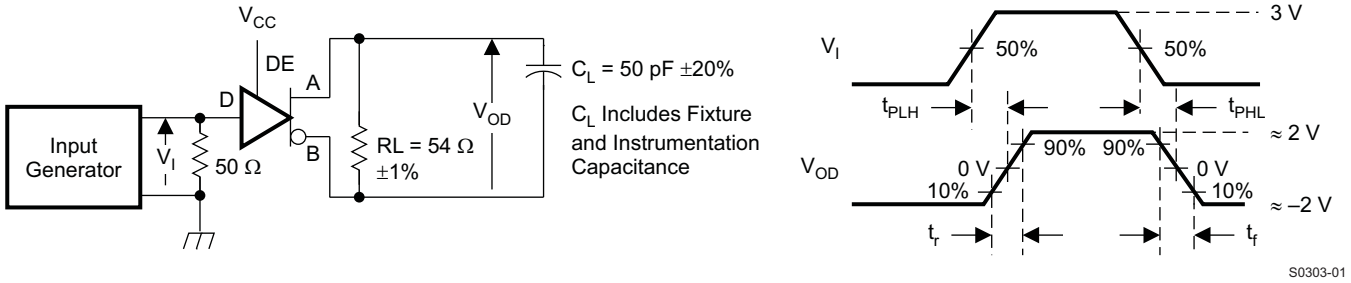
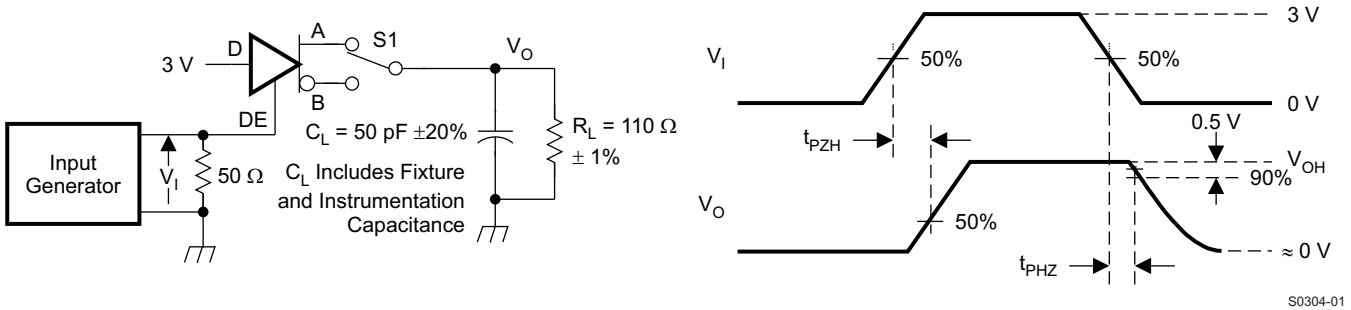


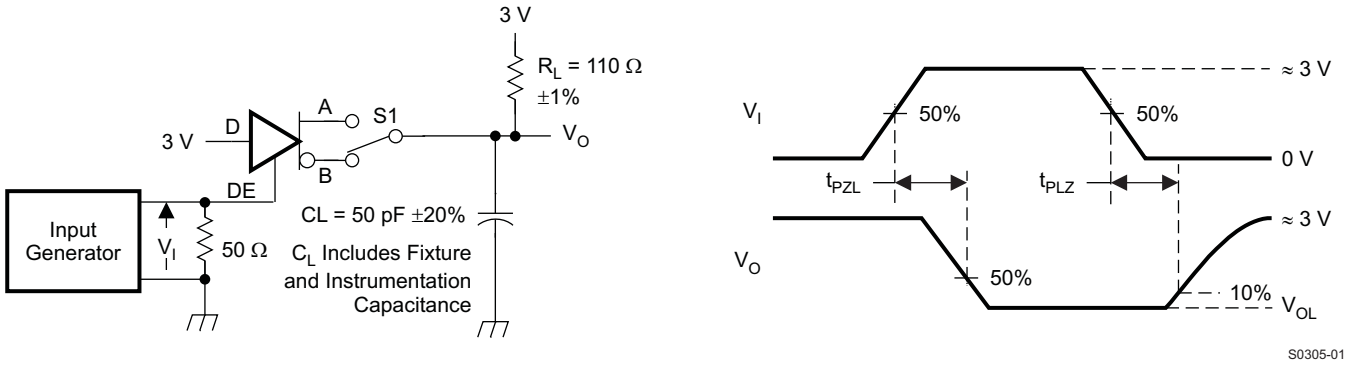
Figure 7. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 8. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

Parameter Measurement Information (continued)



NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

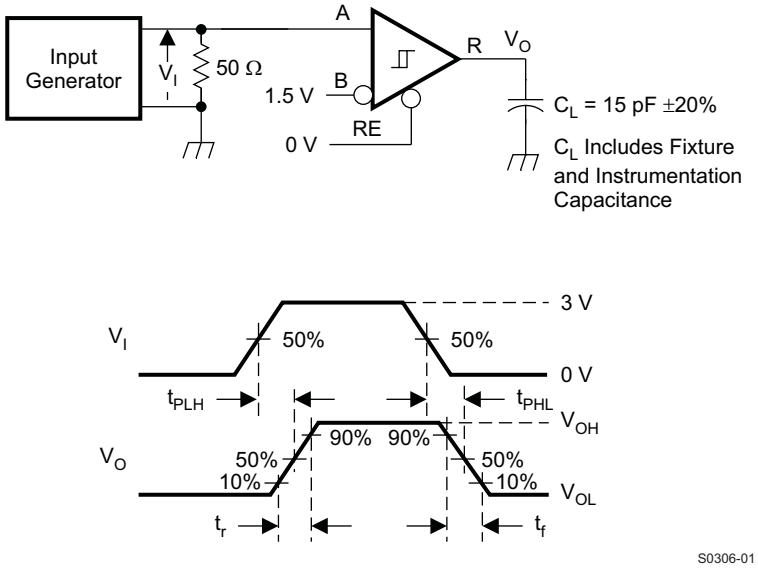


Figure 10. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

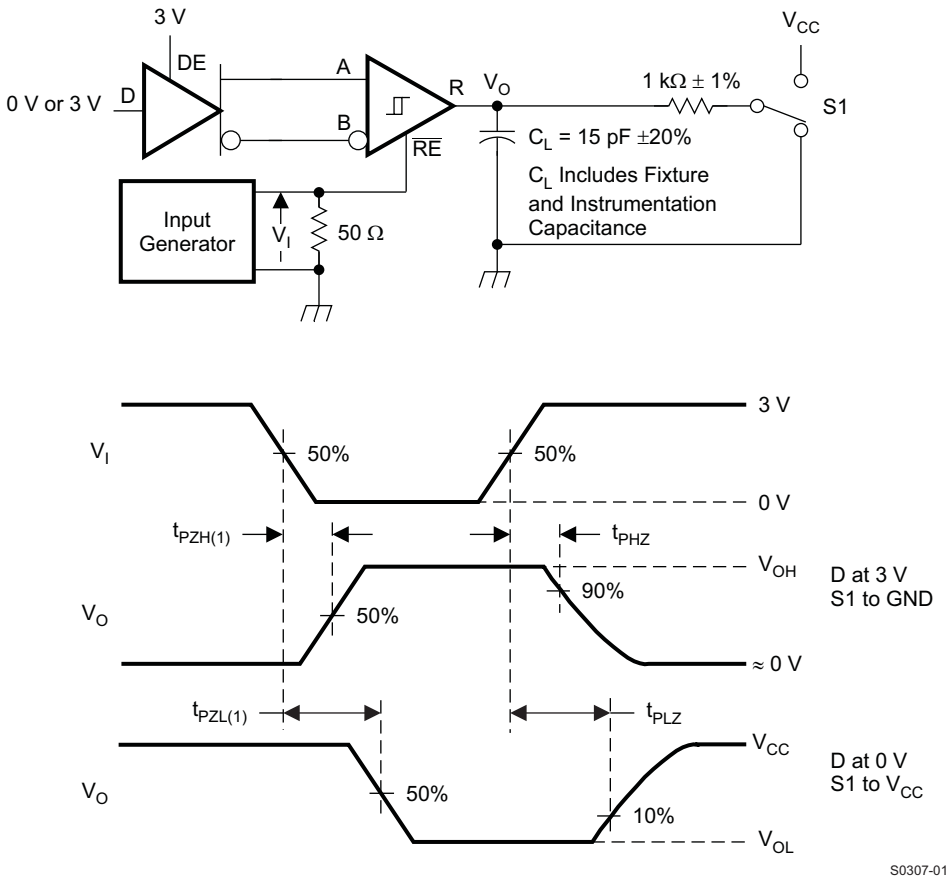


Figure 11. Measurement of Receiver Enable/Disable Times With Driver Enabled

Parameter Measurement Information (continued)

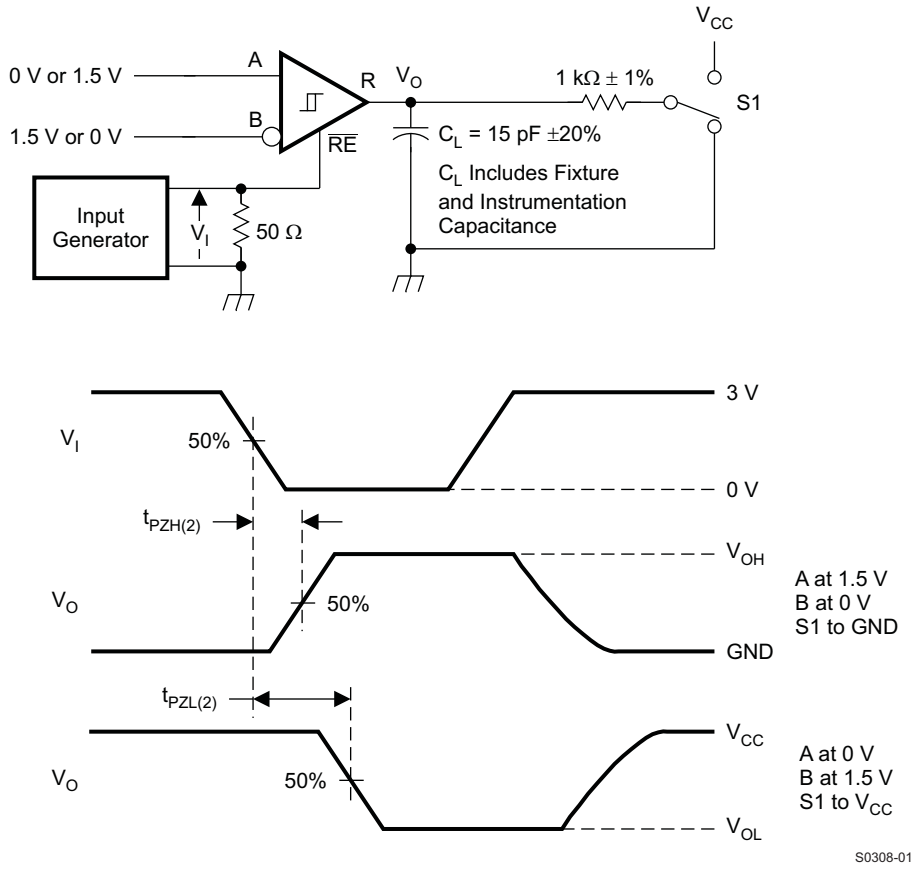


Figure 12. Measurement of Receiver Enable Times With Driver Disabled

Detailed Description

Overview

The 65HVD17xx family of RS-485 transceivers are designed to operate up to 115 kbps (HVD1785 and HVD1791), 1 Mbps (HVD1786 and HVD1792), or 10 Mbps (HVD1787 or HVD1793) and to withstand DC overvoltage faults on the bus interface pins. This helps to protect the devices against damages resulting from direct shorts to power supplies, cable mis-wirings, connector failures, or other common faults.

The 65HVD178x devices are half-duplex, and thus have the transmitter and receiver bus interfaces connected together internally. The 65HVD179x family leaves these two interfaces separate, allowing for full-duplex communication. The low receiver loading allows for up to 256 nodes to share a common RS-485 bus. The devices feature a wide common-mode range as well as fail-safe receivers, which ensure a stable logic-level output during bus open, short, or idle conditions.

Functional Block Diagram

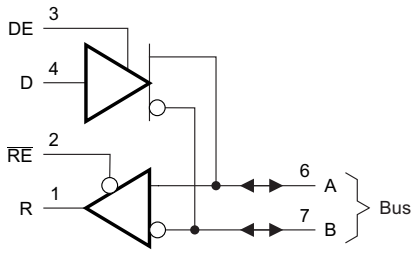


Figure 13. Half-Duplex Transceiver

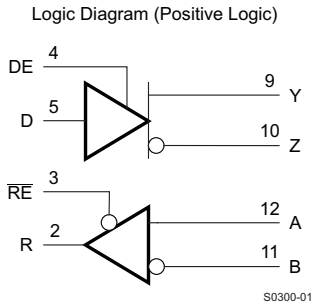


Figure 14. Full Duplex Transceiver

Feature Description

Hot-Plugging

These devices are designed to operate in hot swap or hot pluggable applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 1, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in *Device Functional Modes*, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

Feature Description (continued)

Receiver Failsafe

The differential receiver is *failsafe* to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the HVD17xx family of RS-485 devices, receiver failsafe is accomplished by offsetting the receiver thresholds so that the "input indeterminate" range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The HVD17xx receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. In the *Electrical Characteristics* table, V_{IT-} has a typical value of –150 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of V_{IT+} is -100mV, and V_{IT+} is never more positive than -10 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

For the HVD17xx devices, the typical noise immunity is typically about 150 mV, which is the negative noise level needed to exceed the V_{IT-} threshold (V_{IT-} TYP = –150 mV). In the worst case, the failsafe noise immunity is never less than 40 mV, which is set by the maximum positive threshold (V_{IT+} MAX = –10 mV) plus the minimum hysteresis voltage (V_{HYS} MIN = 30 mV).

70-V Fault-Protection

The 65HVD17xx family of RS-485 devices is designed to survive bus pin faults up to ±70V. The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND

2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR

2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Feature Description (continued)

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	LO	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	HI	L	-70V < V_A < 70V	-70V < V_B < 30V	Device survives
ON	HI	L	-70V < V_A < 70V	30V < V_B	Damage may occur
ON	HI	H	-70V < V_A < 30V	-70V < V_B < 30V	Device survives
ON	HI	H	30V < V_A	-70V < V_B < 30V	Damage may occur

Additional Options

The 65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard 65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring.

Table 2. 65HVD17xx Options for J1708 Applications

PART NUMBER	65HVD17xx		
FOOTPRINT/FUNCTION	SLOW	MEDIUM	FAST
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10

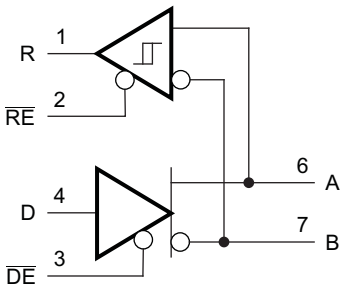


Figure 15. 65HVD1708E Transceiver for J1708 Applications

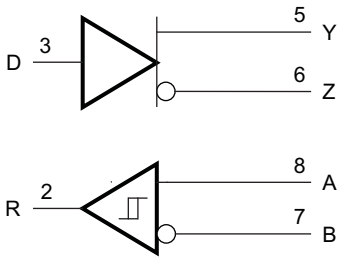


Figure 16. 65HVD17xx Always-Enabled Driver Receiver

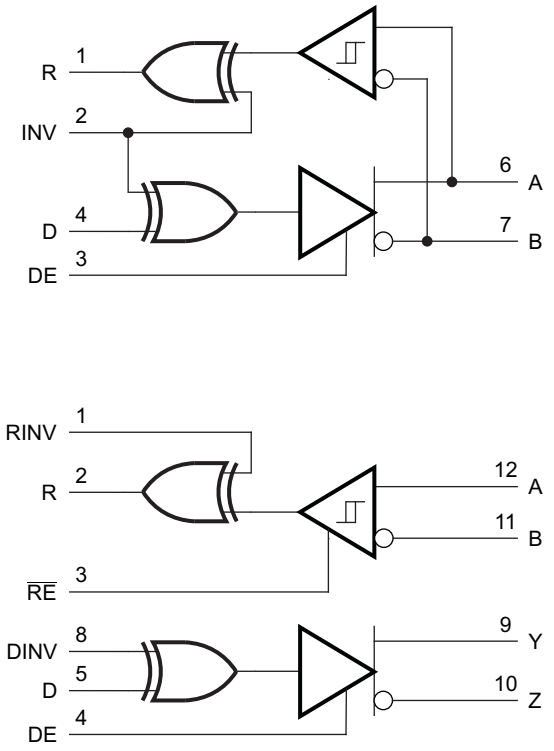


Figure 17. 65HVD17xx Options With Inverting Feature to Correct for Miswired Cables

Device Functional Modes

Table 3. Driver Function Table

INPUT	ENABLE	OUTPUTS		
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

Table 4. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Application Information

The 65HVD17xx family consists of both half-duplex and full-duplex transceivers that can be used for asynchronous data communication. Half-duplex implementations require one signaling pair (two wires), while full-duplex implementations require two signaling pairs (four wires). The driver and receiver enable pins of the 65HVD17xx family allow for control over the direction of data flow. Since it is common for multiple transceivers to share a common communications bus, care should be taken at the system level to ensure that only one driver is enabled at a time. This avoids bus contention, a fault condition in which multiple drivers attempt to send data at the same time.

Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

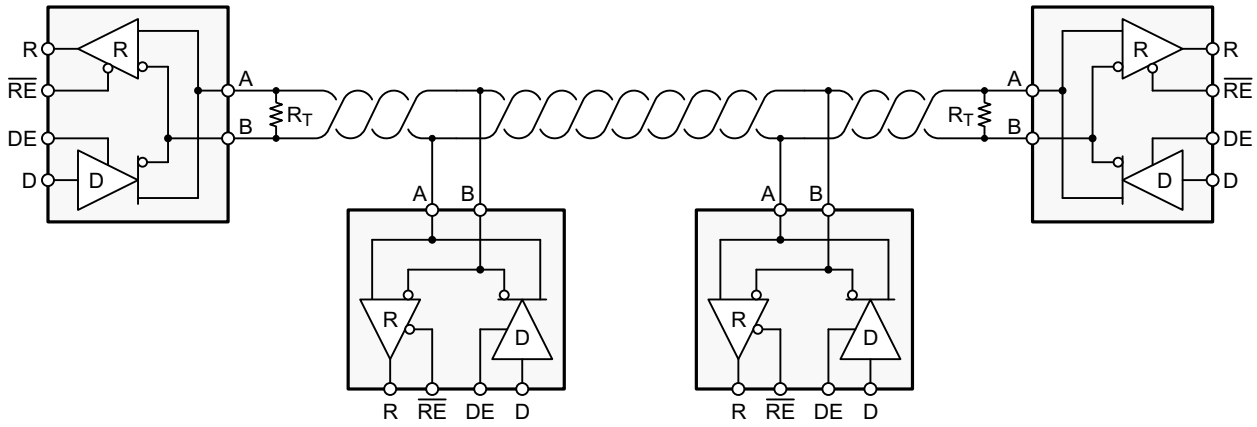


Figure 18. Typical RS-485 Network With Half-duplex Transceivers

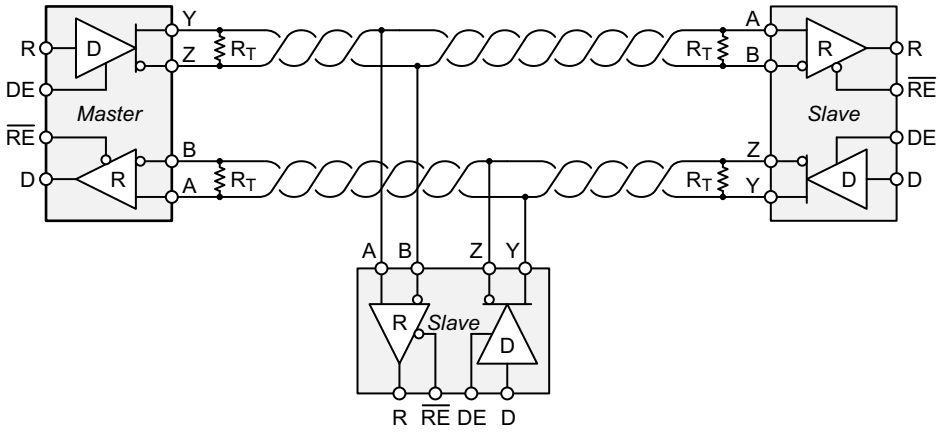


Figure 19. Typical RS-485 Network With Full-duplex Transceivers

Typical Application (continued)

Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

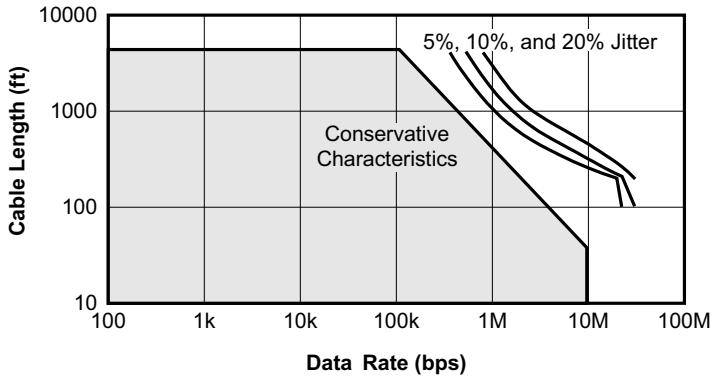


Figure 20. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (for example, 10 Mbps for the 65HVD1787 and 65HVD1793) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of *c*

Receiver Failsafe

The differential receiver of the 65HVD17xx family is *failsafe* to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

n any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Typical Application (continued)

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than +200 mV, and must output a low when VID is more negative than -200 mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$ and $V_{IT(-)}$. As shown in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a low receiver output, and differential signals more positive than +200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of -10 mV, and the receiver output will be high.

Detailed Design Procedure

Although the 65HVD17xx family is internally protected against human-body-model ESD strikes up to 16 kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

Application Curve

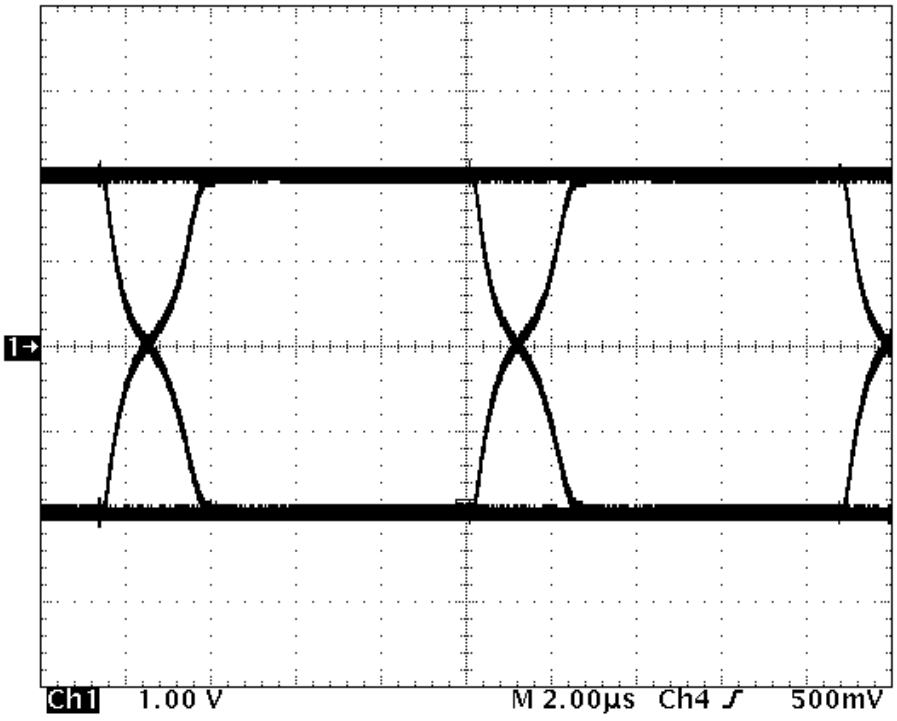


Figure 21. 65HVD1785 Differential Output at 115 kbps

Important statement:

Huaguan Semiconductor Co,Ltd. reserves the right to change the products and services provided without notice. Customers should obtain the latest relevant information before ordering, and verify the timeliness and accuracy of this information.

Customers are responsible for complying with safety standards and taking safety measures when using our products for system design and machine manufacturing to avoid potential risks that may result in personal injury or property damage.

Our products are not licensed for applications in life support, military, aerospace, etc., so we do not bear the consequences of the application of these products in these fields.

Our documentation is only permitted to be copied without any tampering with the content, so we do not accept any responsibility or liability for the altered documents.

单击下面可查看定价，库存，交付和生命周期等信息

>>HGSEMI(华冠)