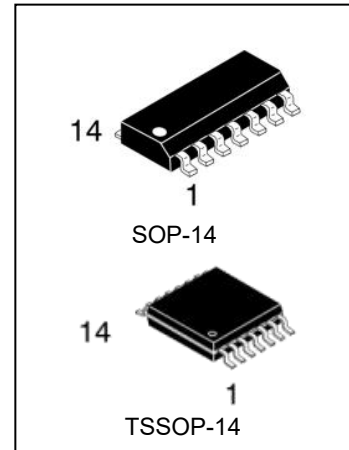


Quad 3-State Noninverting Buffers

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb-Free Devices



Ordering Information

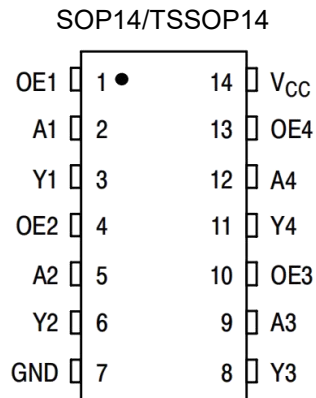
DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC125M/TR	SOP-14	74HC125	REEL	2500pcs/Reel
74HC125MT/TR	TSSOP-14	HC125	REEL	2500pcs/Reel

High-Performance Silicon-Gate CMOS

The 74HC125 is identical in pinout to the LS125. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The 74HC125 noninverting buffer is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has four separate output enables that are active-low.

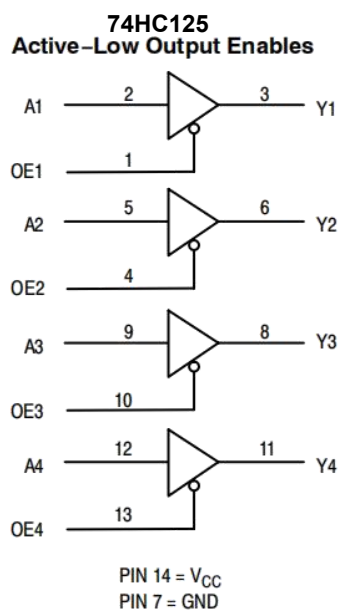
Pin Connection



Function Table

74HC125		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

Logic Diagram



Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, VCC and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, SOP Package†	500	mW
	TSSOP Package†	450	
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (SOP or TSSOP Package)	245	°C

Note: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Unused outputs must be left open. Stresses exceeding Maximum Recommended Operating Conditions may affect device reliability. †Derating – SOP Package: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 mW/°C fgs may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recrom 65° to 125°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-40	+ 85	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

Dc Electrical Characteristics (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Guaranteed Limit			Unit				
				-40 to 25°C	≤ 85°C	≤ 125°C					
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			3.0	2.1	2.1	2.1					
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V				
			3.0	0.9	0.9	0.9					
			4.5	1.35	1.35	1.35					
			6.0	1.8	1.8	1.8					
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	2.48	2.34	2.20					
			4.5	3.98	3.84	3.70					
			6.0	5.48	5.34	5.20					
			V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0		0.1	0.1	0.1	V
						4.5		0.1	0.1	0.1	
6.0	0.1	0.1				0.1					
V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26			0.33	0.40					
	4.5	0.26	0.33	0.40							
	6.0	0.26	0.33	0.40							
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA				
I _{oz}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	0.5	5.0	10	μA				
I _{cc}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	2.0	20	40	μA				

Ac Electrical Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	V_{CC} (V)	Guaranteed Limit			Unit
			-40 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	90	115	135	ns
		3.0	36	45	60	
		4.5	18	23	27	
		6.0	15	20	23	
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	120	150	180	ns
		3.0	45	60	80	
		4.5	24	30	36	
		6.0	20	26	31	
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	90	115	135	ns
		3.0	36	45	60	
		4.5	18	23	27	
		6.0	15	20	23	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	22	28	34	
		4.5	12	15	18	
		6.0	10	13	15	
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum 3-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF
CPD	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$			pF	
		30				

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^{2f} + I_{CC} V_{CC}$.

Switching Waveforms

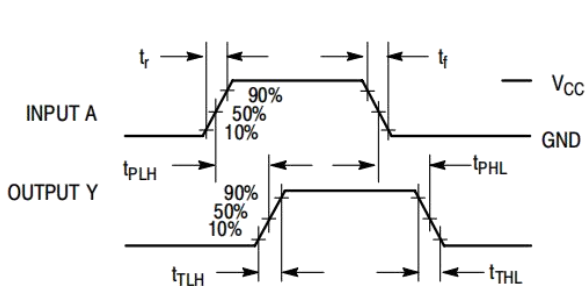


Figure 1.

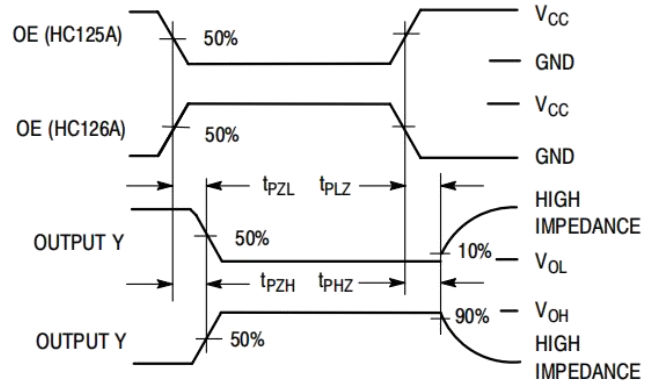
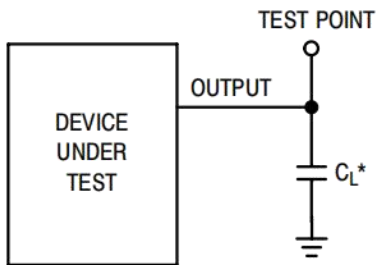
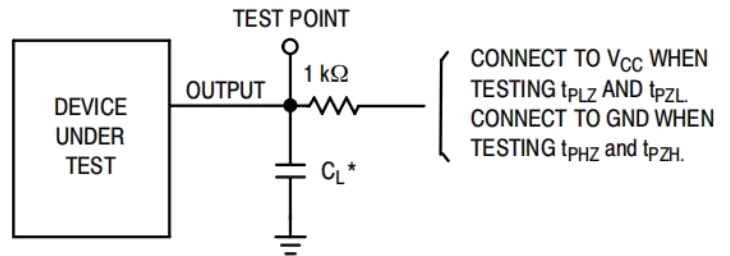


Figure 2.



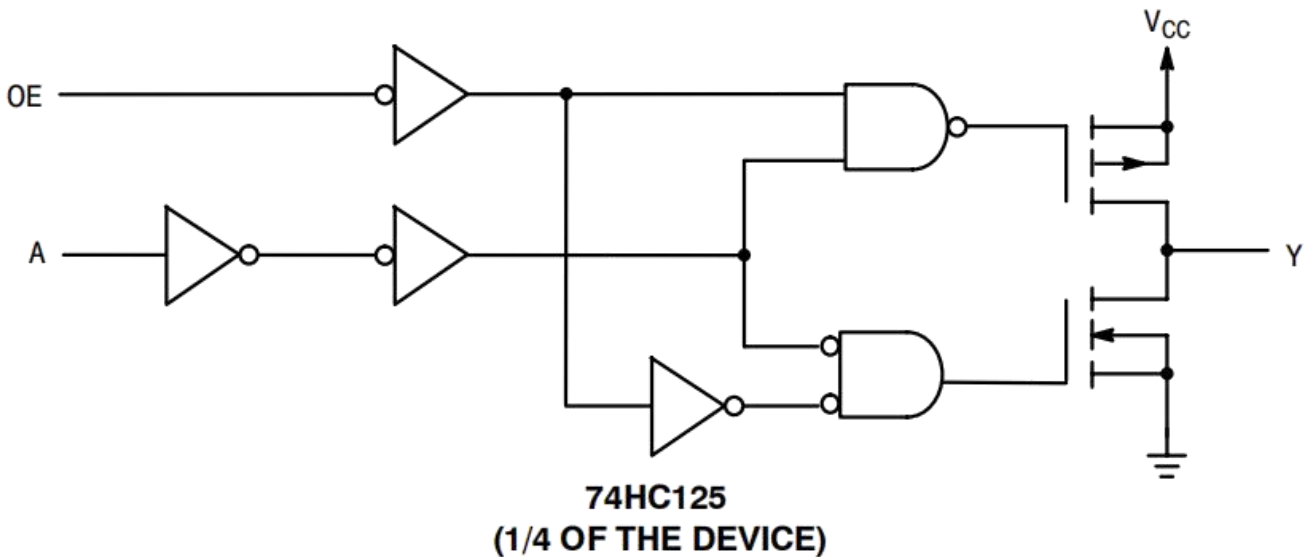
*Includes all probe and jig capacitance

Figure 3. Test Circuit



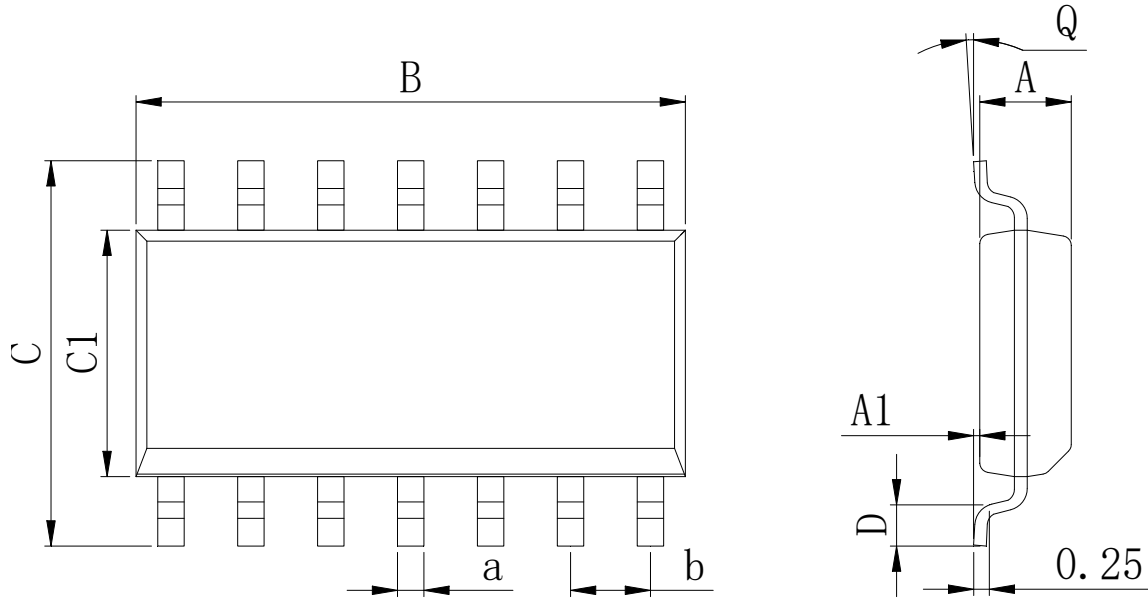
*Includes all probe and jig capacitance

Figure 4. Test Circuit



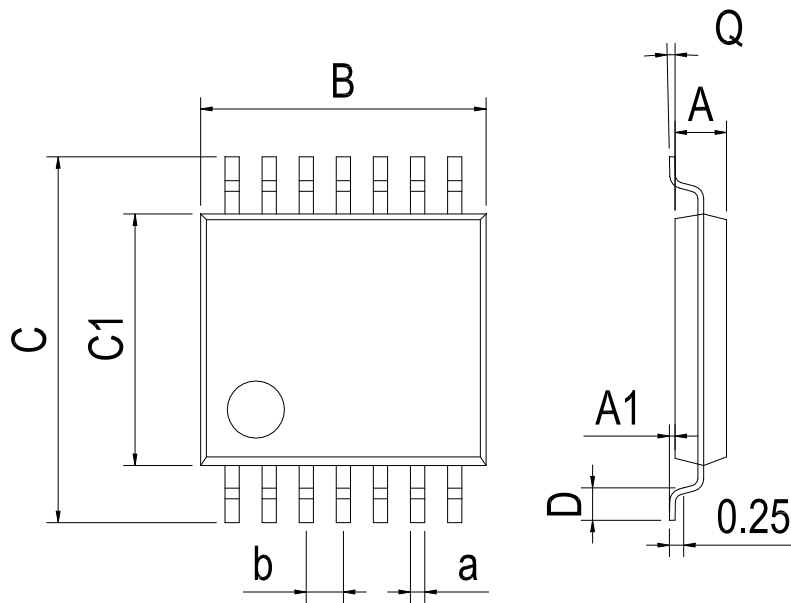
Physical Dimensions

SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2014-9-6	New	1-9
2023-9-18	Update Lead Temperature、 Update encapsulation type、 Add annotation for Maximum Ratings.	1、 3

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