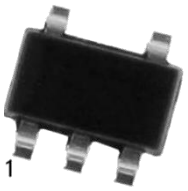
具有开漏和推挽输出的 LMV7235 和 LMV7239
75ns、超低功耗、低压、轨至轨输入比较器

特性

- V_S = 5V，T_A = 25°C（典型值，除非另有说明）
- 传播延迟：75ns
- 低电源电流：65μA
- 轨至轨输入
- 开漏和推挽输出
- 非常适合 2.7V 和 5V 单电源 应用
- 采用节省空间的封装：SOT-23-5 和 SC70-5 封装



SOT-23-5

SC70-5

产品订购信息

产品名称	封装	打印名称	包装	包装数量
LMV7235M5/TR	SOT-23-5	V7235,C21A	编带	3000 只/盒
LMV7235M7/TR	SC70-5	V7235,C21	编带	3000 只/盘
LMV7239M5/TR	SOT-23-5	V7239,C20A	编带	3000 只/盒
LMV7239M7/TR	SC70-5	V7239,C20	编带	3000 只/盘

说明

LMV7235 和 LMV7239 是 75ns 超低功耗低压比较器。这些器件可在 2.7V 至 5.5V 的完整电源电压范围内正常运行。这些器件可实现 75ns 的传播延迟，而在 5V 电压下仅消耗 65μA 的电源电流。

LMV7235 和 LMV7239 具有更大的轨至轨共模电压范围。输入共模电压范围可基于地电压向下扩展 200mV 并基于电源电压向上扩展 200mV，从而允许接地感应和电源感应。

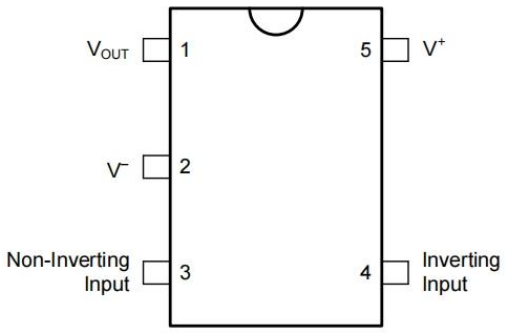
LMV7235 具有开漏输出。通过连接一个外部电阻器，该比较器的输出可以用作电平转换器。LMV7239 具有推挽式输出级。凭借此特性，器件无需外部上拉电阻器即可运行。

LMV7235 和 LMV7239 采用 5 引脚 SC70 和 5 引脚 SOT-23 封装，因此非常适合需要小尺寸和低功耗特性的系统。

应用

- 便携式和电池供电类系统
- 机顶盒
- 高速差分线路接收器
- 窗口比较器
- 过零检测器
- 高速采样电路

引脚配置和功能



SOT23-5/SC70-5

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^-	P	Negative Supply
3	IN^+	I	Noninverting Input
4	IN^-	I	Inverting Input
5	V^+	P	Positive Supply

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Min	Max	Unit
Differential Input Voltage			± Supply Voltage	V
Output Short Circuit Duration			See (2)	
Supply Voltage (V+ - V−)			6	V
Voltage at Input/Output Pins		(V⁻)−0.3	(V⁺) +0.3	V
Current at Input Pin (3)			±10	mA
Storage Temperature, Tstg		–65	150	°C
Junction Temperature,TJ			150	°C
Lead Temperature (Soldering, 10 seconds)		-	245	°C
Electrostatic discharge	Human-body model (HBM)		±1000	V
	Machine model (MM)		±100	
Junction-to-ambient thermal resistance $R_{\theta JA}$	SC70		478	°C/W
	SOT-23		265	°C/W

1、Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2、Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.

3、Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply Voltages (V^+ - V^-)	2.7	5.5	V
Temperature Range(1)	-40	85	°C

(1) The maximum power dissipation is a function of $TJ_{(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

Electrical Characteristics, 2.7 V

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{CM} = V^+ /2, V^+ = 2.7 V, V^- = 0 V^-

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage			-6	±0.8	+6	mV
		At temp extremes		-8		+8	
I_B	Input Bias Current				30	400	nA
		At temp extremes				600	
I_{OS}	Input Offset Current				5	200	nA
		At temp extremes				400	
CMRR	Common-Mode Rejection Ratio	0 V < V_{CM} < 2.7 V (1)		52	62		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V		65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50 dB		V^- -0.1	-0.2 to 2.9	V^+ +0.1	V
			At temp extremes	V^-		V^+	
V_O	Output Swing High (LMV7239 only)	I_L = 4 mA, V_{ID} = 500 mV		V^+ -0.35	V^+ -0.26		V
		I_L = 0.4 mA, V_{ID} = 500 mV			V^+ -0.02		V
	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV			230	350	mV
		At temp extremes				450	
		I_L = −0.4 mA, V_{ID} = −500 mV			15		mV
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0 V (LMV7239 only)			15		mA
		Sinking, V_O = 2.7 V (LMV7235, R_L = 10 k)			20		mA
I_S	Supply Current	No load			52	85	µA
		At temp extremes				100	
t_{PD}	Propagation Delay	Overdrive = 20 mV C_{LOAD} = 15 pF (2)			96		ns
		Overdrive = 50 mV C_{LOAD} = 15 pF (2)			87		ns
		Overdrive = 100 mV C_{LOAD} = 15 pF (2)			85		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV (3)			2		ns
t_r	Output Rise Time	LMV7239 10% to 90%			1.7		ns
		LMV7235 10% to 90%(4)			112		ns
t_f	Output Fall Time	90% to 10%			1.7		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)				3		nA

(1) CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to $V_{CC/2}$ or $V_{CC/2}$ to V_{CC}.

(2) A 10k pullup resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.

(3) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL}.

Electrical Characteristics, 5 V

Unless otherwise specified, all limits ensured for T_A = 25°C, V_{CM} = V^+ /2, V^+ = 5 V, V^- = 0 V.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage			-6	±1	+6	mV
		At temp extremes		-8		+8	
I_B	Input Bias Current				30	400	nA
		At temp extremes				600	
I_{OS}	Input Offset Current				5	200	nA
		At temp extremes		400			
CMRR	Common-Mode Rejection Ratio	0 V < V_{CM} < 5 V		52	67		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V		65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB		V^- −0.1	-0.2 to 5.2	V^+ +0.1	V
			At temp extremes	V^-		V^+	
V_O	Output Swing High (LMV7239 only)	I_L = 4 mA, V_{ID} = 500 mV		V^+ -0.25	V^+ -0.15		V
		I_L = 0.4 mA, V_{ID} = 500 mV			V^+ -0.01		V
	Output Swing Low	I_L = −4 mA, V_{ID} = −500 mV			230	350	mV
			At temp extremes			450	
		I_L = −0.4 mA, V_{ID} = −500 mV			10		mV
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0 V (LMV7239 only)		25	55		mA
			At temp extremes	15			
		Sinking, V_O = 5 V (LMV7235, R_L = 10k)		30	60		mA
			At temp extremes	20			
I_S	Supply Current	No load			65	95	µA
			At temp extremes			110	
t_{PD}	Propagation Delay	Overdrive = 20 mV C_{LOAD} = 15 pF(1)			89		ns
		Overdrive = 50 mV C_{LOAD} = 15 pF(1)			82		ns
		Overdrive = 100 mV C_{LOAD} = 15 pF(1)			75		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV(2)			1		ns
t_r	Output Rise Time	LMV7239 10% to 90%			1.2		ns
		LMV7235 10% to 90%			100		ns
t_f	Output Fall Time	90% to 10%			1.2		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)				3		nA

(1) A 10k pullup resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.

(2) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL}.

Typical Characteristics

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

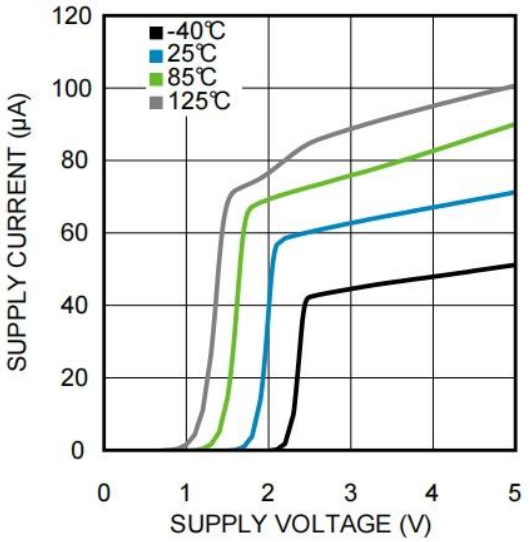


Figure 1. Supply Current vs. Supply Voltage

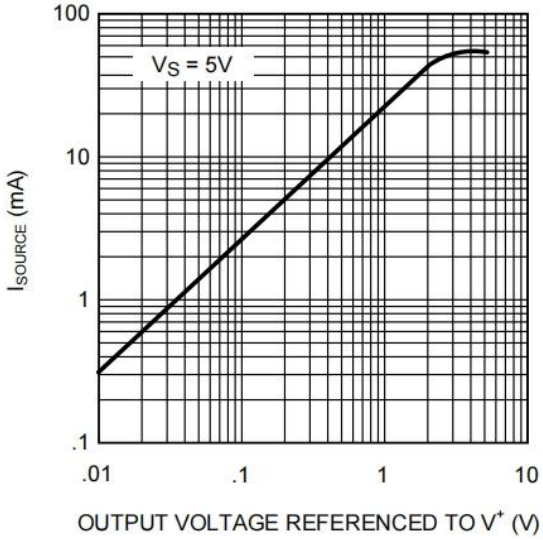


Figure 2. Sourcing Current vs. Output Voltage

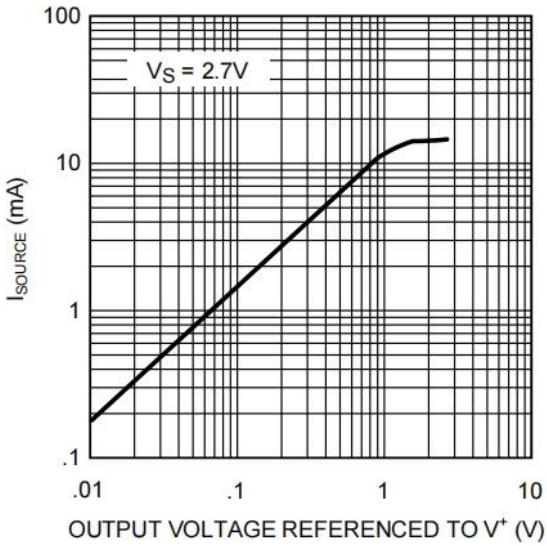


Figure 3. Sourcing Current vs. Output Voltage

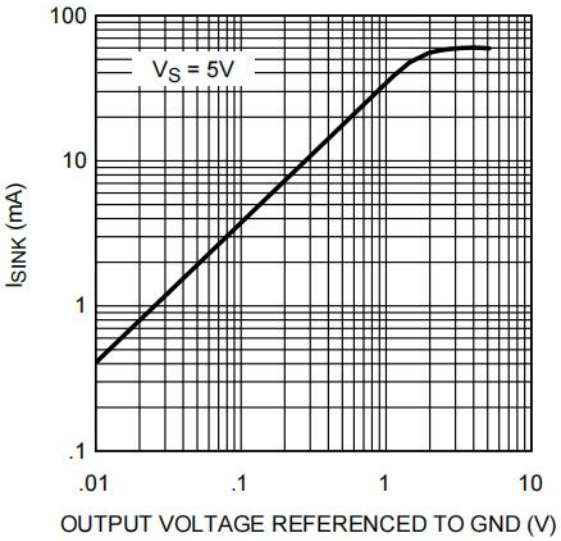


Figure 4. Sinking Current vs. Output Voltage

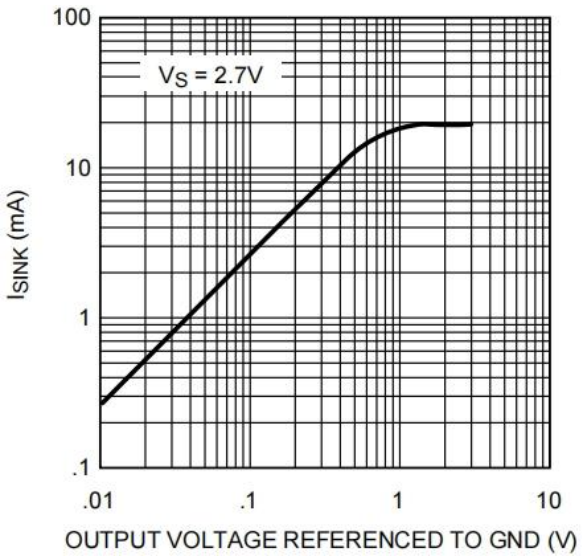


Figure 5. Sinking Current vs. Output Voltage

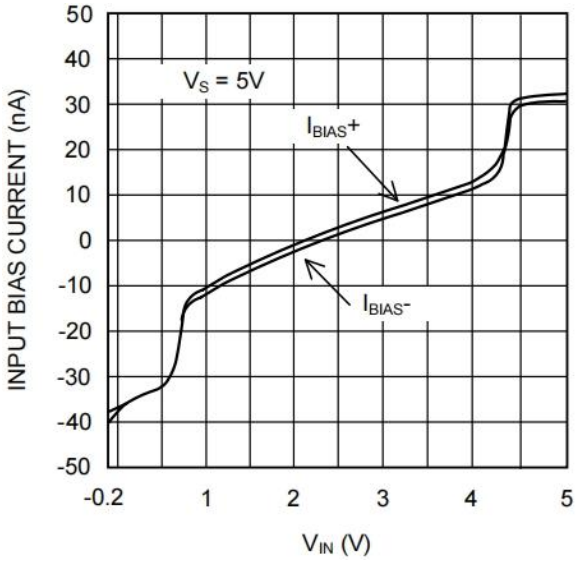


Figure 6. Input Bias Current vs. Input Voltage

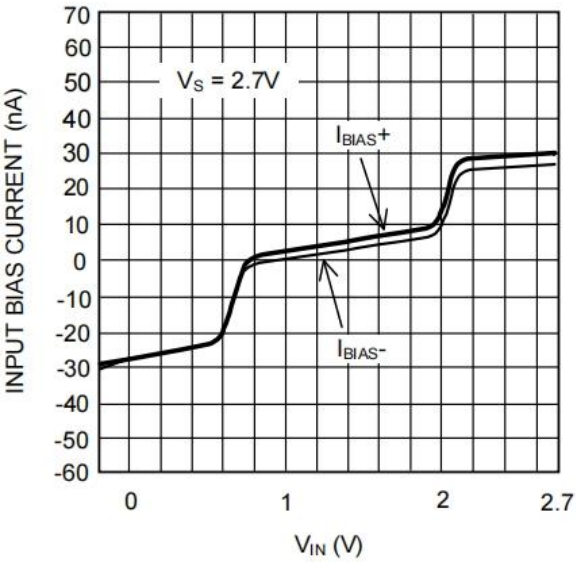


Figure 7. Input Bias Current vs. Input Voltage

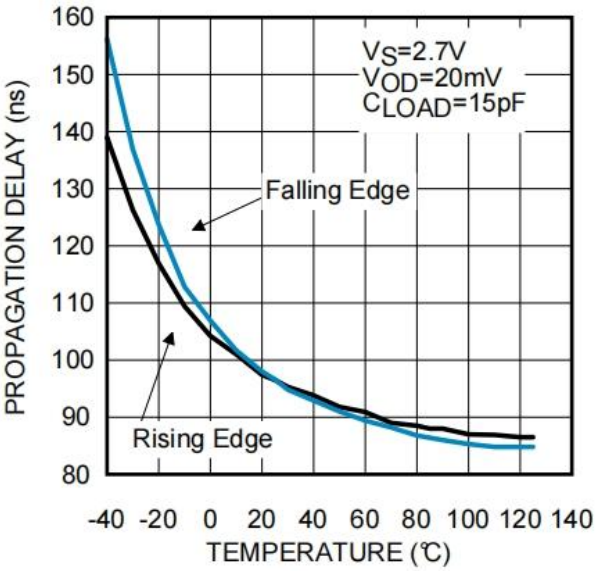


Figure 8. Propagation Delay vs. Temperature

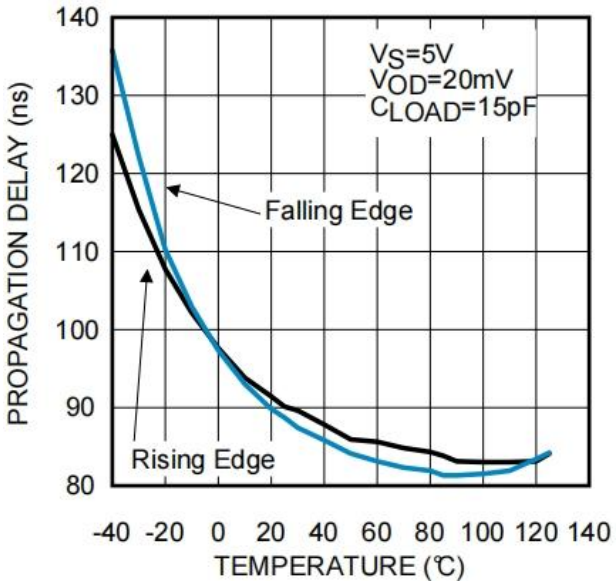


Figure 9. Propagation Delay vs. Temperature

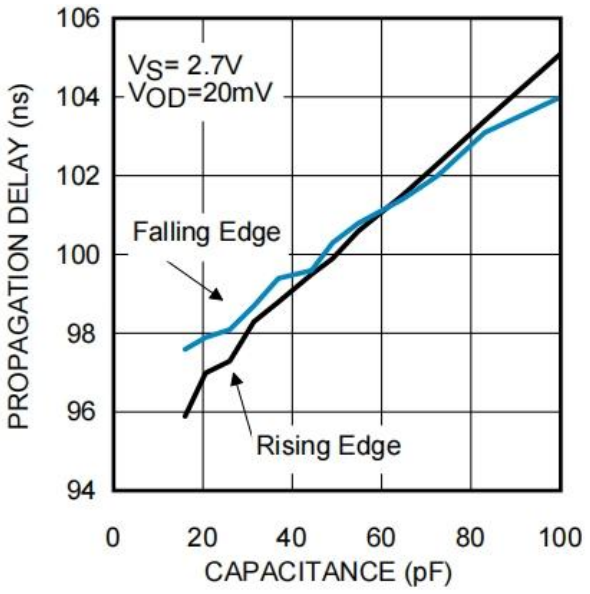


Figure 10. Propagation Delay vs. Capacitive Load

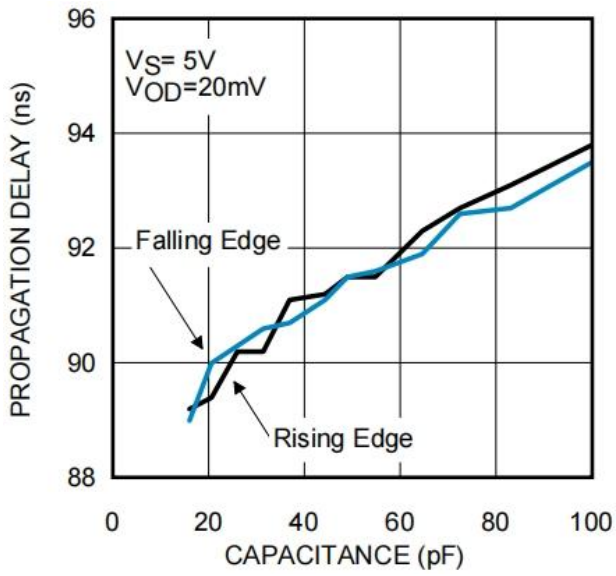


Figure 11. Propagation Delay vs. Capacitive Load

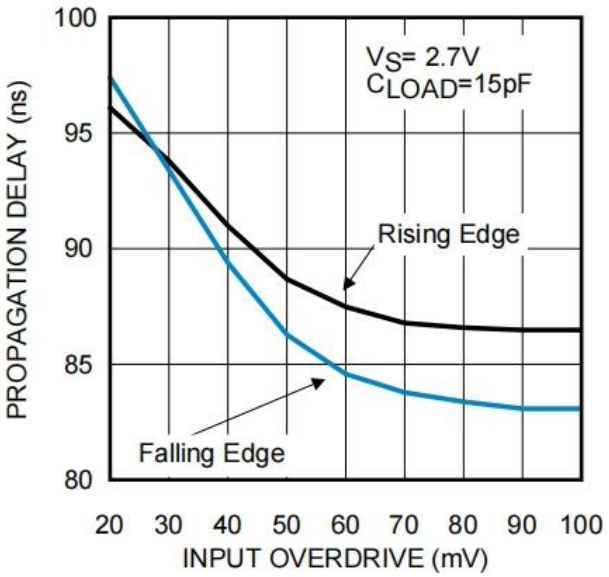


Figure 12. Propagation Delay vs. Input Overdrive

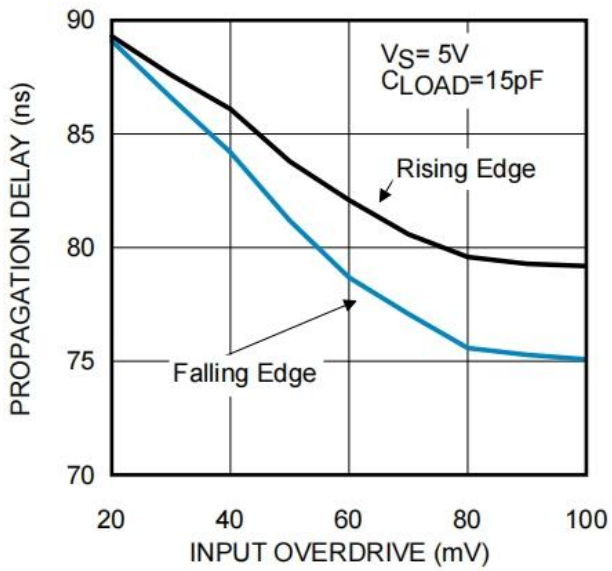


Figure 13. Propagation Delay vs. Input Overdrive

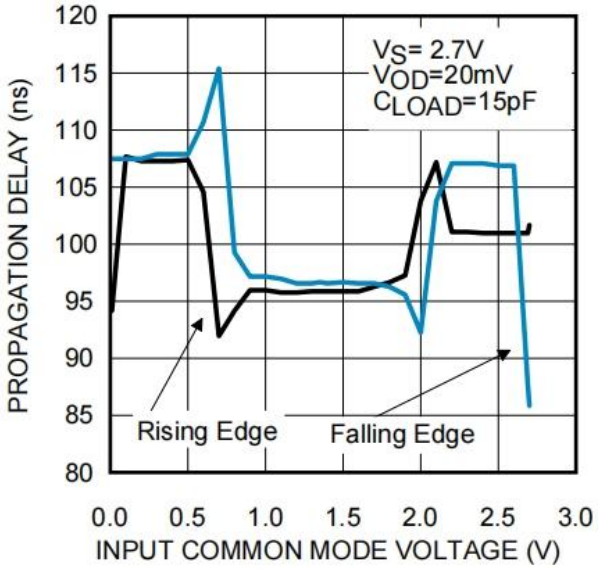


Figure14. Propagation Delay vs. Common-Mode Voltage

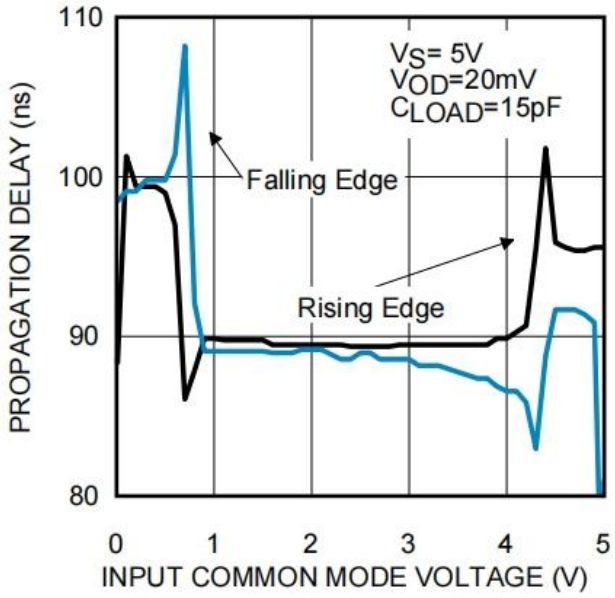


Figure 15. Propagation Delay vs. Common-Mode Voltage

Detailed Description

The LMV7235 and LMV7239 are ultra low power, low voltage, 75-ns comparators. They are ensured to operate over the full supply voltage range of 2.7 V to 5.5 V. These devices achieve a 75-ns propagation delay while consuming only 65 μA of supply current at 5 V.

The LMV7235 and LMV7239 have a greater than rail-to-rail common-mode voltage range. The input commonmode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

Functional Block Diagram

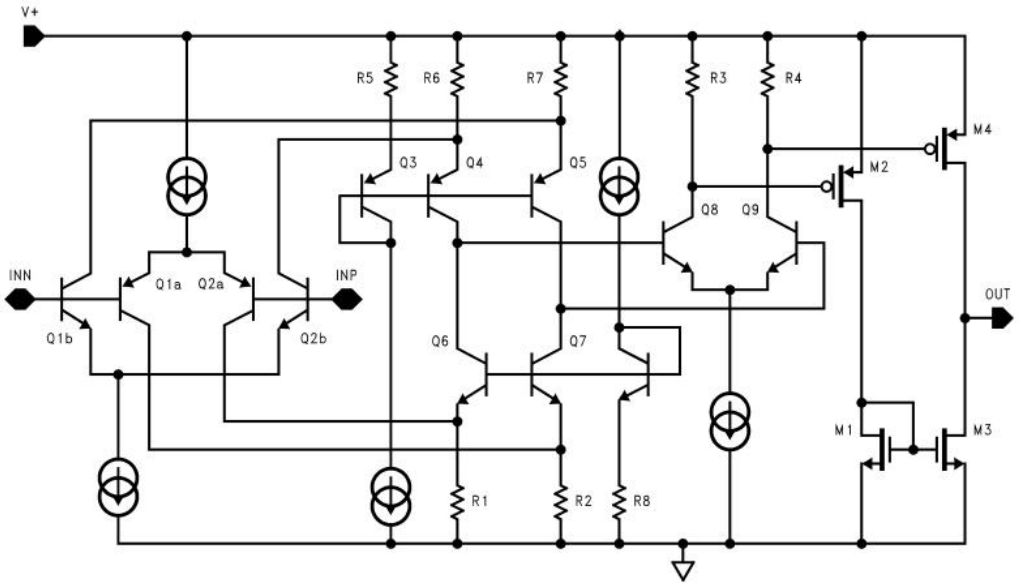


Figure 16. Simplified Schematic of LMV7239

Feature Description

Input Stage

The LMV7235 and LMV7239 are rail-to-rail input and output. The typical input common-mode voltage range of −0.2 V below the ground to 0.2 V above the supply. The LMV7235 and LMV7239 use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on resulting in an increase of input bias current.

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common-mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

Output Stage: LMV7239

The LMV7239 has a push-pull output. When the output switches, there is a low resistance path between V_{CC} and ground, causing high output sinking or sourcing current during the transition.

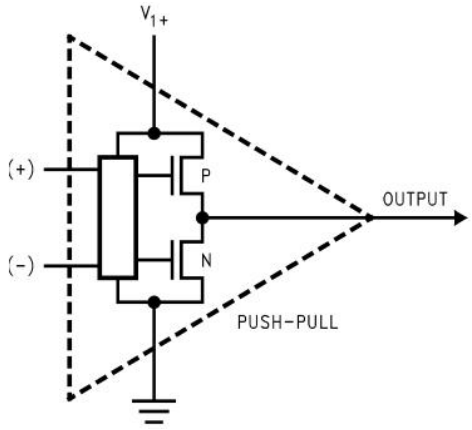


Figure 17. LMV7239 Push-Pull Output Stage

Output Stage: LMV7235

The LMV7235 has an open drain that requires a pull-up resistor to a positive supply voltage for the output to switch properly. The internal circuitry is identical to the LMV7239 except that the upper P channel output device M4 is absent in the Functional Block Diagram above. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage by the external pull-up resistor. This allows the output to be OR'ed with other open drain outputs on the same bus. The output pull-up resistor can be connected to any voltage level between V- and V+ for level shifting applications.

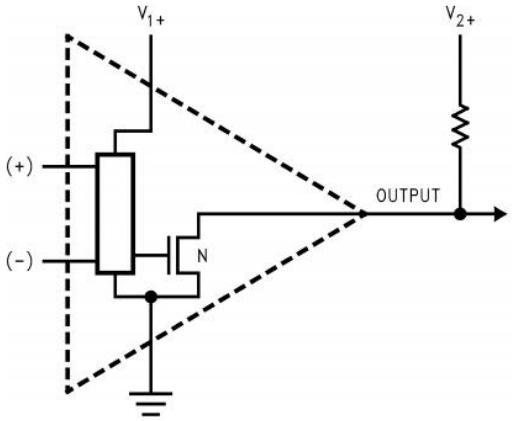


Figure 18. LMV7235 Open Drain Output

Device Functional Modes

Capacitive and Resistive Loads

The propagation delay on the rising edge of the LMV7235 depends on the load resistance and capacitance values.

Noise

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero. The high gain of this comparator eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See Hysteresis.)

Hysteresis

To improve propagation delay when low overdrive is needed hysteresis can be added.

Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V^+ of the comparator as shown in Figure 19. When V_{IN} at the inverting input is less than V_A, the voltage at the noninverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume VO switches as high as V^+). The three network resistors can be represented as R_1 //R_3 in series with R_2 .

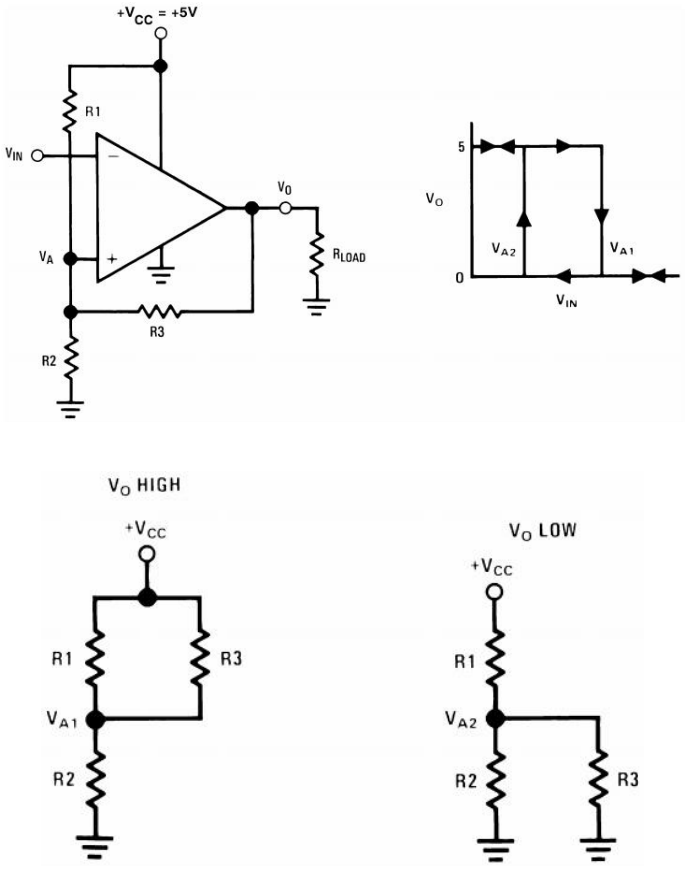


Figure 19. Inverting Comparator With Hysteresis

The lower input trip voltage VA1 is defined as:

$$V_{A1} = V_{CC}R_2 / [(R_1 // R_3) + R_2)] \quad (1)$$

When VIN is greater than VA, the output voltage is low or very close to ground. In this case the three network resistors can be presented as R_2 // R_3 in series with R_1 .

The upper trip voltage V_{A2} is defined as:

$$V_{A2} = V_{CC} (R_2 // R_3) / [(R_1) + (R_2 // R_3)] \quad (2)$$

The total hysteresis provided by the network is defined as $\Delta V_A = V_{A1} - V_{A2}$.

$$\Delta V_A = \frac{+V_{CC}R_1R_2}{R_1R_2 + R_1R_3 + R_2R_3} \quad (3)$$

Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by:

$$\Delta V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \quad (4)$$

As soon as V_O switches to V_{CC}, V_A steps to a value greater than V_{REF} which is given by:

$$V_A = V_{1N}\frac{(V_{CC} - V_{IN1})R_1}{R_1 + R_2} \quad (5)$$

To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN2} can be calculated by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (6)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC}R_1 / R_2. \quad (7)$$

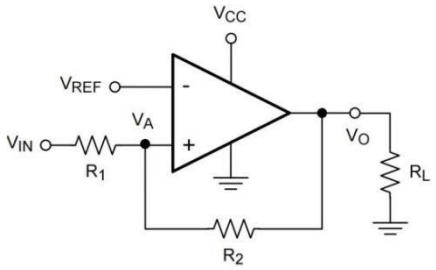


Figure 20. Noninverting Comparator With Hysteresis

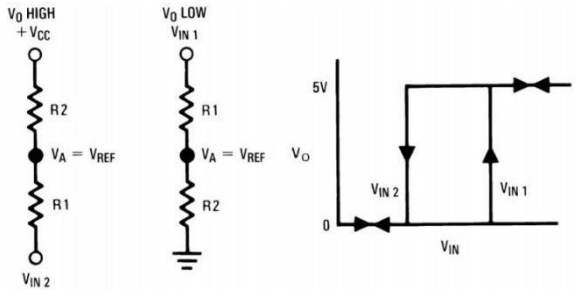


Figure 21. Noninverting Comparator Thresholds

Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100 mV_{PP} A_C signal. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

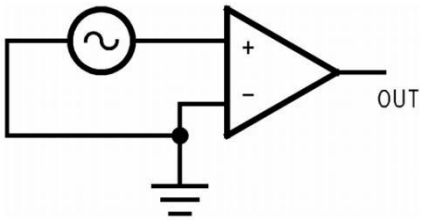


Figure 22. Simple Zero Crossing Detector

Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R_4 and R_5 establishes a reference voltage, V_1 , at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5 , the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

The positive feedback resistor, R_6 , is made very large with respect to R_5 || R_6 = 2000 R_5). The resultant hysteresis established by this network is very small (ΔV_1 < 10 mV) but it is sufficient to insure rapid output voltage transitions.

Diode D_1 is used to ensure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1 .

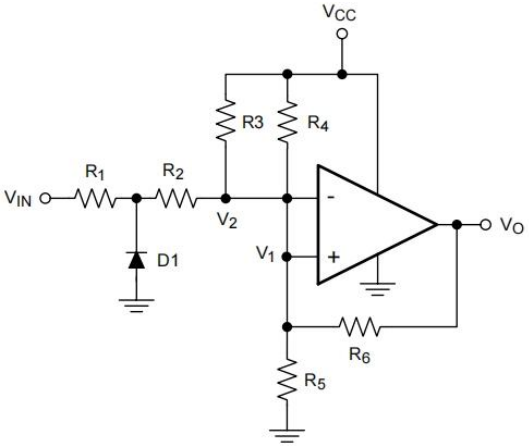


Figure 23. Zero Crossing Detector With Hysteresis

Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the V_{REF} threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

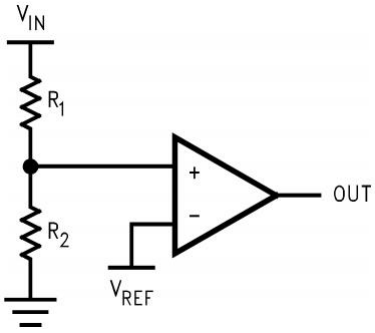


Figure 24. Threshold Detector

Application Information

The LMV7235 and LMV7239 are single supply comparators with 75 ns of propagation delay and only 65 μA of supply current.

Typical Applications

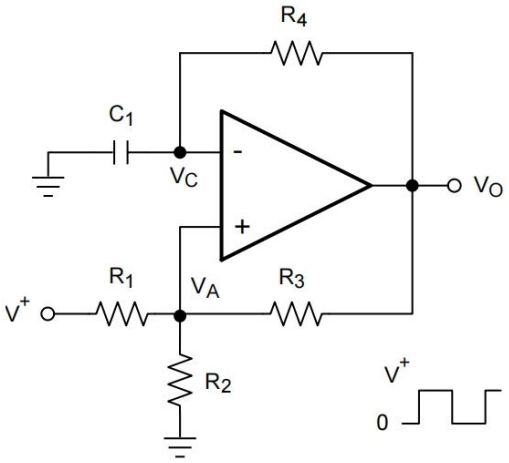


Figure 25. Square Wave Oscillator

Design Requirements

A typical application for a comparator is as a square wave oscillator. The circuit in Figure 25 generates a square wave whose period is set by the RC time constant of the capacitor C_1 and resistor R_4 .

Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

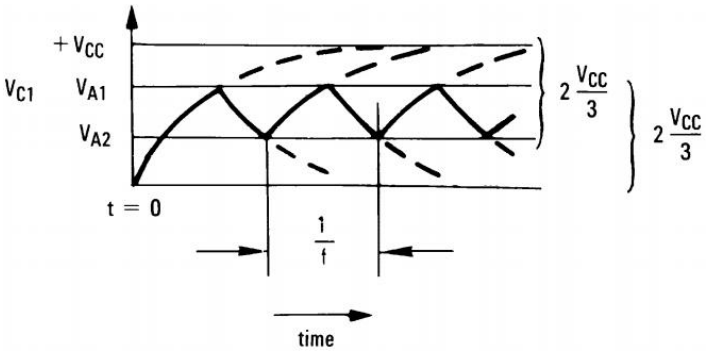


Figure 26. Square Wave Oscillator Timing Thresholds

Consider the output of Figure 25 to be high to analyze the circuit. That implies that the inverted input (V_C) is lower than the noninverting input (V_A). This causes the C1 to be charged through R4 , and the voltage V_C increases until it is equal to the noninverting input. The value of VA at this point is:

$$V_{A1} = \frac{V_{CC} \bullet R_2}{R2 + R_1 \| R_3} \quad (8)$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ Vcc/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is:

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + (R_2 \| R_3)} \quad (9)$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$.

The capacitor C_1 now discharges through R4 , and the voltage V_C decreases until it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1 \cdot \ln 2$. Hence the formula for the frequency is:

$$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2) \quad (10)$$

The LMV7239 should be used for a symmetrical output. The LMV7235 will require a pullup resistor on the output to function, and will have a slightly asymmetrical output due to the reduced sourcing current.

Application Curves

Figure 27 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
2. $C_1 = 100\ pF$, $C_L = 20\ pF$
3. V+ = 5 V, V– = GND
4. C_{STRAY} (not shown) from Va to GND = 10 pF

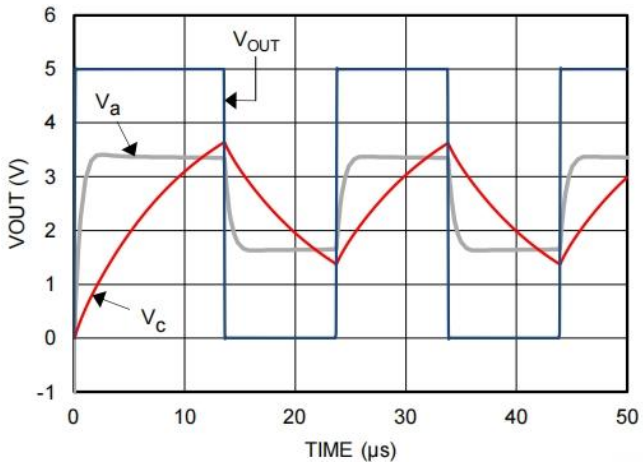


Figure 27. Square Wave Oscillator Output Waveform

Crystal Oscillator

A simple crystal oscillator using the LMV7235 or LMV7239 is shown in Figure 28. Resistors R1 and R_2 set the bias point at the comparator's noninverting input. Resistors, R_3 and R_4 and capacitor C_1 set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator

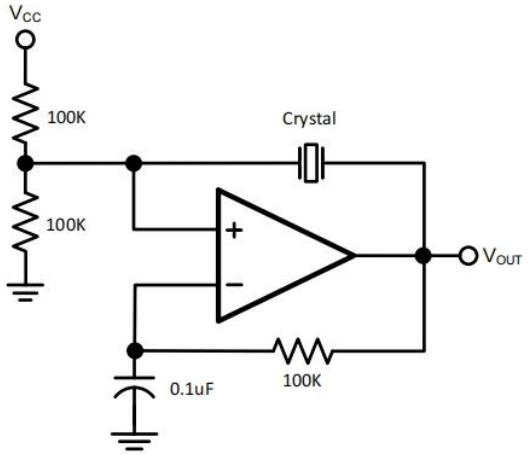


Figure 28. Crystal Oscillator

Infrared (IR) Receiver

The LMV7235 and LMV7239 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across RD. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

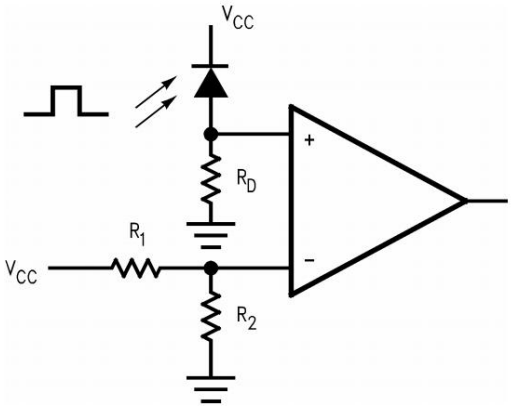


Figure 29. IR Receiver

Window Detector

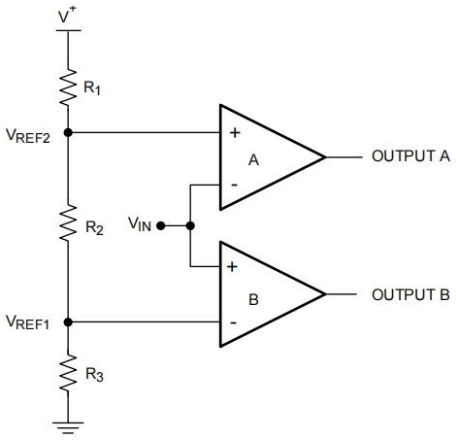


Figure 30. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$

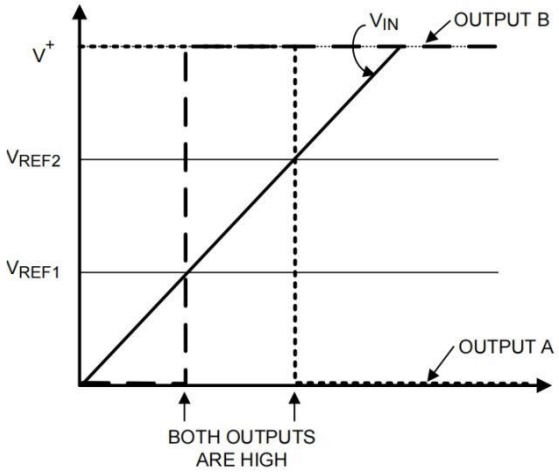


Figure 31. Window Detector Output Signal

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$, or "within the window", where these are defined as:

$$V_{REF1} = R_3 / R_1+R_2+R_3) \times V+ \quad (11)$$

$$V_{REF2} = R_2+R_3)/R_1+R_2+R_3) \times V+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The LMV7235 with an open drain output should be used if the outputs are to be tied together for a common logic output.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-μF ceramic capacitor in parallel with a 10-μF capacitor.

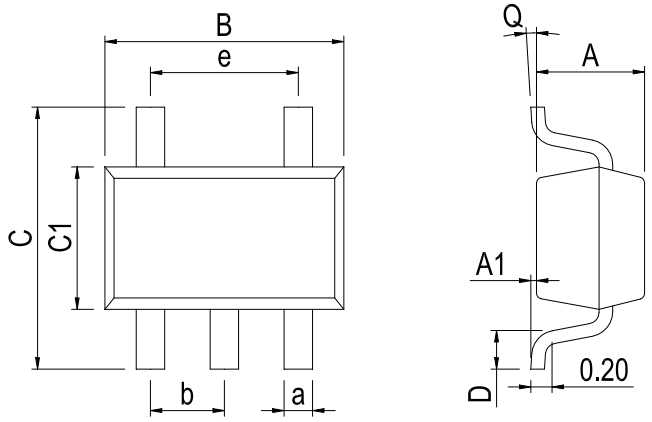
Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to "ring" due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7235 and LMV7239 as high-speed devices. Keep the ground paths short and place small (low ESR ceramic) bypass capacitors directly between the V+ and V– pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

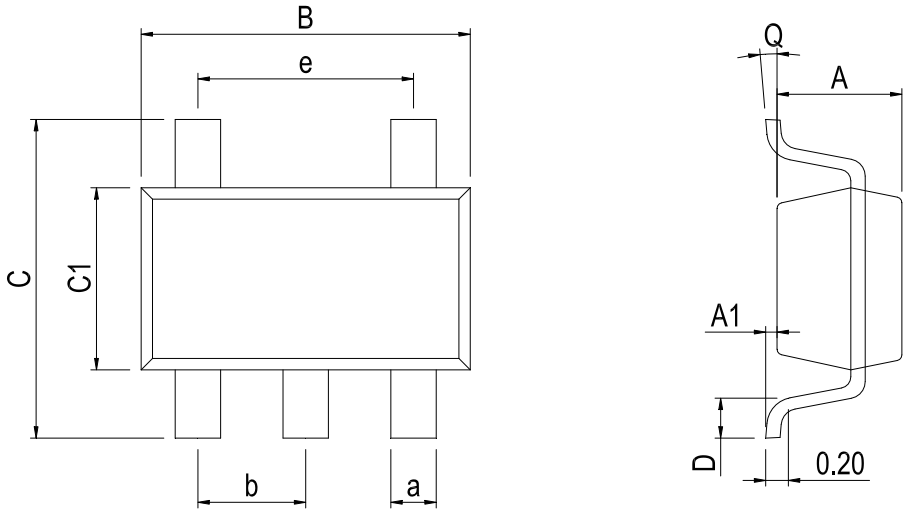
Physical Dimensions

SOT23-5



Dimensions In Millimeters(SOT23-5)										
Symbol:	A	A1	B	C	C1	D	Q	a	b	e
Min:	1.05	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC	1.90 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.40		

SC70-5



Dimensions In Millimeters(SC70-5)										
Symbol:	A	A1	B	C	C1	D	Q	a	b	e
Min:	0.90	0.00	2.00	2.15	1.15	0.26	0°	0.15	0.65 BSC	1.30 BSC
Max:	1.00	0.15	2.20	2.45	1.35	0.46	8°	0.35		

Revision History

DATE	REVISION	PAGE
2015-3-17	New	1-23
2023-10-31	Document Reformatting、Update SC70-5 Physical Dimensions	1-22、20

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