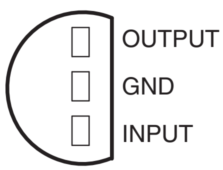
LP2950/LP2951

ADJUSTABLE MICROPOWER VOLTAGE REGULATORS WITH SHUTDOWN

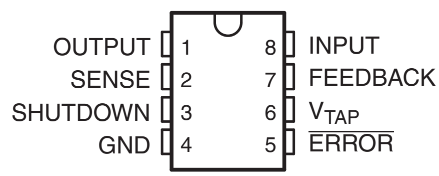
FEATURES

- **Wide Input Range…up to 30 V**
- **Rated Output Current of 100 mA**
- **Low Dropout…380 mV (Typ) at 100 mA**
- **Low Quiescent Current…75 μA (Typ)**
- **Tight Line Regulation…0.03% (Typ)**
- **Tight Load Regulation…0.04% (Typ)**
- **High V_O Accuracy**
  - **1.4% at 25°C**
  - **2% Over Temperature**
- **Can Be Used as a Regulator or Reference**
- **Stable With Low ESR (>12 mΩ) Capacitors**
- **Current- and Thermal-Limiting Features**
- **LP2950 Only (3-Pin Package)**
  - **Fixed-Output Voltages of 5 V, 3.3 V, and 3 V**
- **LP2951 Only (8-Pin Package)**
  - **Fixed- or Adjustable-Output Voltages: 5 V/ADJ, 3.3 V/ADJ, and 3 V/ADJ**
  - **Low-Voltage Error Signal on Falling Output**
  - **Shutdown Capability**
  - **Remote Sense Capability for Optimal Output Regulation and Accuracy**

LP2950...LP (TO-226/TO-92 PACKAGE)
(BOTTOM VIEW)



LP2951...D (SOIC) PACKAGE
(TOP VIEW)



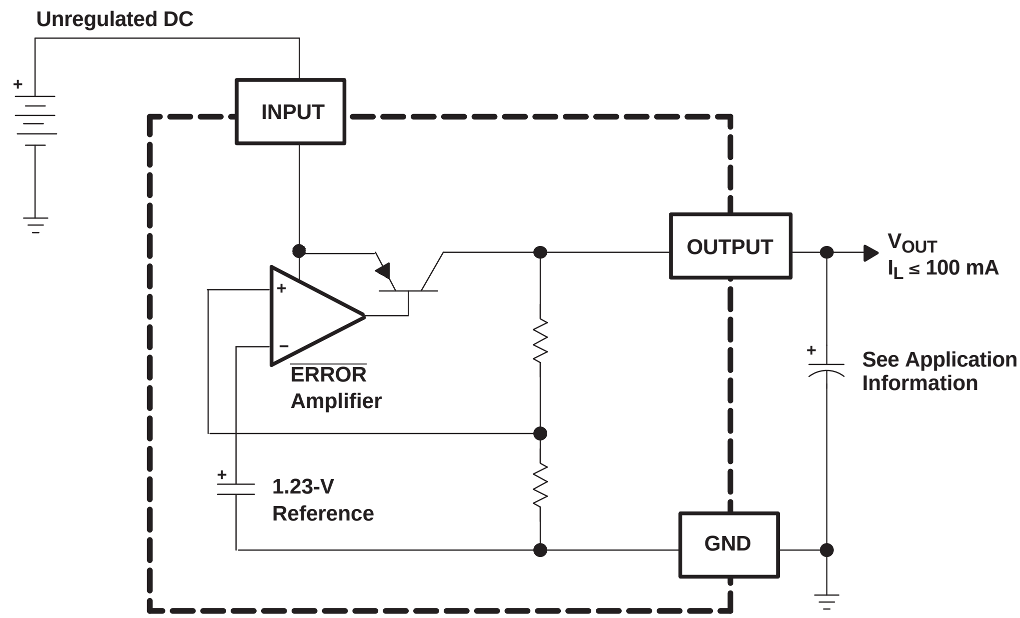
DESCRIPTION

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The easy-to-use, 3-pin LP2950 is available in fixed-output voltages of 5 V, 3.3 V, and 3 V. However, the 8-pin LP2951 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and V_{TAP} pins together, the LP2951 outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and V_{TAP} pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

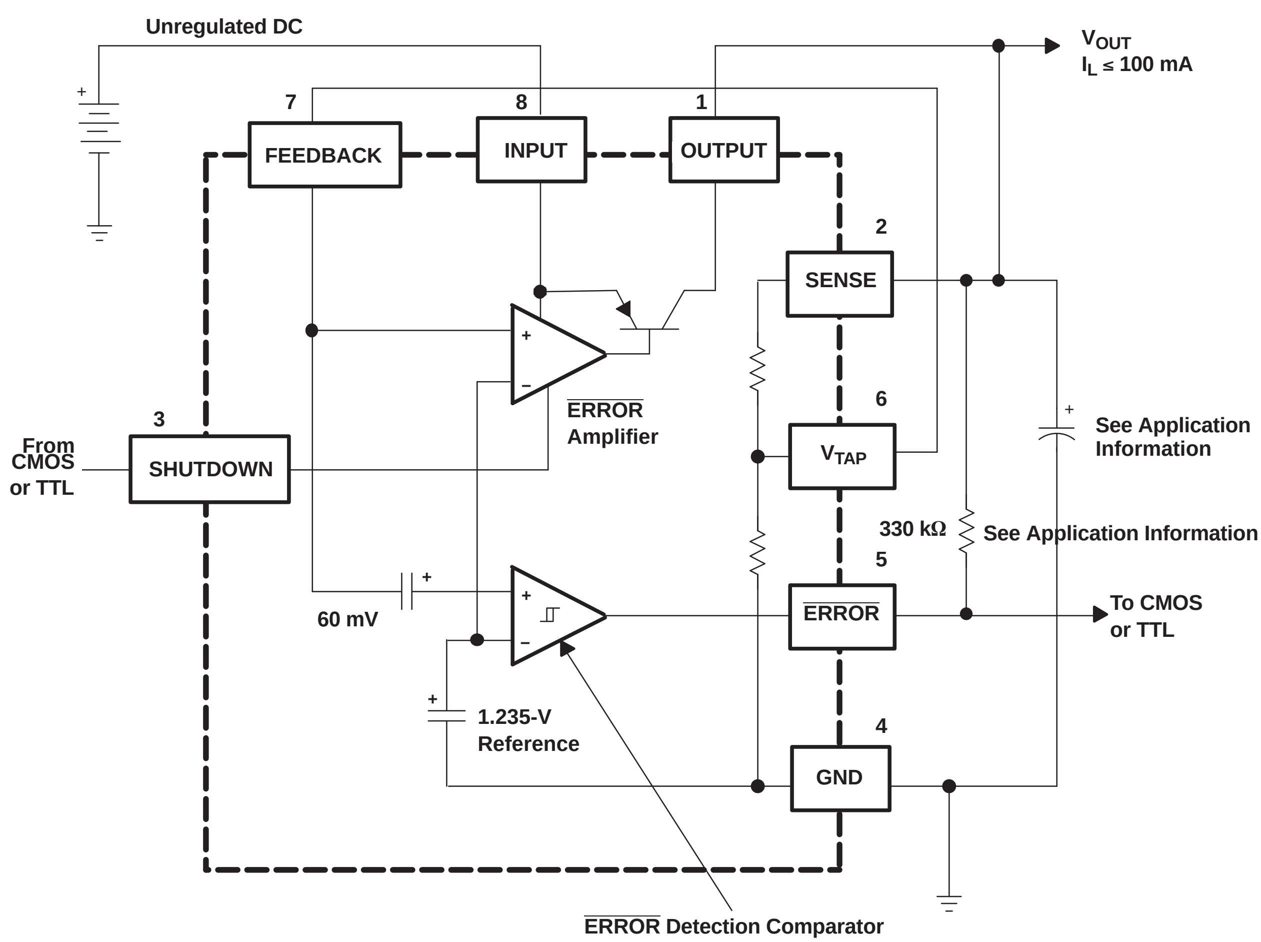
The 8-pin LP2951 also offers additional functionality that makes it particularly suitable for battery-powered applications. For example, a logic-compatible shutdown feature allows the regulator to be put in standby mode for power savings. In addition, there is a built-in supervisor reset function in which the $\overline{\text{ERROR}}$ output goes low when V_{OUT} drops by 6% of its nominal value for whatever reasons – due to a drop in V_{IN}, current limiting, or thermal shutdown.

The LP2950 and LP2951 are designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20 ppm typical), extremely good line and load regulation (0.3% and 0.4% typical), and remote sensing capability, the parts can be used as either low-power voltage references or 100-mA regulators.

LP2950 FUNCTIONAL BLOCK DIAGRAM



LP2951 FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Continuous input voltage range		–0.3	30	V
V_{SHDN}	SHUTDOWN input voltage range		–1.5	30	V
	$\overline{\text{ERROR}}$ comparator output voltage range[2]		–1.5	30	V
V_{FDBK}	FEEDBACK input voltage range[2][3]		–1.5	30	V
θ_{JA}	Package thermal impedance[4][5]	D package		97	°C/W
		LP package		140	°C/W
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) May exceed input supply voltage
(3) If load is returned to a negative power supply, the output must be diode clamped to GND.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	[1]	30	V
T_J	Operating virtual junction temperature	–40	125	°C

(1) Minimum V_{IN} is the greater of:
   a. 2 V (25°C), 2.3 V (over temperature), or
   b. $V_{OUT(MAX)}$ + Dropout (Max) at rated I_L

Electrical Characteristics

$V_{IN} = V_{OUT}$ (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3-V and 3.3-V versions),
8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN} \leq 0.7$ V

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
3-V VERSION (LP295x-30)							
V_{OUT}	Output voltage	I_L = 100µA	25°C	2.970	3	3.030	V
			–40°C to 125°C	2.940	3	3.060	
3.3-V VERSION (LP295x-33)							
V_{OUT}	Output voltage	I_L = 100µA	25°C	3.267	3.3	3.333	V
			–40°C to 125°C	3.234	3.3	3.366	
5-V VERSION (LP295x-50)							
V_{OUT}	Output voltage	I_L = 100µA	25°C	4.950	5	5.050	V
			–40°C to 125°C	4.900	5	5.100	
ALL VOLTAGE OPTIONS							
	Output voltage temperature coefficient (1)	I_L = 100 µA	–40°C to 125°C		20	100	ppm/°C
	Line regulation (2)	V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 30 V	25°C		0.03	0.2	%/V
			–40°C to 125°C			0.4	
	Load regulation (2)	I_L = 100 µA to 100 mA	25°C		0.04	0.2	%
			–40°C to 125°C			0.3	
$V_{IN} - V_{OUT}$	Dropout voltage (3)	I_L = 100 µA	25°C		50	80	mV
			–40°C to 125°C			150	
		I_L = 100 mA	25°C		380	450	
			–40°C to 125°C			600	
I_{GND}	GND current	I_L = 100 µA	25°C		75	120	µA
			–40°C to 125°C			140	
		I_L = 100 mA	25°C		8	12	mA
			–40°C to 125°C			14	
	Dropout ground current	$V_{IN} = V_{OUT(NOM)}$ – 0.5 V, I_L = 100 µA	25°C		110	170	µA
			–40°C to 125°C			200	
	Current limit	V_{OUT} = 0 V	25°C		160	200	mA
			–40°C to 125°C			220	
	Thermal regulation (4)	I_L = 100 µA	25°C		0.05	0.2	%/W
	Output noise (RMS), 10 Hz to 100 kHz	C_L = 1 µF (5 V only)	25°C		430		µV
		C_L = 200 µF			160		
		LP2951-50: C_L = 3.3 µF, C_{Bypass} = 0.01 µF between pins 1 and 7			100		
(LP2951-xx) 8-PIN VERSION ONLY ADJ							
	Reference voltage		25°C	1.218	1.235	1.252	V
			–40°C to 125°C	1.212		1.257	
		$V_{OUT} = V_{REF}$ to (V_{IN} – 1 V), V_{IN} = 2.3 V to 30 V, I_L = 100 µA to 100 mA	–40°C to 125°C	1.200		1.272	
	Reference voltage temperature coefficient (1)		25°C		20		ppm/°C

(1) Output or reference voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(2) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(3) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV, below the value measured at 1-V differential. The minimum input supply voltage of 2 V (2.3 V over temperature) must be observed.
(4) Thermal regulation is defined as the change in output voltage at a time (T) after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50-mA load pulse at V_{IN} = 30 V, V_{OUT} = 5 V (1.25-W pulse) for t = 10 ms.

Electrical Characteristics (continued)

V_{IN} = V_{OUT} (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3-V and 3.3-V versions),
8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

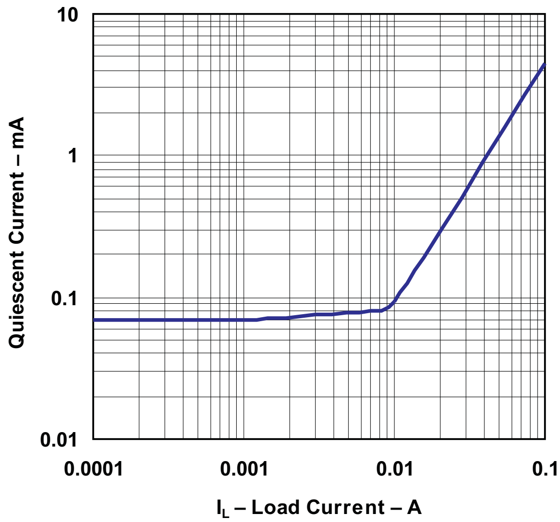
PARAMETER	TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
FEEDBACK bias current		25°C		20	40	nA
		–40°C to 125°C			60	
FEEDBACK bias current temperature coefficient		25°C		0.1		nA/°C
$\overline{\text{ERROR}}$ COMPARATOR						
Output leakage current	V_{OUT} = 30 V	25°C		0.01	1	µA
		–40°C to 125°C			2	
Output low voltage	V_{IN} = $V_{OUT(NOM)}$ – 0.5 V, I_{OL} = 400 µA	25°C		150	250	mV
		–40°C to 125°C			400	
Upper threshold voltage ($\overline{\text{ERROR}}$ output high)(5)		25°C	40	60		mV
		–40°C to 125°C	25			
Lower threshold voltage ($\overline{\text{ERROR}}$ output low)(5)		25°C		75	95	mV
		–40°C to 125°C			140	
Hysteresis(6)		25°C		15		mV
SHUTDOWN INPUT						
Input logic voltage	Low (regulator ON)	–40°C to 125°C			0.7	V
	High (regulator OFF)		2			
SHUTDOWN input current	V_{TAP} = 2.4 V	25°C		30	50	µA
		–40°C to 125°C			100	
	V_{TAP} = 30 V	25°C		450	600	
		–40°C to 125°C			750	
Regulator output current in shutdown	$V_{SHUTDOWN}$ ≥ 2 V, V_{IN} ≤ 30 V, V_{OUT} = 0, FEEDBACK tied to V_{TAP}	25°C		3	10	µA
		–40°C to 125°C			20	

(5) Comparator thresholds are expressed in terms of a voltage differential equal to the nominal reference voltage (measured at V_{IN} – V_{OUT} = 1 V) minus FEEDBACK terminal voltage. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5 V, the $\overline{\text{ERROR}}$ output is specified to go low when the output drops by 95 mV × 5 V/1.235 V = 384 mV. Thresholds remain constant as a percentage of V_{OUT} (as V_{OUT} is varied), with the low-output warning occurring at 6% below nominal (typ) and 7.7% (max).

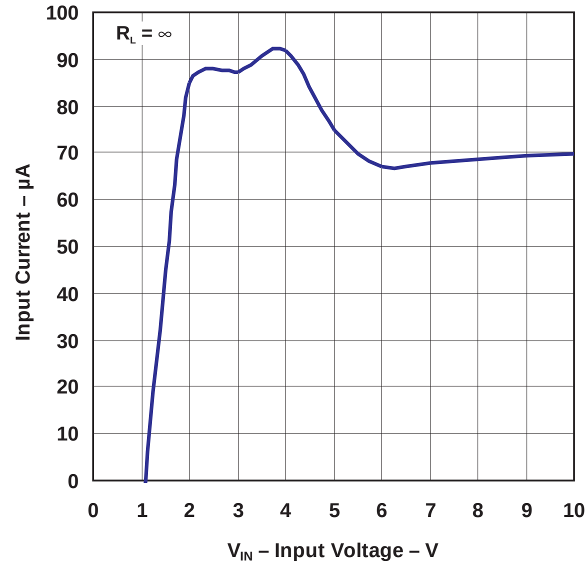
(6) Comparator thresholds are expressed in terms of a voltage differential equal to the nominal reference voltage (measured at V_{IN} – V_{OUT} = 1 V) minus FEEDBACK terminal voltage. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5 V, the $\overline{\text{ERROR}}$ output is specified to go low when the output drops by 95 mV × 5 V/1.235 V = 384 mV. Thresholds remain constant as a percentage of V_{OUT} (as V_{OUT} is varied), with the low-output warning occurring at 6% below nominal (typ) and 7.7% (max).

TYPICAL CHARACTERISTICS

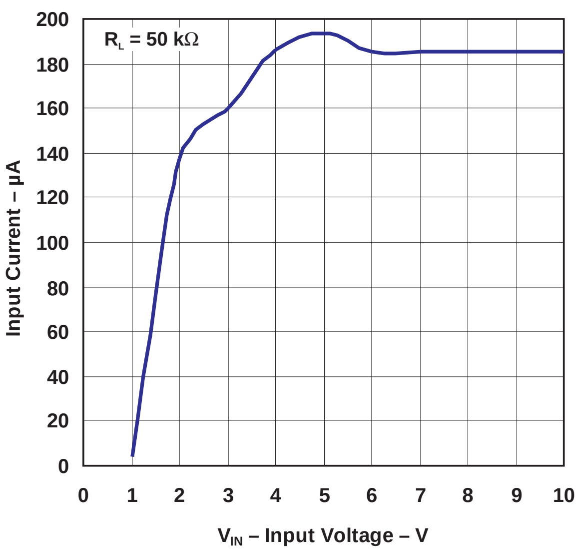
QUIESCENT CURRENT
vs
LOAD CURRENT



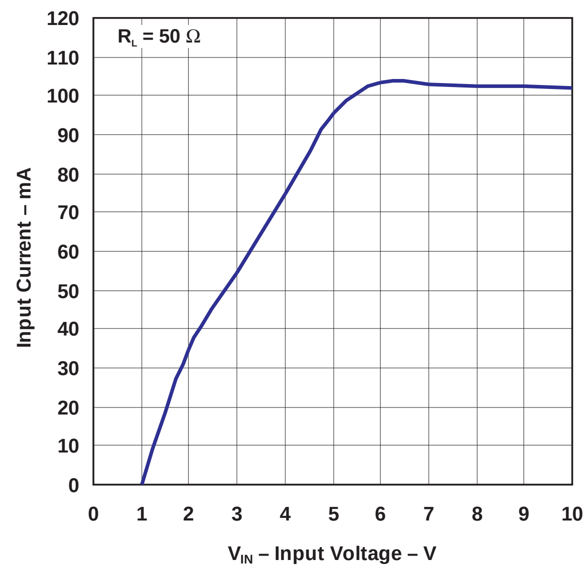
INPUT CURRENT
vs
INPUT VOLTAGE



INPUT CURRENT
vs
INPUT VOLTAGE

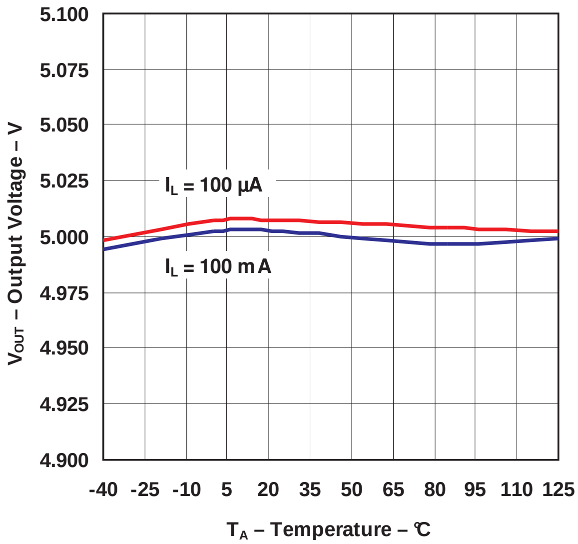


INPUT CURRENT
vs
INPUT VOLTAGE

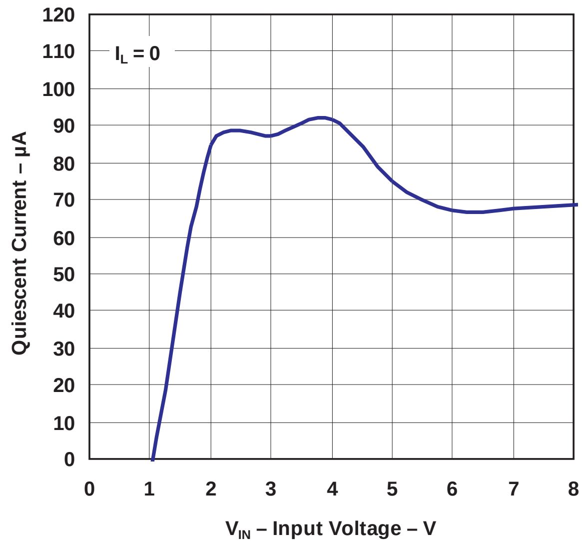


TYPICAL CHARACTERISTICS (continued)

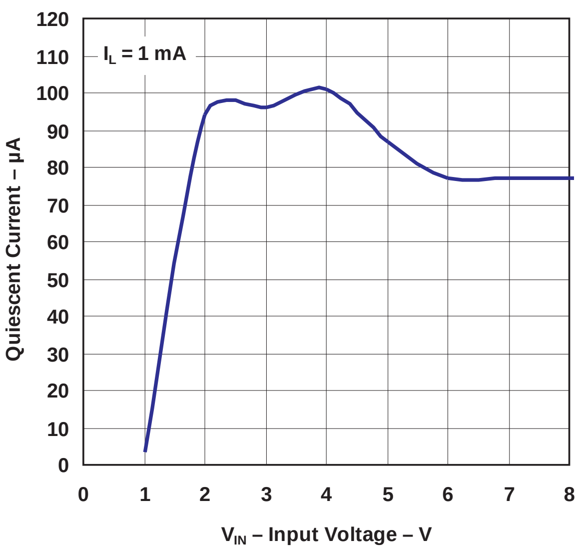
OUTPUT VOLTAGE vs TEMPERATURE



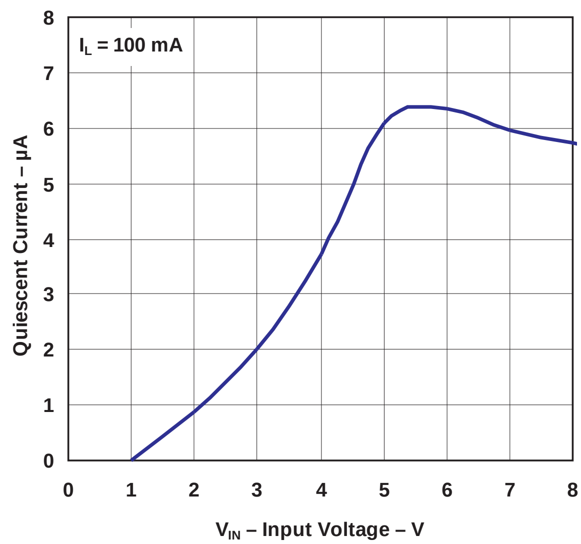
QUIESCENT CURRENT vs INPUT VOLTAGE



QUIESCENT CURRENT vs INPUT VOLTAGE

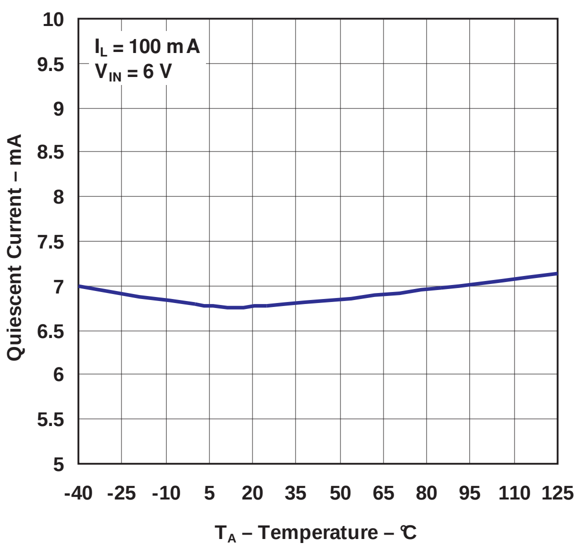


QUIESCENT CURRENT vs INPUT VOLTAGE

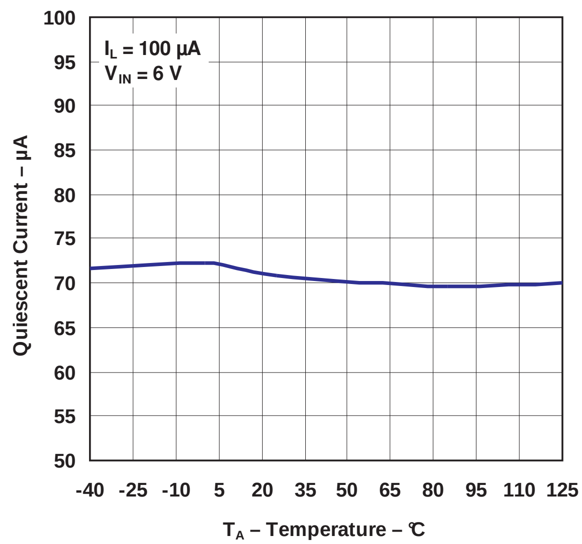


TYPICAL CHARACTERISTICS (continued)

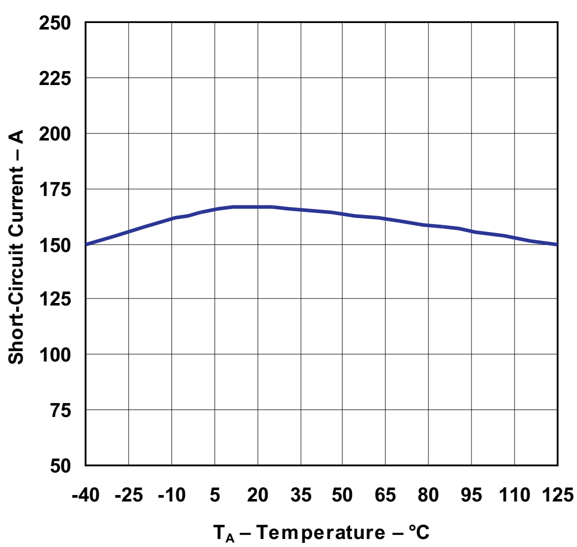
QUIESCENT CURRENT vs TEMPERATURE



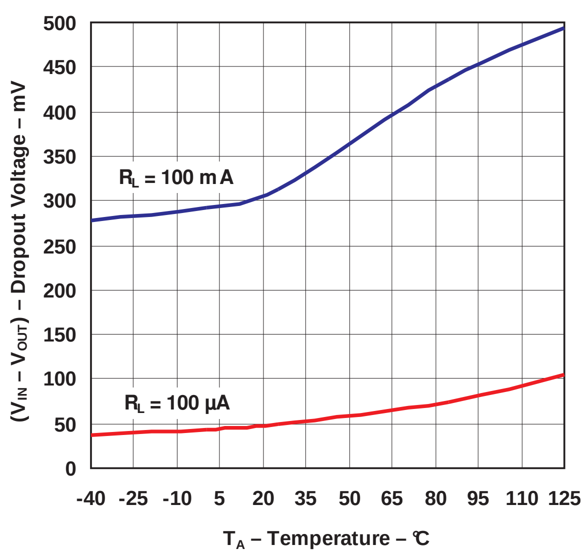
QUIESCENT CURRENT vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs TEMPERATURE

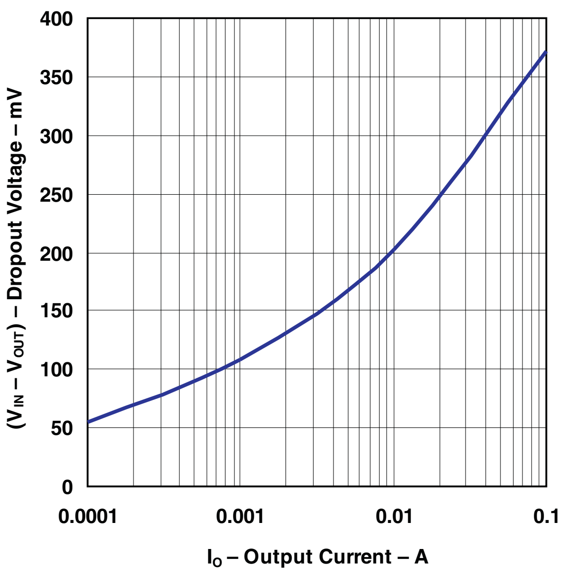


DROPOUT VOLTAGE vs TEMPERATURE

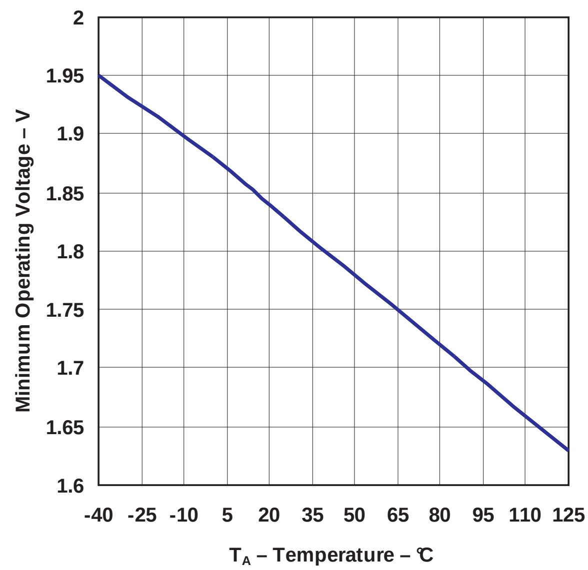


TYPICAL CHARACTERISTICS (continued)

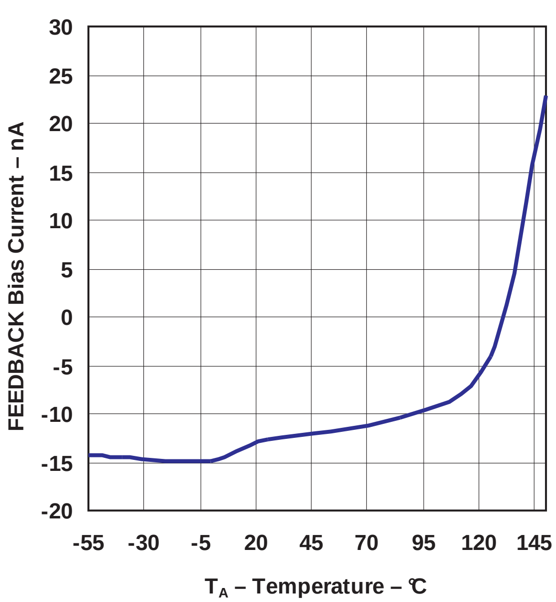
DROPOUT VOLTAGE vs OUTPUT CURRENT



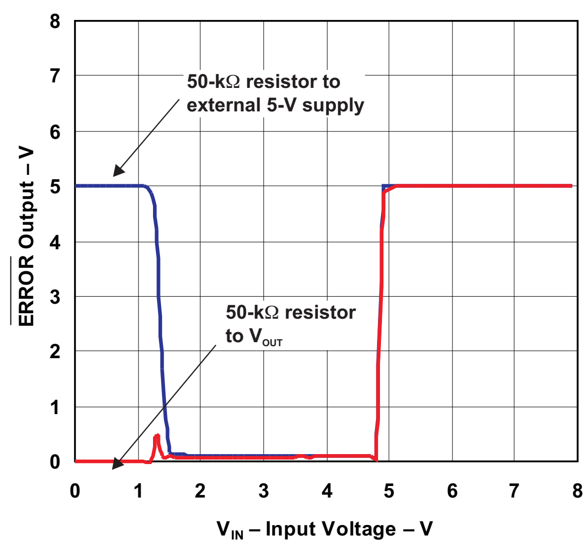
LP2951 MINIMUM OPERATING VOLTAGE vs TEMPERATURE



LP2951 FEEDBACK BIAS CURRENT vs TEMPERATURE

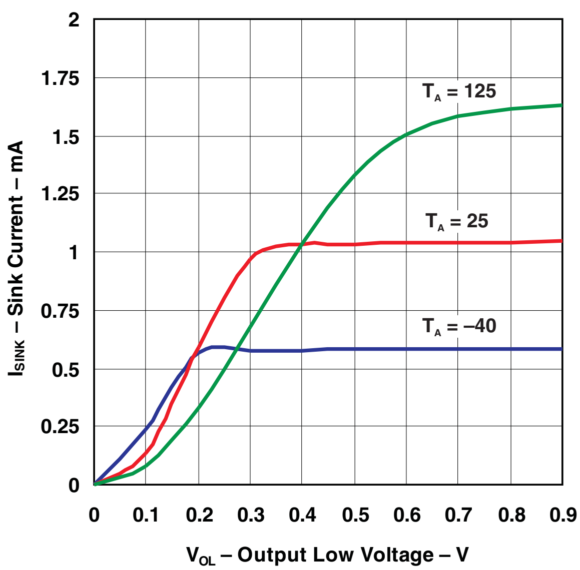


LP2951 $\overline{\text{ERROR}}$ COMPARATOR OUTPUT vs INPUT VOLTAGE

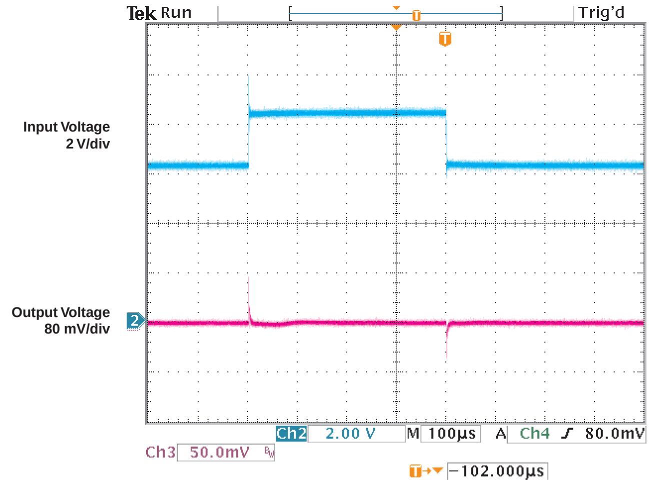


TYPICAL CHARACTERISTICS (continued)

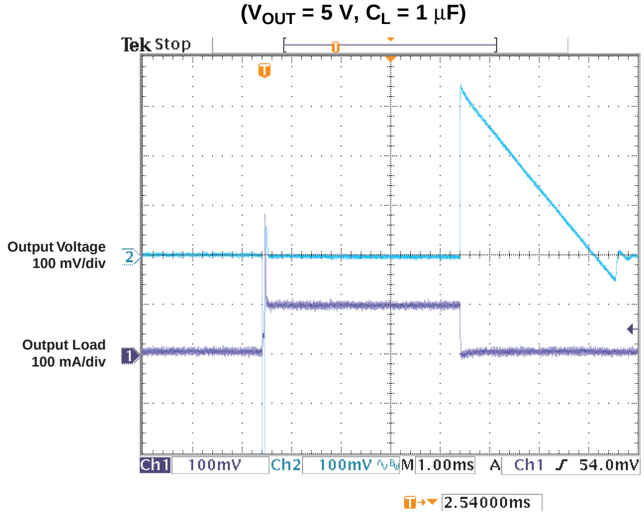
LP2951 ERROR COMPARATOR SINK CURRENT vs OUTPUT LOW VOLTAGE



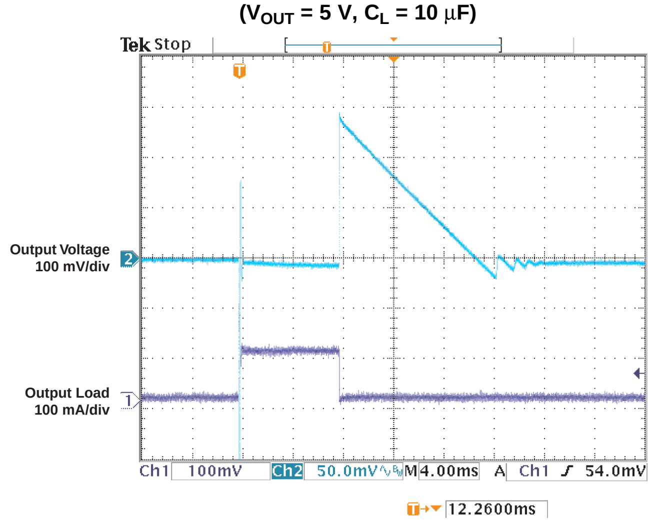
LINE TRANSIENT RESPONSE vs TIME



LOAD TRANSIENT RESPONSE vs TIME (V_{OUT} = 5 V, C_L = 1 µF)

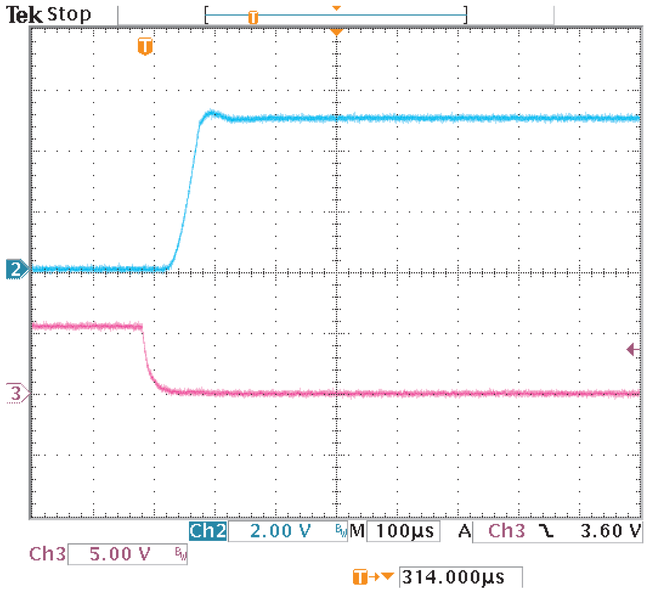


LOAD TRANSIENT RESPONSE vs TIME (V_{OUT} = 5 V, C_L = 10 µF)

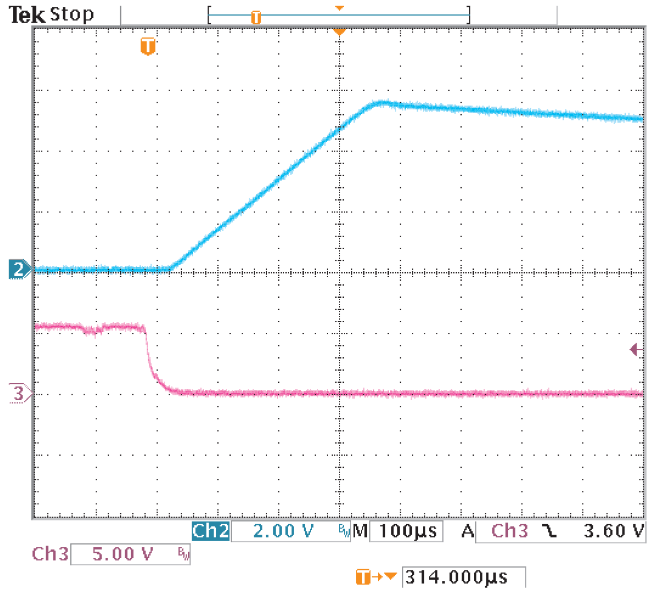


TYPICAL CHARACTERISTICS (continued)

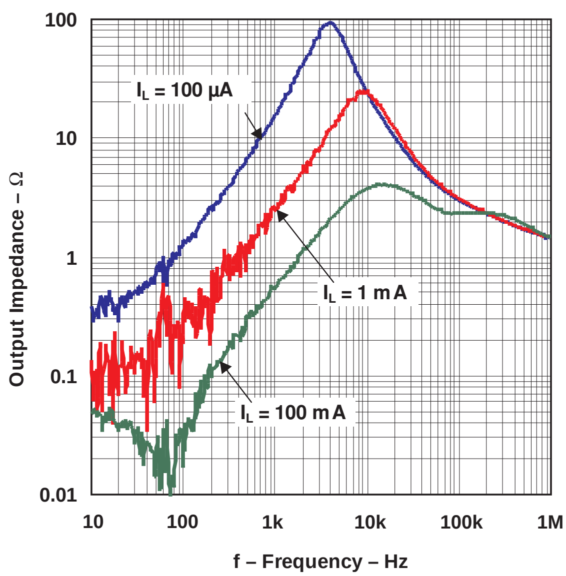
ENABLE TRANSIENT RESPONSE vs TIME (C_L = 1 µF, I_L = 1 mA)



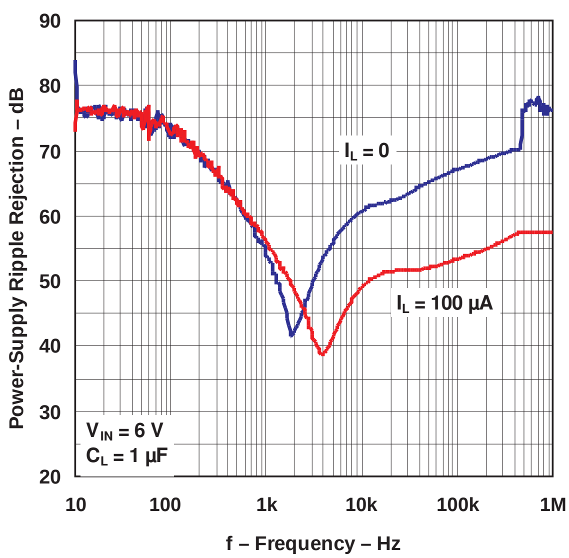
ENABLE TRANSIENT RESPONSE vs TIME (C_L = 10 µF, I_L = 1 mA)



OUTPUT IMPEDANCE vs FREQUENCY

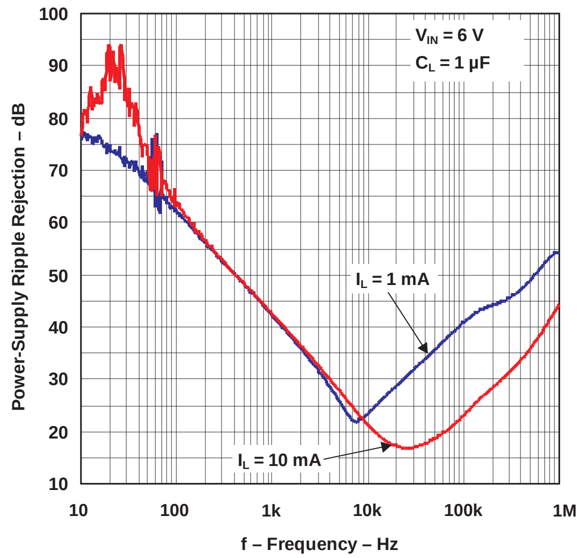


RIPPLE REJECTION vs FREQUENCY

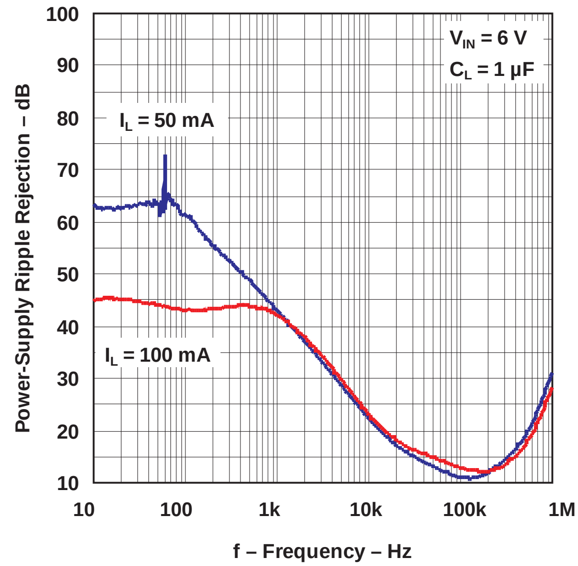


TYPICAL CHARACTERISTICS (continued)

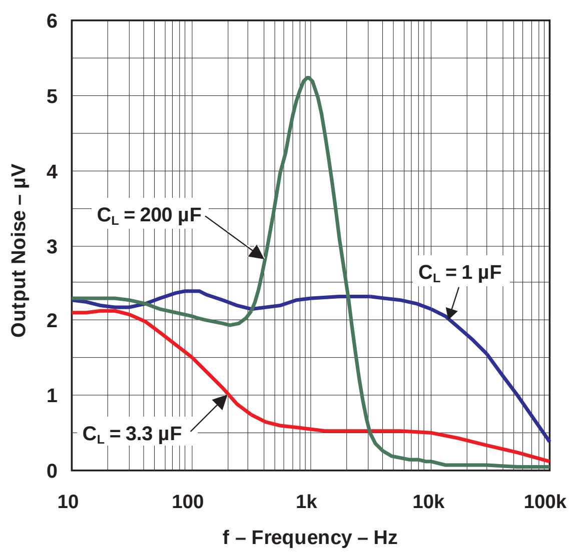
RIPPLE REJECTION vs FREQUENCY



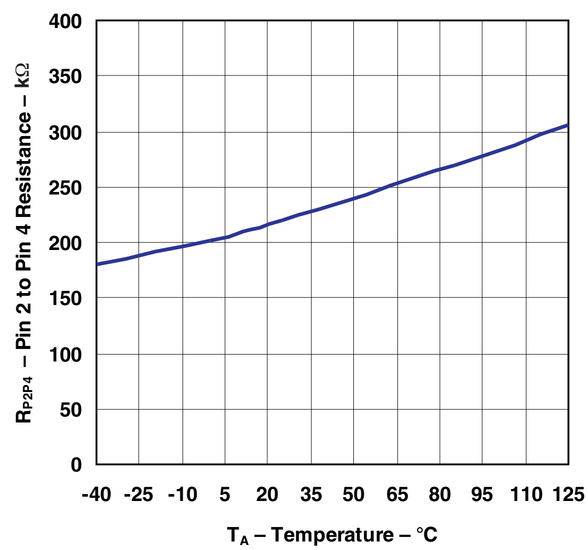
RIPPLE REJECTION vs FREQUENCY



LP2951 OUTPUT NOISE vs FREQUENCY

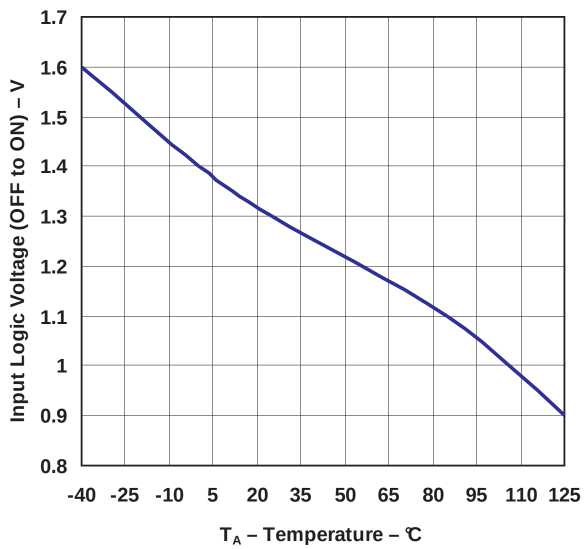


LP2951 DIVIDER RESISTANCE vs TEMPERATURE

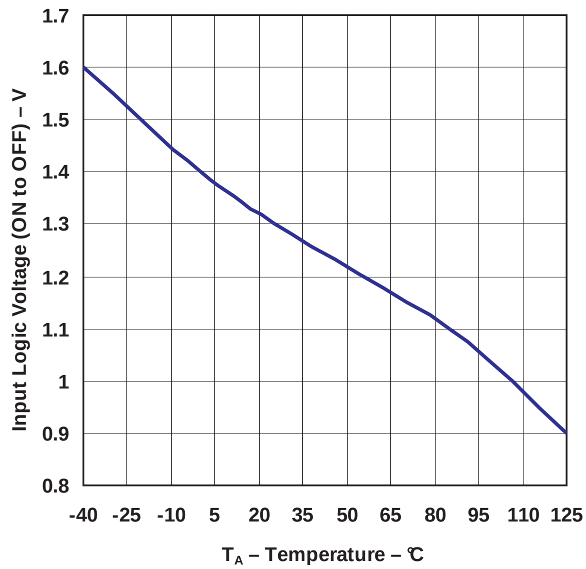


TYPICAL CHARACTERISTICS (continued)

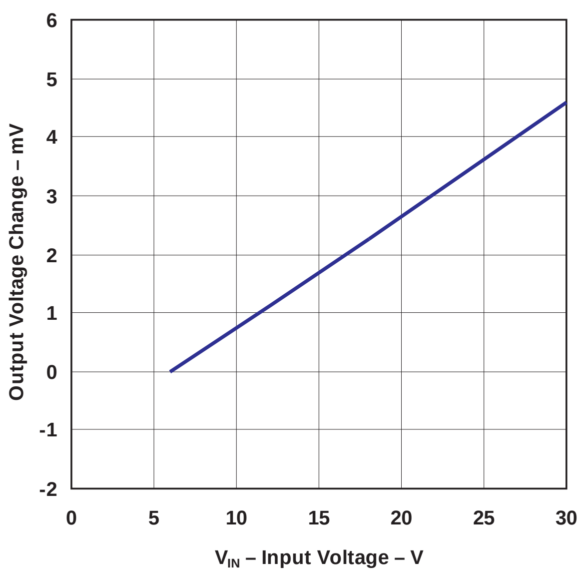
SHUTDOWN THRESHOLD VOLTAGE (OFF TO ON)
vs
TEMPERATURE



SHUTDOWN THRESHOLD VOLTAGE (ON TO OFF)
vs
TEMPERATURE



LINE REGULATION
vs
INPUT VOLTAGE



APPLICATION INFORMATION

Input Capacitor (C_{IN})

A 1-µF (tantalum, ceramic, or aluminum) electrolytic capacitor should be placed locally at the input of the LP2950 or LP2951 if there is, or will be, significant impedance between the ac filter capacitor and the input; for example, if a battery is used as the input or if the ac filter capacitor is located more than 10 in away. There are no ESR requirements for this capacitor, and the capacitance can be increased without limit.

Output Capacitor (C_{OUT})

As with most PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

Capacitance Value

For $V_{OUT} \geq 5$ V, a minimum of 1 µF is required. For lower V_{OUT}, the regulator 's loop gain is running closer to unity gain and, thus, has lower phase margins. Consequently, a larger capacitance is needed for stability. For V_{OUT} = 3 V or 3.3 V, a minimum of 2.2 µF is recommended. For worst case, V_{OUT} = 1.23 V (using the ADJ version), a minimum of 3.3 µF is recommended. C_{OUT} can be increased without limit and only improves the regulator stability and transient response. Regardless of its value, the output capacitor should have a resonant frequency less than 500 kHz.

The minimum capacitance values given above are for maximum load current of 100 mA. If the maximum expected load current is less than 100 mA, then lower values of C_{OUT} can be used. For instance, if $I_{OUT} < 10$ mA, then only 0.33 µF is required for C_{OUT}. For $I_{OUT} < 1$ mA, 0.1 µF is sufficient for stability requirements. Thus, for a worst-case condition of 100-mA load and $V_{OUT} = V_{REF}$ = 1.235 V (representing the highest load current and lowest loop gain), a minimum C_{OUT} of 3.3 µF is recommended.

For the LP2950, no load stability is inherent in the design — a desirable feature in CMOS circuits that are put in standby (such as RAM keep-alive applications). If the LP2951 is used with external resistors to set the output voltage, a minimum load current of 1 µA is recommended through the resistor divider.

ESR Range

The regulator control loop relies on the ESR of the output capacitor to provide a zero to add sufficient phase margin to ensure unconditional regulator stability; this requires the closed-loop gain to intersect the open-loop response in a region where the open-loop gain rolls off at 20 dB/decade. This ensures that the phase always is less than 180° (phase margin greater than 0°) at unity gain. Thus, a minimum-maximum range for the ESR must be observed.

The upper limit of this ESR range is established by the fact that too high an ESR could result in the zero occurring too soon, causing the gain to roll off too slowly, which, in turn allows a third pole to appear before unity gain and introduce enough phase shift to cause instability. This typically limits the max ESR to approximately 5 Ω.

Conversely, the lower limit of the ESR is tied to the fact that too low an ESR shifts the zero too far out (past unity gain) and, thus, allows the gain to roll off at 40 dB/decade at unity gain, with a resulting phase shift of greater than 180°. Typically, this limits the minimum ESR to approximately 20 mΩ to 30 mΩ.

For specific ESR requirements, see *Typical Characteristics* .

APPLICATION INFORMATION (continued)

Capacitor Types

Most tantalum or aluminum electrolytics are suitable for use at the input. Film-type capacitors also work, but at higher cost. When operating at low temperature, care should be taken with aluminum electrolytics, as their electrolytes often freeze at –30°C. For this reason, solid tantalum capacitors should be used at temperatures below –25°C.

Ceramic capacitors can be used, but due to their low ESR (as low as 5 mΩ to 10 mΩ), they may not meet the minimum ESR requirement previously discussed. If a ceramic capacitor is used, a series resistor between 0.1 Ω to 2 Ω must be added to meet the minimum ESR requirement. In addition, ceramic capacitors have one glaring disadvantage that must be taken into account — a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥2.2 µF) can lose more than half of its capacitance as temperature rises from 25°C to 85°C. Thus, a 2.2-µF capacitor at 25°C drops well below the minimum C_{OUT} required for stability as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2-µF required for stability for the entire operating temperature range.

C_{BYPASS}: Noise and Stability Improvement

In the LP2951, an external FEEDBACK pin directly connected to the error amplifier noninverting input can allow stray capacitance to cause instability by shunting the error amplifier feedback to GND, especially at high frequencies. This is worsened if high-value external resistors are used to set the output voltage, because a high resistance allows the stray capacitance to play a more significant role; i.e., a larger RC time delay is introduced between the output of the error amplifier and its FEEDBACK input, leading to more phase shift and lower phase margin. A solution is to add a 100-pF bypass capacitor (C_{BYPASS}) between OUTPUT and FEEDBACK; because C_{BYPASS} is in parallel with R1, it lowers the impedance seen at FEEDBACK at high frequencies, in effect offsetting the effect of the parasitic capacitance by providing more feedback at higher frequencies. More feedback forces the error amplifier to work at a lower loop gain, so C_{OUT} should be increased to a minimum of 3.3 µF to improve the regulator 'sphase margin.

C_{BYPASS} can be also used to reduce output noise in the LP2951. This bypass capacitor reduces the closed loop gain of the error amplifier at the high frequency, so noise no longer scales with the output voltage. This improvement is more noticeable with higher output voltages, because loop gain reduction is greatest. A suitable C_{BYPASS} is calculated as shown in Equation 1:

$$f_{(CBYPASS)} \simeq 200\text{ Hz} \rightarrow C_{BYPASS} = \frac{1}{2\pi \times R1 \times 200\text{ Hz}} \quad (1)$$

On the 3-pin LP2950, noise reduction can be achieved by increasing the output capacitor, which causes the regulator bandwidth to be reduced, therefore, eliminating high-frequency noise. However, this method is relatively inefficient, as increasing C_{OUT} from 1 µF to 220 µF only reduces the regulator 'soutput noise from 430 µV to 160 µV (over a 100-kHz bandwidth).

$\overline{\text{ERROR}}$ Function (LP2951 Only)

The LP2951 has a low-voltage detection comparator that outputs a logic low when the output voltage drops by ≈6% from its nominal value, and outputs a logic high when V_{OUT} has reached ≈95% of its nominal value. This 95% of nominal figure is obtained by dividing the built-in offset of ≈60 mV by the 1.235-V bandgap reference, and remains independent of the programmed output voltage. For example, the trip-point threshold ($\overline{\text{ERROR}}$ output goes high) typically is 4.75 V for a 5-V output and 11.4 V for a 12-V output. Typically, there is a hysteresis of 15 mV between the thresholds for high and low $\overline{\text{ERROR}}$ output.

A timing diagram is shown in Figure 1 for $\overline{\text{ERROR}}$ vs V_{OUT} (5 V), as V_{IN} is ramped up and down. $\overline{\text{ERROR}}$ becomes valid (low) when V_{IN} ≈ 1.3 V. When V_{IN} ≈ 5 V, V_{OUT} = 4.75 V, causing $\overline{\text{ERROR}}$ to go high. Because the dropout voltage is load dependent, the output trip-point threshold is reached at different values of V_{IN}, depending on the load current. For instance, at higher load current, $\overline{\text{ERROR}}$ goes high at a slightly higher value of V_{IN}, and vice versa for lower load current. The output-voltage trip point remains at ≈4.75 V, regardless of the load. Note that when V_{IN} ≤ 1.3 V, the $\overline{\text{ERROR}}$ comparator output is turned off and pulled high to its pullup voltage. If V_{OUT} is used as the pullup voltage, rather than an external 5-V source, $\overline{\text{ERROR}}$ typically is ≈1.2 V. In this condition, an equal resistor divider (10 kΩ is suitable) can be tied to $\overline{\text{ERROR}}$ to divide down the voltage to a valid logic low during any fault condition, while still enabling a logic high during normal operation.

APPLICATION INFORMATION (continued)

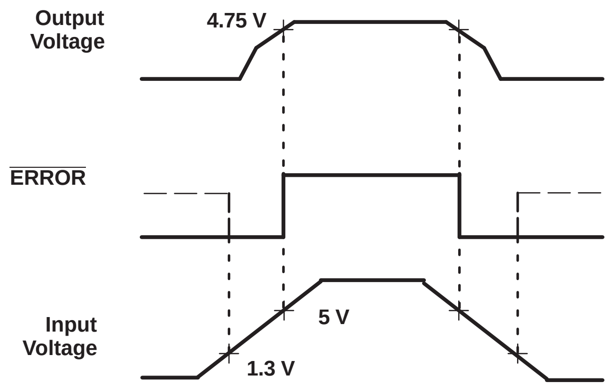


Figure 1. $\overline{\text{ERROR}}$ Output Timing

Because the $\overline{\text{ERROR}}$ comparator has an open-collector output, an external pullup resistor is required to pull the output up to V_{OUT} or another supply voltage (up to 30 V). The output of the comparator is rated to sink up to 400 µA. A suitable range of values for the pullup resistor is from 100 kΩ to 1 MΩ. If $\overline{\text{ERROR}}$ is not used, it can be left open.

Programming Output Voltage (LP2951 Only)

A unique feature of the LP2951 is its ability to output either a fixed voltage or an adjustable voltage, depending on the external pin connections. To output the internally programmed fixed voltage, tie the SENSE pin to the OUTPUT pin and the FEEDBACK pin to the V_{TAP} pin. Alternatively, a user-programmable voltage ranging from the internal 1.235-V reference to a 30-V max can be set by using an external resistor divider pair. The resistor divider is tied to V_{OUT}, and the divided-down voltage is tied directly to FEEDBACK for comparison against the internal 1.235-V reference. To satisfy the steady-state condition in which its two inputs are equal, the error amplifier drives the output to equal Equation 2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) - I_{FB}R_1 \tag{2}$$

Where:

- V_{REF} = 1.235 V applied across R2
- I_{FB} = FEEDBACK bias current, typically 20 nA

A minimum regulator output current of 1 µA must be maintained. Thus, in an application where a no-load condition is expected (for example, CMOS circuits in standby), this 1-µA minimum current must be provided by the resistor pair, effectively imposing a maximum value of R2 = 1.2 MΩ (1.235 V/1.2 MΩ ≈ 1 µA).

I_{FB} = 20 nA introduces an error of ≈0.02% in V_{OUT}. This can be offset by trimming R1. Alternatively, increasing the divider current makes I_{FB} less significant, thus, reducing its error contribution. For instance, using R2 = 100 kΩ reduces the error contribution of I_{FB} to 0.17% by increasing the divider current to ≈12 µA. This increase in the divider current still is small compared to the 600-µA typical quiescent current of the LP2951 under no load.

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