



Hi3559A V100 ultra-HD Mobile Camera SoC

Brief Data Sheet

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Introduction

Hi3559A V100 is a professional 8K ultra-HD mobile camera SoC. It supports 8K30/4K120 digital video recording with broadcast-level picture quality. It also supports multiple sensor inputs as well as the H.265 encoding output or movie-level raw data output. It integrates the high-performance ISP and employs the advanced low-power process and architecture design. Hi3559A V100 provides excellent image processing capability.

Hi3559A V100 supports the industry-leading multi-channel 4K sensor inputs, multi-channel ISP image processing, HDR10 technology standard, and multi-channel panoramic hardware splicing. When supporting 8K30/4K120 video recording, Hi3559A V100 provides the 6-DOF DIS hardware, which reduces its dependence on the mechanical head.

Hi3559A V100 provides efficient and rich computing resources to assist customers in developing consumer applications and industry applications. Hi3559A V100 integrates the dual-core A73 processor and dual-core A53 processor as well as the big.LITTLE architecture and dual operating systems, achieving balance between the power consumption and startup time.

Hi3559A V100 supports the product miniaturization design because it uses the advanced 12 nm low-power process and miniaturization package and supports DDR4/LPDDR4 SDRAMs.

With the stable and easy-to-use mobile SDK design provided by HiSilicon, Hi3559A V100 can assist customers in rapid product mass production.

Key Features

- **Low Power Consumption**
Typical power consumption of 3 W in 8KP30 (7680 x 4320)+1080P30 H.265 encoding mode
- **Miniaturization Package**
25 mm x 25 mm (0.98 in. x 0.98 in.) FC-BGA package
- **8K30/4K120 Encoding**
8KP30+1080P30 or 4KP120+1080P30 H.265 encoding
- **Multi-Channel Video Recording**
2x4KP60, 4x4KP30, or 8x1080P30 video recording, supporting hardware splicing within the camera
- **High-Speed Memory Interfaces**
USB 3.0 or PCIe 2.0 high-speed interface
UFS and eMMC interfaces
- **RAW Video Output**
Professional 4KP30 raw video output
- **Visual Computing Processing Capability**



Key Specifications

Processor Core

- Dual-core ARM Cortex A73@1.8 GHz, 32 KB I cache, 64 KB D cache or 512 KB L2 cache
- Dual-core ARM Cortex A53@1.2 GHz, 32 KB I cache, 32 KB D cache or 256 KB L2 cache
- Single-core ARM Cortex A53@1 GHz, 32 KB I cache, 32 KB D cache or 128 KB L2 cache
- Neon acceleration and integrated FPU

GPU

- Dual-core ARM Mali G71@900 MHz, 256 KB cache
- OpenCL 1.1/1.2/2.0
- OpenGL ES 3.0/3.1/3.2

Sensor Hub

- Integrated ARM Cortex M7@192 MHz
- Integrated PMC, which supports only external reset
- Internal POR
- General peripheral IPs (UART, SPI, I²C, PWM, GPIO, and LSADC)
- 2-channel LSADC, seven UART interfaces, and eight PWM interfaces

Video Encoding

- H.264 BP/MP/HP
- H.265 Main Profile/Main 10 Profile
- I/P/B frame supported in H.264/H.265 encoding mode
- MJPEG/JPEG Baseline encoding
- A maximum of 8192 x 8640 resolution for H.264 encoding
- A maximum of 16384 x 8640 resolution for H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capability:
 - 7680 x 4320@30 fps+1080p@30 fps+7680 x 4320@2 fps snapshot
- Maximum JPEG snapshot performance of 7680 x 4320@15 fps
- CBR, VBR, AVBR, FIXQP, and QPMAP bit rate control modes
- Maximum 200 Mbit/s output bit rate
- Encoding of eight ROIs

Video Decoding

- H.264 BP/MP/HP
- H.265 Main Profile/Main 10 Profile
- JPEG/MJPEG decoding
- Maximum video decoding performance of H.264/H.265 7680 x 4320@30 fps or H.264/H.265 3840 x 2160@120 fps
- Maximum 7680 x 4320@15 fps JPEG decoding

Intelligent Video Processing

- Visual computing processing capability
- Quad-core DSP@700 MHz, 32 KB I cache, 32 KB IRAM, or 512 KB DRAM
- Dual-core NNIE@840 MHz neural network acceleration

engine

- Internal dual-sensor depth detection unit

Video and Graphics Processing

- Anti-flicker for output videos and graphics
- 1/15.5x to 16x video scaling
- 360° or 720° panoramic stitching of up to 6-channel videos
- 1/15.5x to 16x graphics scaling
- OSD overlaying of eight regions before encoding
- Video graphics overlaying of two layers (video layer and graphics layer)

ISP

- 2-channel independent ISP processing of video inputs from multiple sensors in TDM mode
- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- Highlight suppression, backlight compensation, gamma correction, and color enhancement
- DPC, NR, and 6-DOF DIS
- 3DNR, image enhancement, and DCI
- Anti-fog
- LDC and fisheye correction
- Picture rotation by 90° or 270°
- Picture mirror and flip
- HDR10
- BT.2020 WCG
- Sensor built-in WDR, 4F/3F/2F frame-based/line-based WDR and local tone mapping
- ISP tuning tools for the PC

Audio Encoding and Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- G.711, G.726, AAC, and other audio encoding formats
- Audio 3A functions (AEC, ANR, and ALC)

Security Engine

- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA1024/2048/3072/4096 signature verification algorithm implemented by using hardware
- HASH-SHA1/224/256/384/512 and HMAC_SHA1/224/256/384/512 tamper proofing algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and hardware random number generator

Video Interfaces

- VI interfaces
 - Eight sensor inputs
 - Maximum 32-megapixel (7680 x 4320) or 36-megapixel (6000 x 6000) resolution
 - 8-/10-/12-/14-bit RGB Bayer DC timing VI, up to 150 MHz clock frequency
 - BT.601, BT.656, and BT.1120 VI interfaces
 - Maximum 16-lane MIPI/LVDS/sub-

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LVDS/HiSPi/SLVS-EC interface for the serial sensor inputs

- Maximum 8-channel video inputs for the serial sensor inputs, supporting various working modes such as 1x16-lane/2x8-lane/4x4-lane/2x4-lane+4x2-lane/8x2Lane
- Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
- Programmable sensor clock output
- VO interfaces
 - HDMI 2.0, supporting maximum 4K@60 fps output
 - 6-/8-/16-/24-bit RGB digital LCD output, supporting maximum 1920 x 1080@60 fps output
 - 4-lane MIPI DSI output, supporting maximum 2.5 Gbit/s per lane frequency

Audio Interfaces

- Integrated audio codec, supporting 16-bit audio inputs and outputs
- I²S interface for connecting to the external audio codec
- Dual-channel differential MIC inputs for reducing background noises

Peripheral Interfaces

- POR
- External reset input
- Internal RTC
- Integrated 2-channel LSADC
- Five UART interfaces
- IR interface, I²C interface, SSP main interface, and GPIO interface
- Integrated two GMACs, supporting RGMII/RMII
- Two PWM interfaces
- Two SD 3.0/SDIO 3.0 interfaces and an SD 2.0 interface
- Two USB 3.0/USB 2.0 host/device ports
- 2-lane PCIe 2.0 RC/EP mode

External Memory Interfaces

- DDR4/LPDDR4 interface
 - 64-bit DDR4
 - 2x 32-bit LPDDR4 SDRAMs
 - Maximum capacity of 8 GB
- SPI NOR flash interface
 - 1-/2-/4-line mode
 - 3-byte or 4-byte address mode
 - Maximum capacity of 32 MB
- SPI NAND flash interface
 - Maximum capacity of 512 MB
- NAND flash interface
 - 8-bit data width
 - SLC or MLC
 - 4-/8-/16-/24-/28-/40-/64-bit ECC
- eMMC 5.1 interface
 - Maximum capacity of 2 TB
- UFS 2.1 interface
 - Maximum capacity of 512 GB
- Booting from the SPI NOR flash, SPI NAND flash, or NAND flash
- Booting from an eMMC or UFS

SDK

- Linux SMP
- Linux+Huawei LiteOS dual-system AMP
- Client for the iOS and Android mobile phones, and high-performance H.265 decoding library

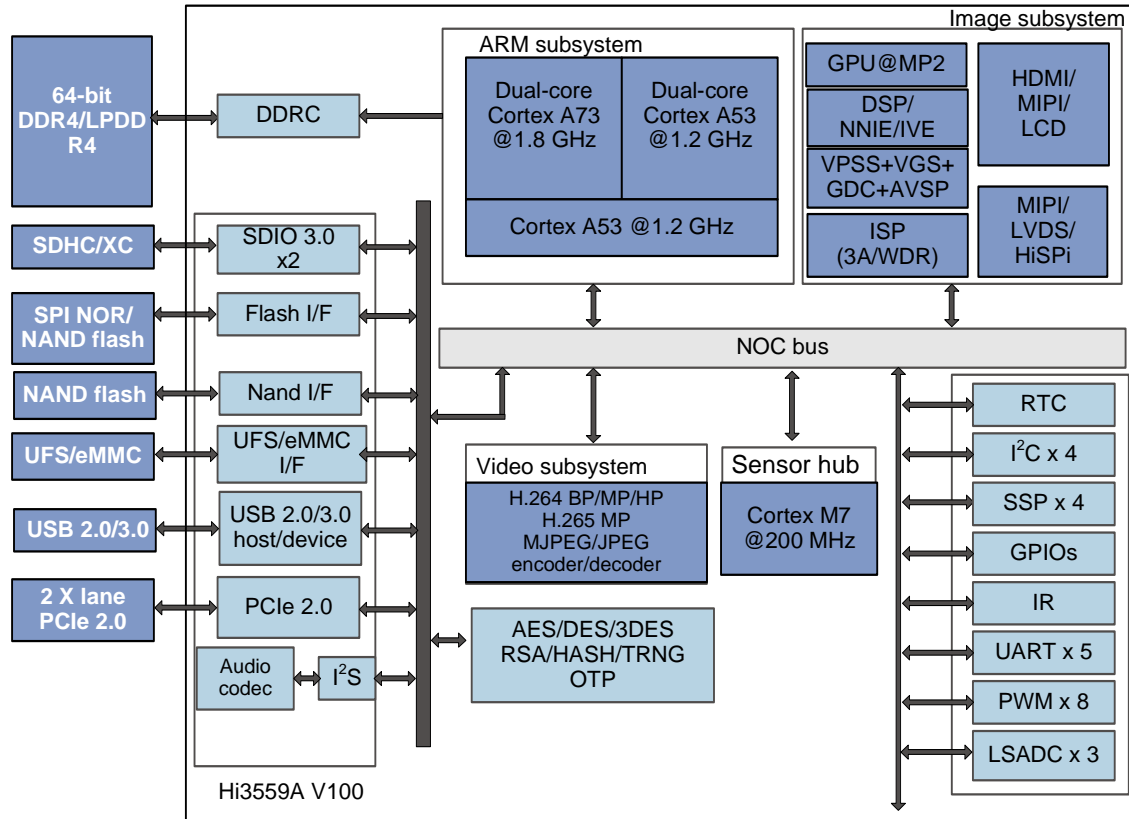
Physical Specifications

- Power Consumption
 - Typical power consumption of 3 W
 - Multi-level power saving mode
- Operating voltages
 - 0.8 V core voltage
 - 1.8 V I/O voltage
 - 1.2 V DDR4 SDRAM interface voltage
 - 1.1 V LPDDR4 SDRAM interface voltage
- Package
 - RoHS, FC-BGA
 - Body size of 25 mm x 25 mm (0.98 in. x 0.98 in.)
 - Lead pitch of 0.65 mm (0.03 in.)



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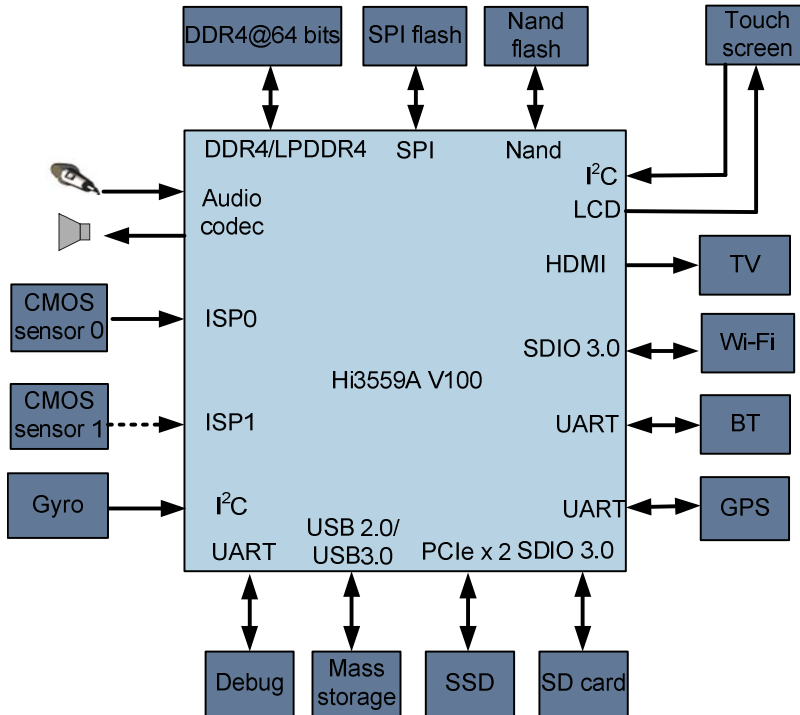
Functional Block Diagram





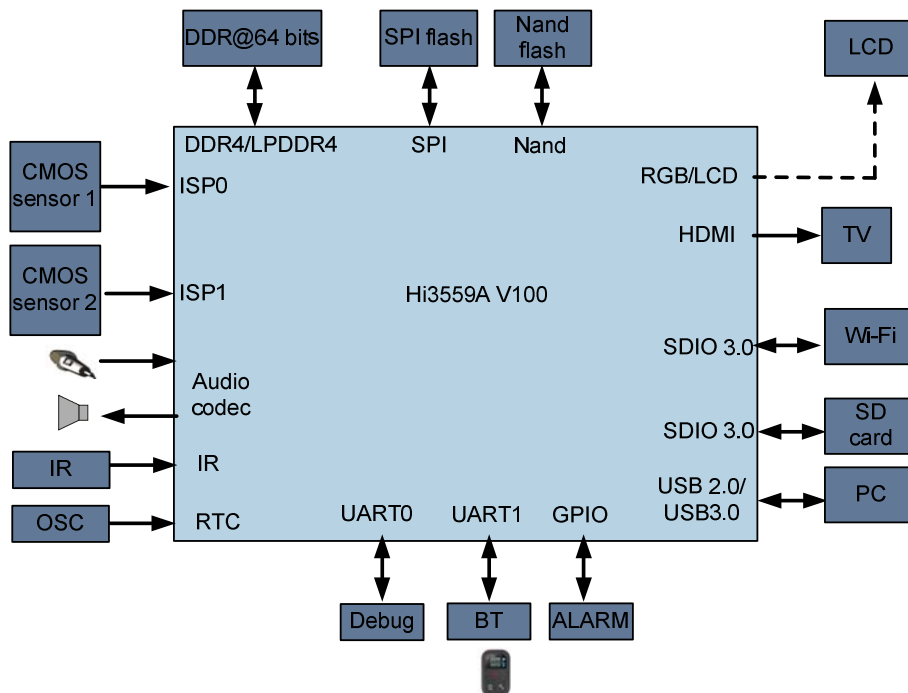
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Hi3559A V100 Mobile Camera and Professional Camera Solution



- Advanced 8K30 6-DOF video DIS
- 10-bit video, supporting HDR10
- Up to 10 Gbit/s rate of the 2-lane PCIe 2.0 interface, supporting 4KP30 RAW video output
- DDR4/LPDDR4 SDRAMs
- Two SDIO 3.0 interfaces, extended low-power Wi-Fi module, and the external SDXC card
- Dual MICs and advanced dual-MIC NR algorithm

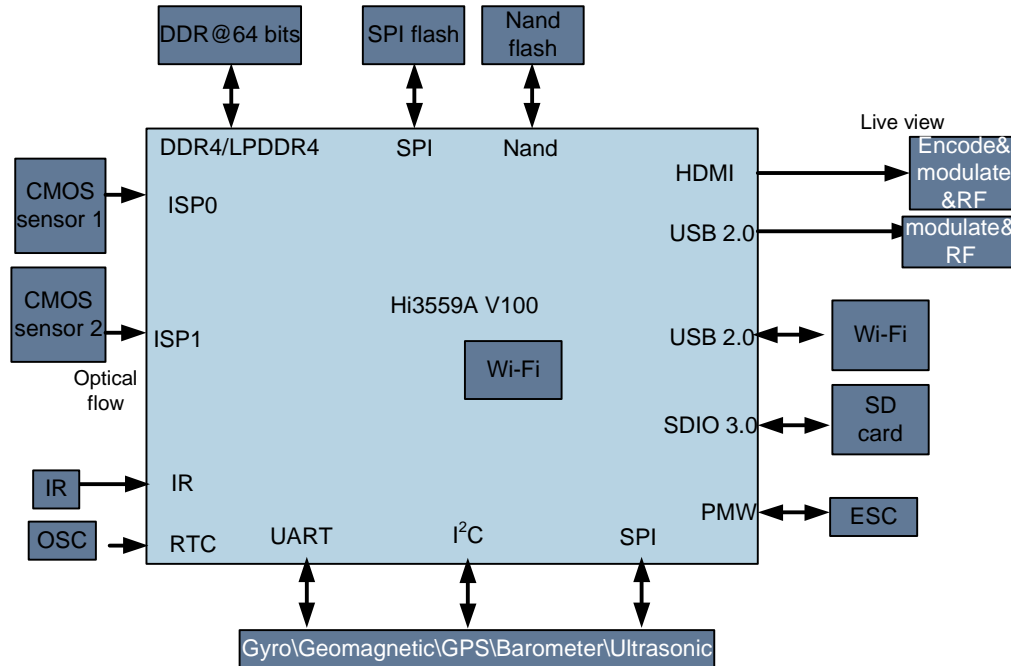
Hi3559A V100 3D/VR Camera Solution



- Dual-channel 4K60fps input, 4-channel 3K x 3K input, or 8-channel 1080p input, supporting multi-channel hardware splicing
- 10-bit video, supporting HDR10
- DDR4/LPDDR4 SDRAMs
- Two SDIO 3.0 interfaces, extended low-power Wi-Fi module, and the external SDXC card
- Dual MICs and advanced dual-MIC NR algorithm



Hi3559A V100 Flying Camera Solution



- 6-DOF 4KP60 video DIS in the gyro auxiliary information
- 10-bit video, supporting HDR10
- 4KP30 RAW video output
- DDR4/LPDDR4 SDRAMs
- Dual sensor inputs for bidirectional vision hovering and obstacle avoidance
- Various UART, I²C, and SPI interfaces for connecting the gyro, GPS, and barometer, implementing the flight control algorithm on Hi3559A V100
- 4-channel PWM signal outputs to the ESC
- Real-time HDMI video outputs for image transmission



Acronyms and Abbreviations

3DES	triple data encryption standard
AAC	advanced audio coding
AE	automatic exposure
AEC	acoustic echo cancellation
AES	advanced encryption standard
AF	automatic focus
ALC	automatic level control
AMP	asymmetric multiprocessing
ANR	audio noise reduction
AVBR	adaptive variable bit rate
AWB	automatic white balance
CBR	constant bit rate
CMOS	complementary metal-oxide-semiconductor
codec	coder/decoder
DCI	dynamic contrast improvement
DDR	double data rate
DES	data encryption standard
DIS	digital image stabilization
DOF	degree of freedom
DPC	defect pixel correction
DRAM	dynamic random access memory
DSI	display serial interface
DSP	digital signal processor
eMMC	embedded multimedia card
EP	end point
ESC	electronic speed control
FPN	fixed pattern noise
FPU	floating-point unit
RoHS	Restriction of Hazardous Substances
GMAC	Gigabit Ethernet Media Access Controller
GPIO	general-purpose input/output
GPS	Global Positioning System
GPU	graphics processing unit
HD	high definition
HMAC	hashed message authentication code
HDMI	high definition multimedia interface
HDR	high dynamic range
HiSPi	high-speed serial pixel interface
I ² C	inter-integrated circuit
I ² S	inter-IC sound
IR	infrared
ISP	image signal processor
LCD	liquid crystal display
LDC	lens distortion correction
LPDDR	low-power double data rate
LSADC	low-speed analog-to-digital converter
LVDS	low-voltage differential signaling
MIC	microphone
MIPI	mobile industry processor interface
MLC	multi-level cell
NNIE	Neural Network Inference Engine

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NR	noise reduction
OSD	on-screen display
OTP	one-time programming
PCIe	peripheral component interconnect express
PMC	power management controller
POR	power-on reset
PWM	pulse-width modulation
RC	root complex
RGB	red-green-blue
RGMII	reduced gigabit media independent interface
RoHS	Restriction of Hazardous Substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SD	secure digital
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SDXC	secure digital extended capacity
SLC	single-level cell
SLVS-EC	Scalable Low Voltage Signaling interface with Embedded Clock
SoC	system-on-chip
SMP	symmetric multiprocessing
SPI	serial peripheral interface
SSP	synchronous serial port
SVP	Smart Vision Process
TDM	time division multiplexing
UART	universal asynchronous receiver transmitter
UFS	Universal Flash Storage
VBR	variable bit rate
VI	video input
VO	video output
VR	virtual reality
WCG	wide color gamut
WDR	wide dynamic range

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