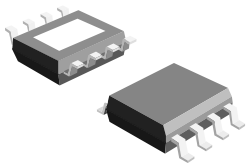
DDR Termination Regulator TJ2998

FEATURES

- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors required
- Linear Topology
- Suspend to RAM (STR) functionality
- Low External Component Count
- Thermal Shutdown
- Under Voltage Lockout and Over Current Limit
- Available in SOP8, SOP8-PP Packages

SOP8 / SOP8-PP PKG



APPLICATIONS

- DDR 2/3/3L/4 Termination Voltage
- SSTL Termination
- HSTL Termination

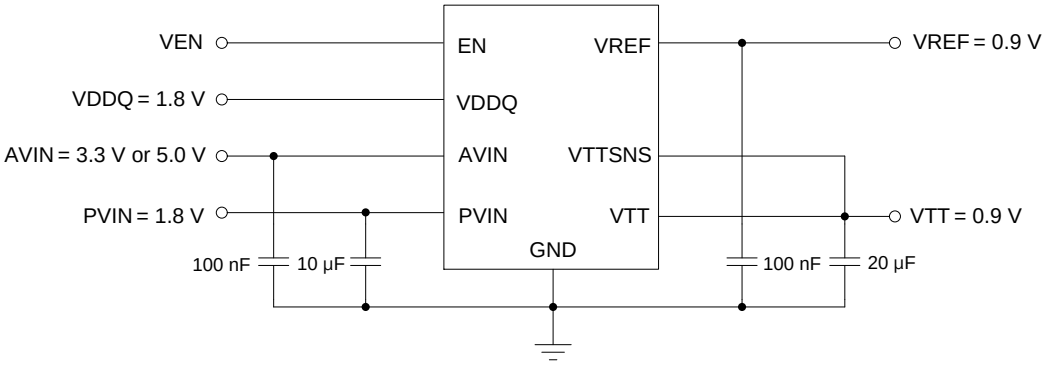
ORDERING INFORMATION

Device	Package
TJ2998GD	SOP8
TJ2998GDP	SOP8-PP

DESCRIPTION

The TJ2998 linear regulator is designed to meet the JEDEC SSTL specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering up to 2A continuous current and transient peaks up to 3A with respect to PVIN operating condition in the application as required for DDR-SDRAM termination. The TJ2998 also incorporates a VTTSNS pin to provide superior load regulation and a VREF output as a reference for the chipset and DIMMs. An additional feature found on the TJ2998 is an active high enable (EN) pin that provides Suspend To RAM (STR) functionality. When EN is pulled low the VTT output will tri-state providing a high impedance output, but, VREF will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

TYPICAL APPLICATION



Please contact us for more information about this product.

单击下面可查看定价，库存，交付和生命周期等信息

>>HTC(泰进)