

# Smart High-Side Power Switch

## Two Channels: 2 x 30mΩ

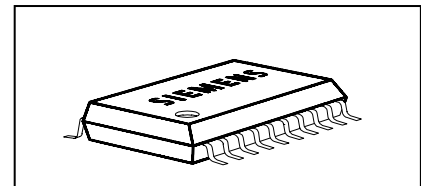
### Current Sense



#### Product Summary

Operating Voltage	$V_{bb(ON)}$	5.0...34V	
	Active channels	one	two parallel
On-state Resistance	$R_{ON}$	30mΩ	15mΩ
Nominal load current	$I_{L(NOM)}$	5.5A	8.5A
Current limitation	$I_{L(SCr)}$	24A	24A

#### Package



PG-DSO20

#### General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input, diagnostic feedback and proportional load current sense monolithically integrated in Smart SIPMOS<sup>®</sup> technology.
- Providing embedded protective functions

#### Applications

- $\mu$ C compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

#### Basic Functions

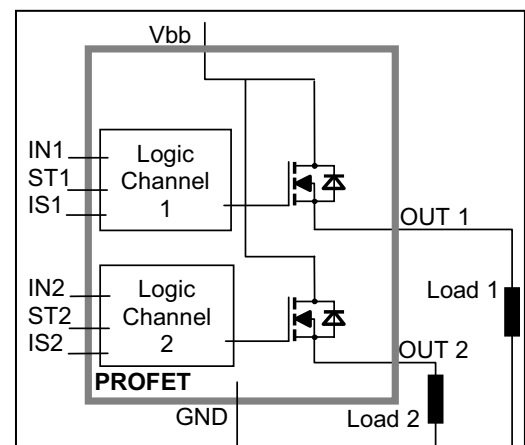
- CMOS compatible input
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Fast demagnetization of inductive loads
- Logic ground independent from load ground

#### Protection Functions

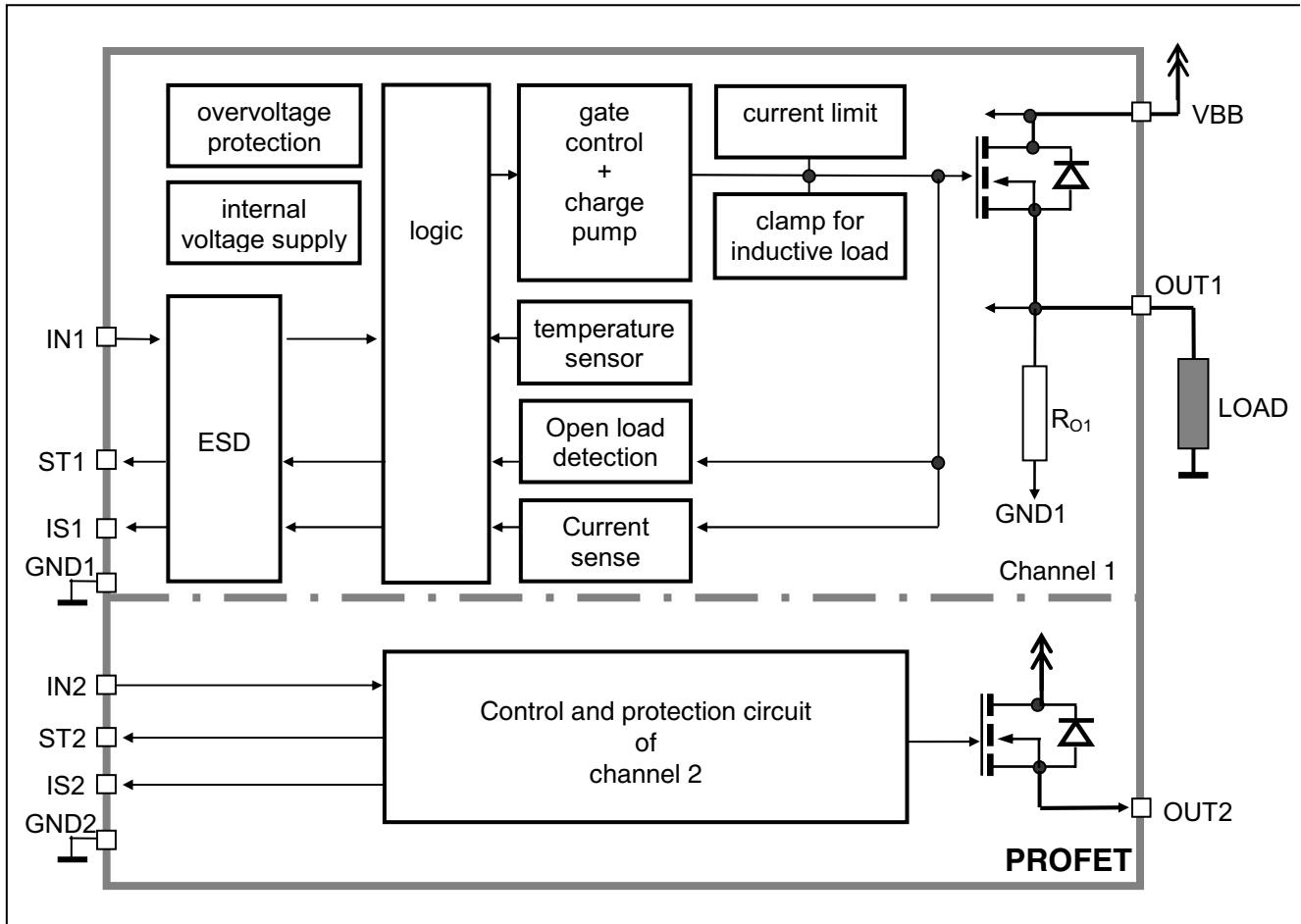
- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of  $V_{bb}$  protection
- Electrostatic discharge protection (ESD)

#### Diagnostic Functions

- Proportional load current sense
- Diagnostic feedback with open drain output
- Open load detection in OFF-state with external resistor
- Feedback of thermal shutdown in ON-state



### Functional diagram

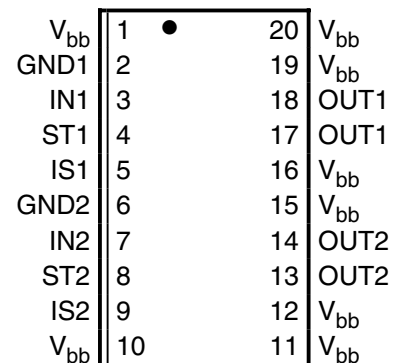


### Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	$V_{bb}$	<b>Positive power supply voltage.</b> Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	<b>Input 1,2,</b> activates channel 1,2 in case of logic high signal
7	IN2	
17,18	OUT1	<b>Output 1,2,</b> protected high-side power output of channel 1,2. Both pins of each output have to be connected in parallel for operation according to the spec (e.g. $k_{iis}$ ). Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	<b>Diagnostic feedback 1,2</b> of channel 1,2, open drain, inverts to input level
8	ST2	
2	GND1	<b>Ground 1</b> of chip 1 (channel 1)
6	GND2	<b>Ground 2</b> of chip 2 (channel 2)
5	IS1	<b>Sense current output 1,2;</b> proportional to the load current, zero in the case of current limitation of the load current
9	IS2	

### Pin configuration

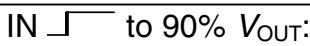
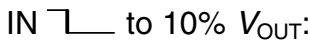
(top view)





Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

### Load Switching Capabilities and Characteristics

On-state resistance ( $V_{bb}$ to OUT); $I_L = 5\text{ A}$ each channel, $T_j = 25^\circ\text{C}$ : $T_j = 150^\circ\text{C}$ : two parallel channels, $T_j = 25^\circ\text{C}$ :	$R_{ON}$	--	27 54 14	30 60 15	m $\Omega$
Output voltage drop limitation at small load currents, see page 14 $I_L = 0.5\text{ A}$ $T_j = -40\dots+150^\circ\text{C}$ :	$V_{ON(NL)}$	--	50	--	mV
Nominal load current one channel active: two parallel channels active: Device on PCB <sup>6)</sup> , $T_a = 85^\circ\text{C}$ , $T_j \leq 150^\circ\text{C}$	$I_{L(NOM)}$	4.9 7.8	5.5 8.5	--	A
Output current while GND disconnected or pulled up <sup>7)</sup> ; $V_{bb} = 30\text{ V}$ , $V_{IN} = 0$ , see diagram page 10	$I_{L(GNDhigh)}$	--	--	8	mA
Turn-on time <sup>8)</sup> IN  to 90% $V_{OUT}$ :	$t_{on}$	25	70	150	$\mu\text{s}$
Turn-off time IN  to 10% $V_{OUT}$ : $R_L = 12\ \Omega$	$t_{off}$	25	80	200	$\mu\text{s}$
Slew rate on <sup>8)</sup> 10 to 30% $V_{OUT}$ , $R_L = 12\ \Omega$ :	$dV/dt_{on}$	0.1	--	1	V/ $\mu\text{s}$
Slew rate off <sup>8)</sup> 70 to 40% $V_{OUT}$ , $R_L = 12\ \Omega$ :	$-dV/dt_{off}$	0.1	--	1	V/ $\mu\text{s}$

### Operating Parameters

Operating voltage <sup>9)</sup>	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown	$V_{bb(under)}$	3.2	--	5.0	V
Undervoltage restart $T_j = -40\dots+25^\circ\text{C}$ : $T_j = +150^\circ\text{C}$ :	$V_{bb(u\ rst)}$	--	4.5	5.5 6.0	V
Undervoltage restart of charge pump see diagram page 13 $T_j = -40\dots+25^\circ\text{C}$ : $T_j = 150^\circ\text{C}$ :	$V_{bb(ucp)}$	--	4.7	6.5 7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.5	--	V
Overvoltage shutdown	$V_{bb(over)}$	34	--	43	V
Overvoltage restart	$V_{bb(o\ rst)}$	33	--	--	V

<sup>6)</sup> Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70 $\mu\text{m}$  thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 15

<sup>7)</sup> not subject to production test, specified by design

<sup>8)</sup> See timing diagram on page 11.

<sup>9)</sup> At supply voltage increase up to  $V_{bb} = 4.7\text{ V}$  typ without charge pump,  $V_{OUT} \approx V_{bb} - 2\text{ V}$

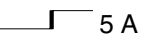
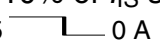
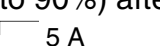


Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	values			Unit
		min	typ	max	

### Reverse Battery

Reverse battery voltage <sup>15)</sup>	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ( $V_{out} > V_{bb}$ ) $I_L = -4.0\text{ A}$ , $T_j = +150^\circ\text{C}$	$-V_{ON}$	--	600	--	mV

### Diagnostic Characteristics

Current sense ratio <sup>16)</sup> , static on-condition, $V_{IS} = 0\dots5\text{ V}$ , $V_{bb(on)} = 6.5^{17)}\dots27\text{V}$ , $k_{ILIS} = I_L / I_{IS}$ $T_j = -40^\circ\text{C}$ , $I_L = 5\text{ A}$ : $T_j = -40^\circ\text{C}$ , $I_L = 0.5\text{ A}$ : $T_j = 25\dots+150^\circ\text{C}$ , $I_L = 5\text{ A}$ : $T_j = 25\dots+150^\circ\text{C}$ , $I_L = 0.5\text{ A}$ :	$k_{ILIS}$	4350 3100 4350 3800	4800 4800 4800 4800	5800 7800 5350 6300	
Current sense output voltage limitation $T_j = -40\dots+150^\circ\text{C}$ $I_{IS} = 0$ , $I_L = 5\text{ A}$ :	$V_{IS(lim)}$	5.4	6.1	6.9	V
Current sense leakage/offset current $T_j = -40\dots+150^\circ\text{C}$ $V_{IN}=0$ , $V_{IS} = 0$ , $I_L = 0$ : $V_{IN}=5\text{ V}$ , $V_{IS} = 0$ , $I_L = 0$ : $V_{IN}=5\text{ V}$ , $V_{IS} = 0$ , $V_{OUT} = 0$ (short circuit)	$I_{IS(LL)}$ $I_{IS(LH)}$ $I_{IS(SH)}^{18)}$	0 0 0	-- -- --	1 15 10	$\mu\text{A}$
Current sense settling time to $I_{IS\text{ static}} \pm 10\%$ after positive input slope <sup>18)</sup> , $I_L = 0$  5 A	$t_{son(IS)}$	--	--	300	$\mu\text{s}$
Current sense settling time to 10% of $I_{IS\text{ static}}$ after negative input slope <sup>18)</sup> , $I_L = 5$  0 A	$t_{soff(IS)}$	--	30	100	$\mu\text{s}$
Current sense rise time (60% to 90%) after change of load current <sup>18)</sup> $I_L = 2.5$  5 A	$t_{slc(IS)}$	--	10	--	$\mu\text{s}$
Open load detection voltage <sup>19)</sup> (off-condition)	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (pin 17,18 to 2 resp. 13,14 to 6), $V_{OUT}=5\text{ V}$	$R_O$	5	15	40	k $\Omega$

<sup>15)</sup> Requires a 150  $\Omega$  resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 9).

<sup>16)</sup> This range for the current sense ratio refers to all devices. The accuracy of the  $k_{ILIS}$  can be raised at least by a factor of two by matching the value of  $k_{ILIS}$  for every single device.  
In the case of current limitation the sense current  $I_{IS}$  is zero and the diagnostic feedback potential  $V_{ST}$  is High. See figure 2c, page 12.



<sup>17)</sup> Valid if  $V_{bb(u\text{ rst})}$  was exceeded before.

<sup>18)</sup> not subject to production test, specified by design

<sup>19)</sup> External pull up resistor required for open load detection in off state

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

**Input and Status Feedback<sup>20)</sup>**

Input resistance (see circuit page 9)	$R_i$	3.0	4.5	7.0	k $\Omega$
Input turn-on threshold voltage 	$V_{IN(T+)}$	--	--	3.5	V
Input turn-off threshold voltage 	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current $V_{IN} = 0.4\text{ V}$ :	$I_{IN(off)}$	1	--	50	$\mu\text{A}$
On state input current $V_{IN} = 5\text{ V}$ :	$I_{IN(on)}$	20	50	90	$\mu\text{A}$
Delay time for status with open load after Input neg. slope (see diagram page 13)	$t_{d(ST\ OL3)}$	--	400	--	$\mu\text{s}$
Status delay after positive input slope (not subject to production test, specified by design)	$t_{don(ST)}$	--	13	--	$\mu\text{s}$
Status delay after negative input slope (not subject to production test, specified by design)	$t_{doff(ST)}$	--	1	--	$\mu\text{s}$
Status output (open drain)					
Zener limit voltage $T_j = -40\dots+150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :	$V_{ST(high)}$	5.4	6.1	6.9	V
ST low voltage $T_j = -40\dots+25^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :	$V_{ST(low)}$	--	--	0.4	
$T_j = +150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :		--	--	0.7	
Status leakage current, $V_{ST} = 5\text{ V}$ , $T_j = 25\dots+150^\circ\text{C}$ :	$I_{ST(high)}$	--	--	2	$\mu\text{A}$

<sup>20)</sup> If ground resistors  $R_{GND}$  are used, add the voltage drop across these resistors.

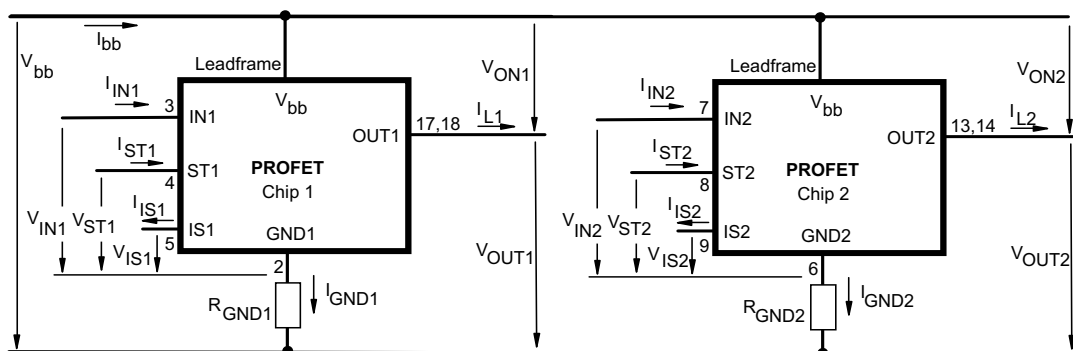
### Truth Table

	Input 1	Output 1	Status 1	Current Sense 1
	Input 2	Output 2	Status 2	Current Sense 2
	level	level	level	$I_{IS}$
Normal operation	L	L	H	0
	H	H	L	nominal
Current-limitation	L	L	H	0
	H	H	H	0
Short circuit to GND	L	L	H	0
	H	L <sup>21)</sup>	H	0
Over-temperature	L	L	H	0
	H	L	H	0
Short circuit to $V_{bb}$	L	H	L <sup>22)</sup>	0
	H	H	L	<nominal <sup>23)</sup>
Open load	L	L <sup>24)</sup>	H (L <sup>25)</sup> )	0
	H	H	L	0
Undervoltage	L	L	H	0
	H	L	L	0
Overvoltage	L	L	H	0
	H	L	L	0
Negative output voltage clamp	L	L	H	0

L = "Low" Level      X = don't care      Z = high impedance, potential depends on external circuit  
H = "High" Level      Status signal after the time delay shown in the diagrams (see fig 5. page 13)

Parallel switching of channel 1 and 2 is possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor. The current sense outputs IS1 and IS2 have to be connected with a single pull-down resistor.

### Terms



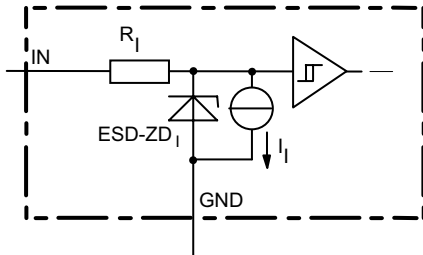
Leadframe ( $V_{bb}$ ) is connected to pin 1,10,11,12,15,16,19,20

External  $R_{GND}$  optional; two resistors  $R_{GND1}$ ,  $R_{GND2} = 150 \Omega$  or a single resistor  $R_{GND} = 75 \Omega$  for reverse battery protection up to the max. operating voltage.

- 21) The voltage drop over the power transistor is  $V_{bb} - V_{OUT} > 3V$  typ. Under this condition the sense current  $I_{IS}$  is zero
- 22) An external short of output to  $V_{bb}$ , in the off state, causes an internal current from output to ground. If  $R_{GND}$  is used, an offset voltage at the GND and ST pins will occur and the  $V_{ST\ low}$  signal may be erroneous.
- 23) Low ohmic short to  $V_{bb}$  may reduce the output current  $I_L$  and therefore also the sense current  $I_{IS}$ .
- 24) Power Transistor off. high impedance

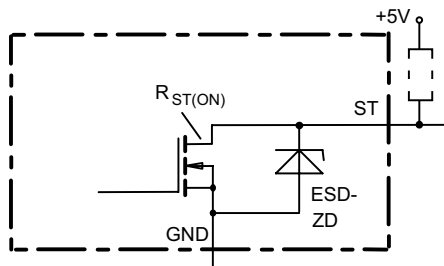


**Input circuit (ESD protection), IN1 or IN2**



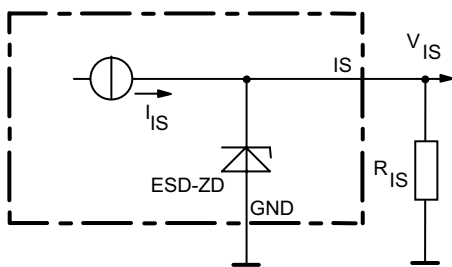
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

**Status output, ST1 or ST2**



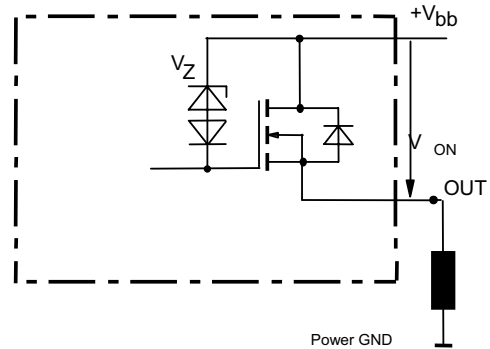
ESD-Zener diode: 6.1 V typ., max 5.0 mA;  $R_{ST(ON)} < 375 \Omega$  at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

**Current sense output**



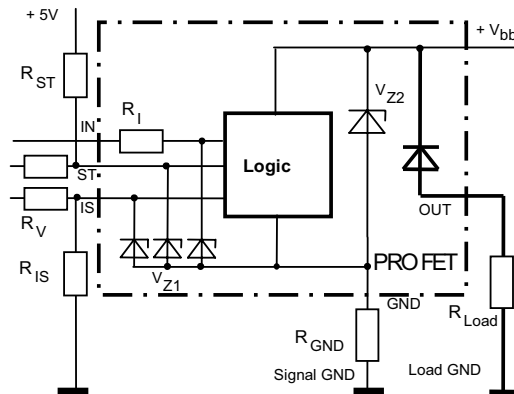
ESD-Zener diode: 6.1 V typ., max 14 mA;  $R_{IS} = 1 \text{ k}\Omega$  nominal

**Inductive and overvoltage output clamp, OUT1 or OUT2**



$V_{ON}$  clamped to  $V_{ON(CL)} = 47 \text{ V}$  typ.

**Overvoltage and reverse batt. protection**

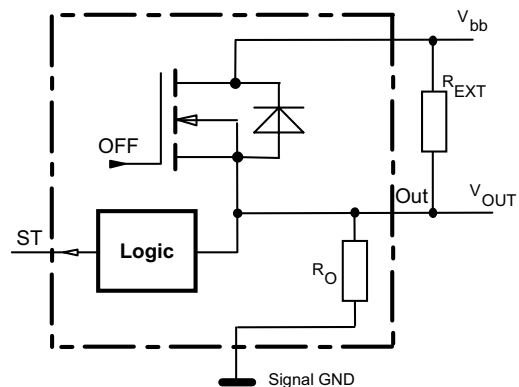


$V_{Z1} = 6.1 \text{ V}$  typ.,  $V_{Z2} = 47 \text{ V}$  typ.,  $R_{GND} = 150 \Omega$ ,  $R_{ST} = 15 \text{ k}\Omega$ ,  $R_I = 4.5 \text{ k}\Omega$  typ.,  $R_{IS} = 1 \text{ k}\Omega$ ,  $R_V = 15 \text{ k}\Omega$ . In case of reverse battery the current has to be limited by the load. Temperature protection is not active

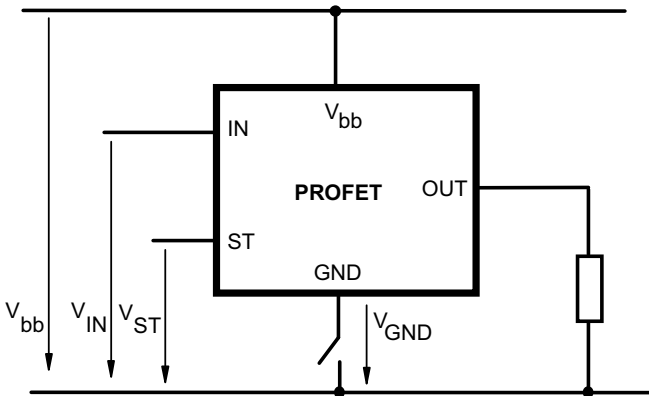
**Open-load detection OUT1 or OUT2**

OFF-state diagnostic condition:

$V_{OUT} > 3 \text{ V}$  typ.; IN low

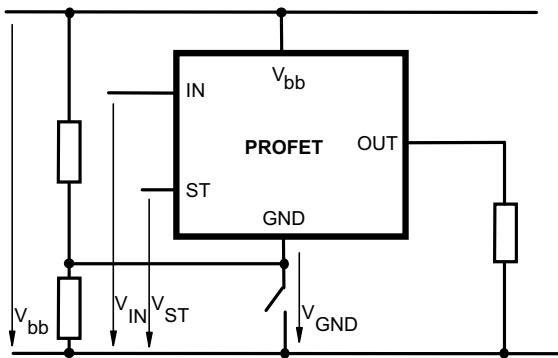


**GND disconnect**



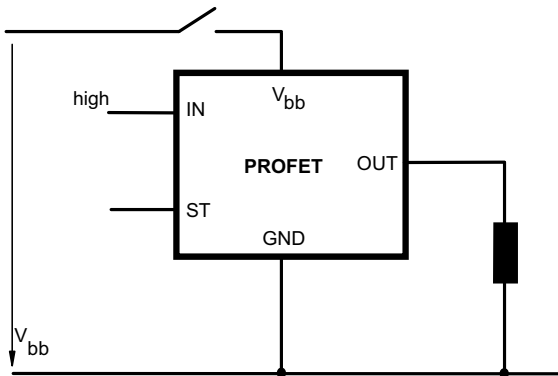
Any kind of load. In case of IN=high is  $V_{OUT} \approx V_{IN} - V_{IN(T+)}$ .  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low}$  signal available.

**GND disconnect with GND pull up**



Any kind of load. If  $V_{GND} > V_{IN} - V_{IN(T+)}$  device stays off  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low}$  signal available.

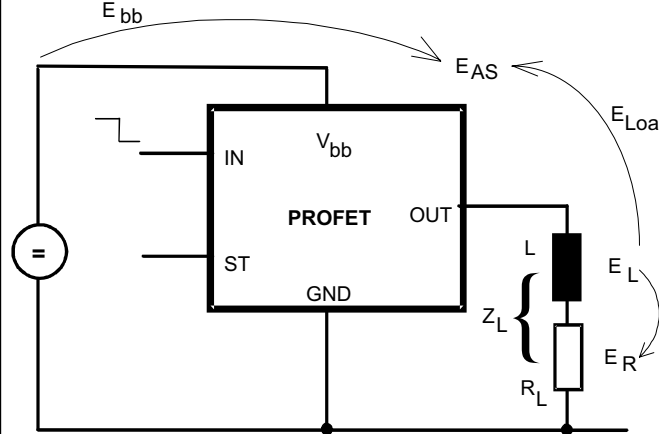
**Vbb disconnect with energized inductive load**



For inductive load currents up to the limits defined by  $Z_L$  (max. ratings and diagram on page 10) each switch is protected against loss of  $V_{bb}$ .

Consider at your PCB layout that in the case of  $V_{bb}$  disconnection with energized inductive load all the load current flows through the GND connection.

**Inductive load switch-off energy dissipation**



Energy stored in load inductance:

$$E_L = 1/2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

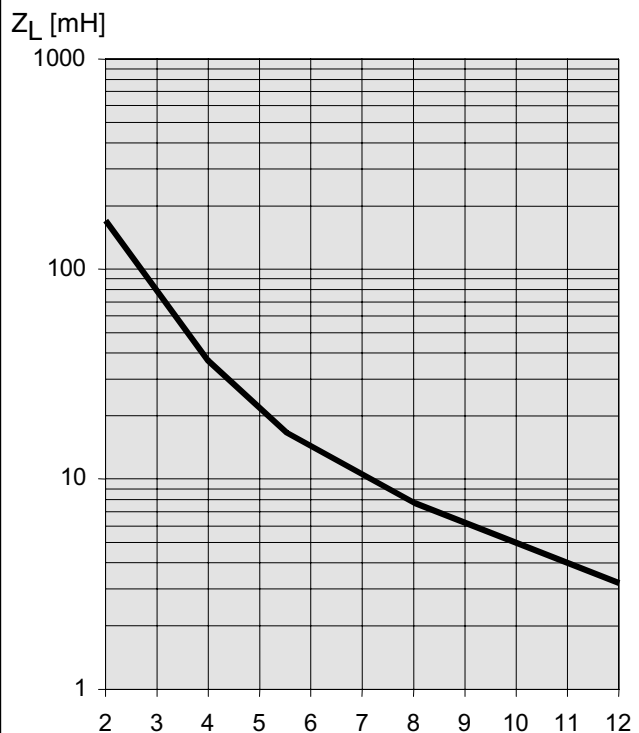
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for  $R_L > 0 \Omega$ :

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left( 1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

**Maximum allowable load inductance for a single switch off (one channel)<sup>4)</sup>**

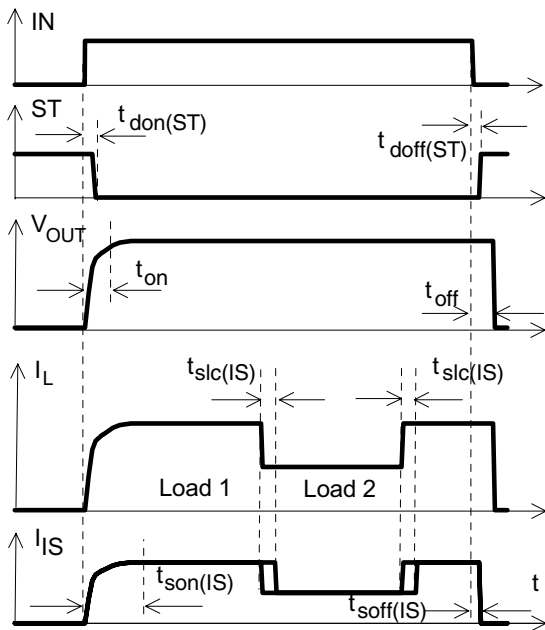
$L = f(I_L)$ ;  $T_{j,start} = 150^\circ\text{C}$ ,  $V_{bb} = 12\text{V}$ ,  $R_L = 0 \Omega$



## Timing diagrams

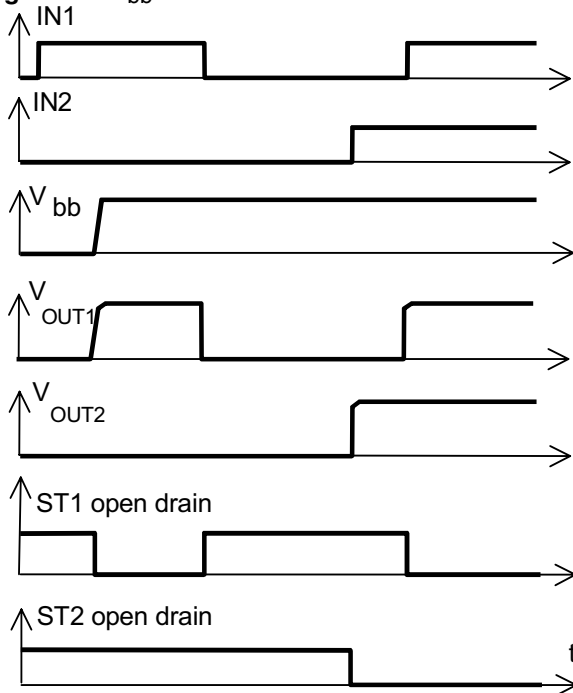
Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

**Figure 1a:** Switching a resistive load, change of load current in on-condition:



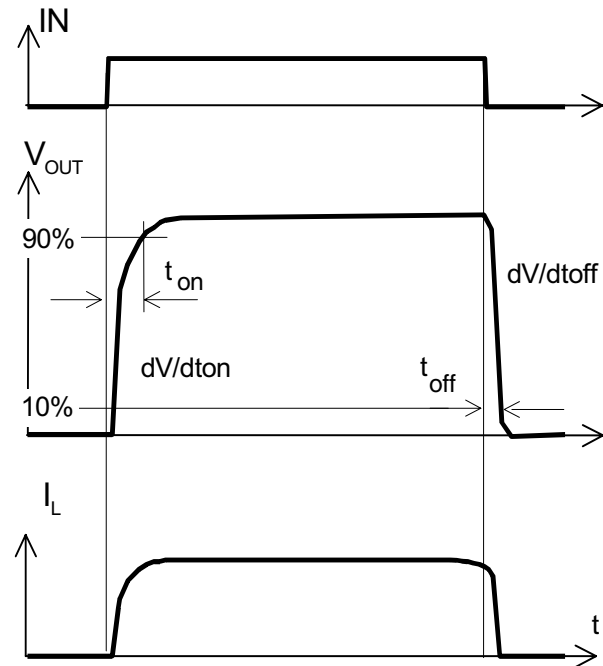
The sense signal is not valid during settling time after turn or change of load current.

**Figure 1b:**  $V_{bb}$  turn on:

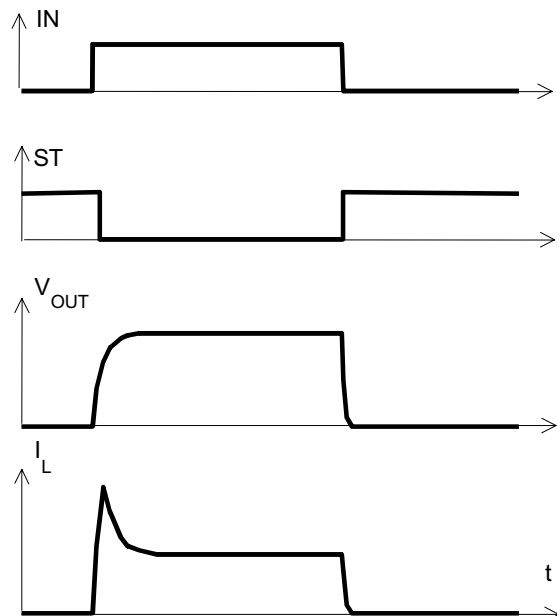


proper turn on under all conditions

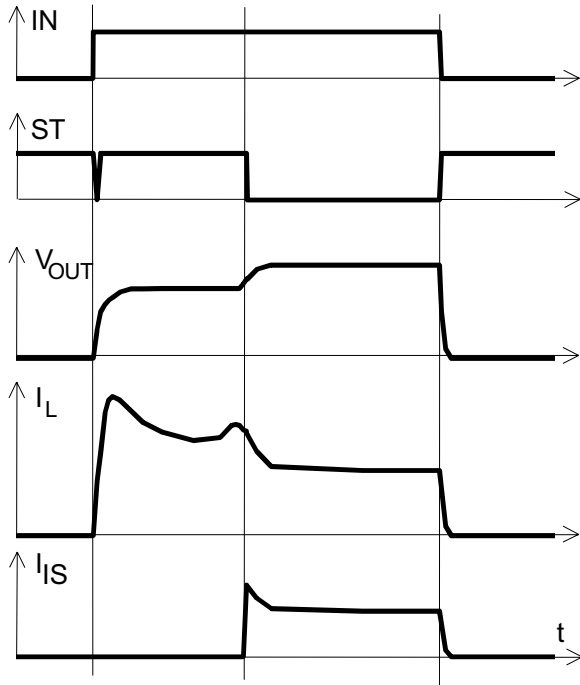
**Figure 2a:** Switching a resistive load, turn-on/off time and slew rate definition:



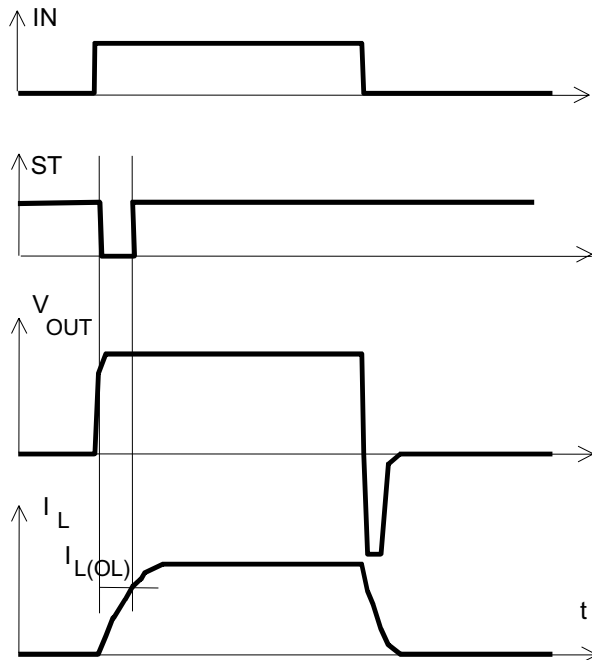
**Figure 2b:** Switching a lamp:



**Figure 2c:** Switching a lamp with current limit:

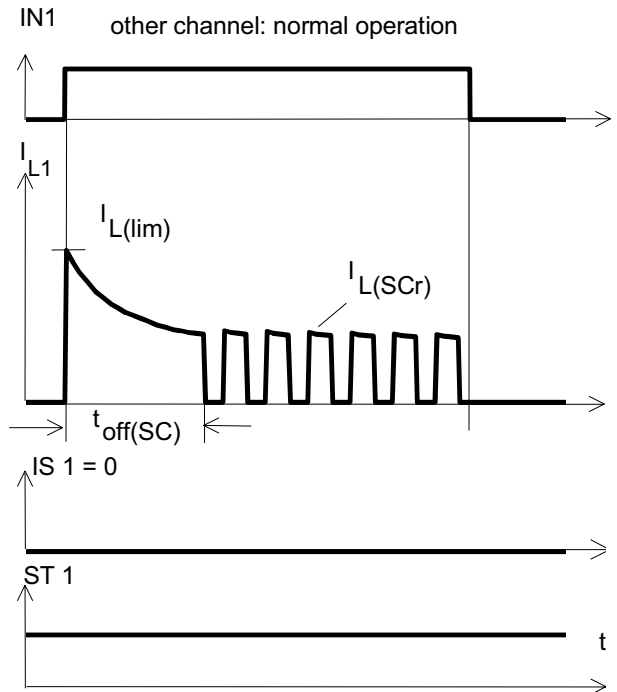


**Figure 2d:** Switching an inductive load



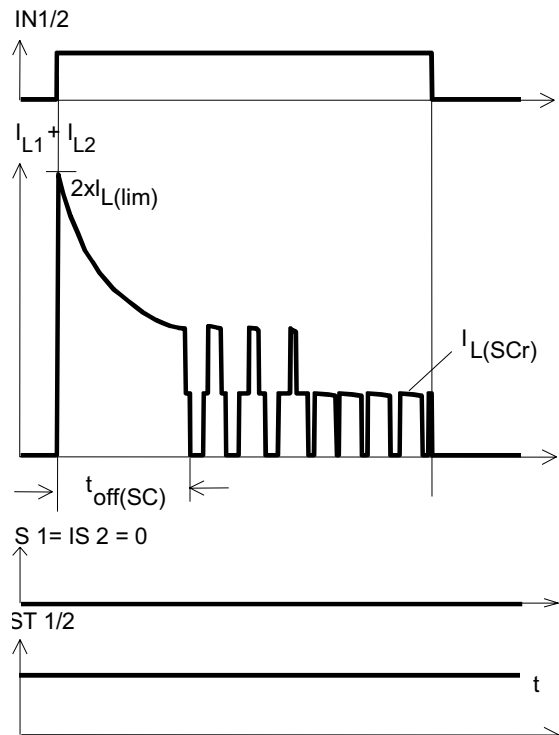
\*) if the time constant of load is too large, open-load-status may occur

**Figure 3a:** Turn on into short circuit: shut down by overtemperature, restart by cooling



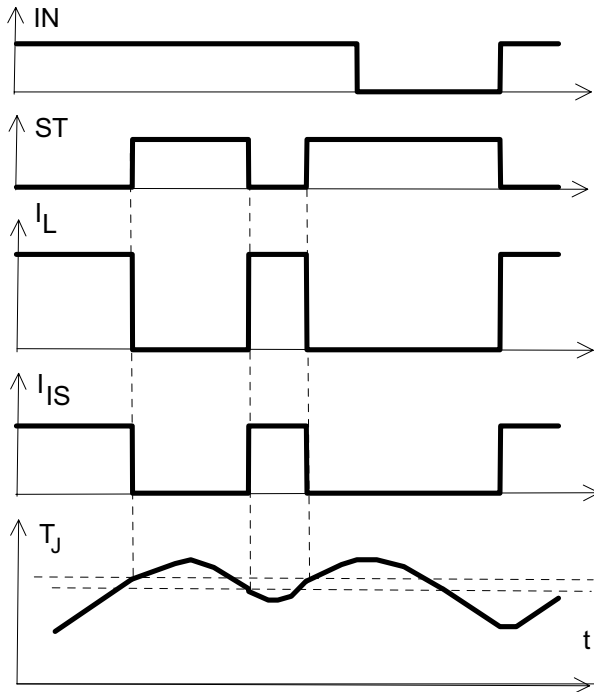
Heating up of the chip may require several milliseconds, depending on external conditions

**Figure 3b:** Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)

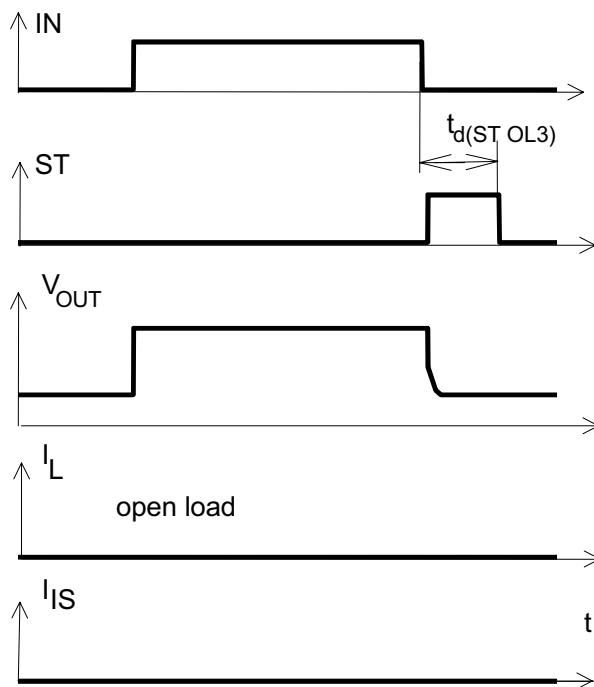


ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor

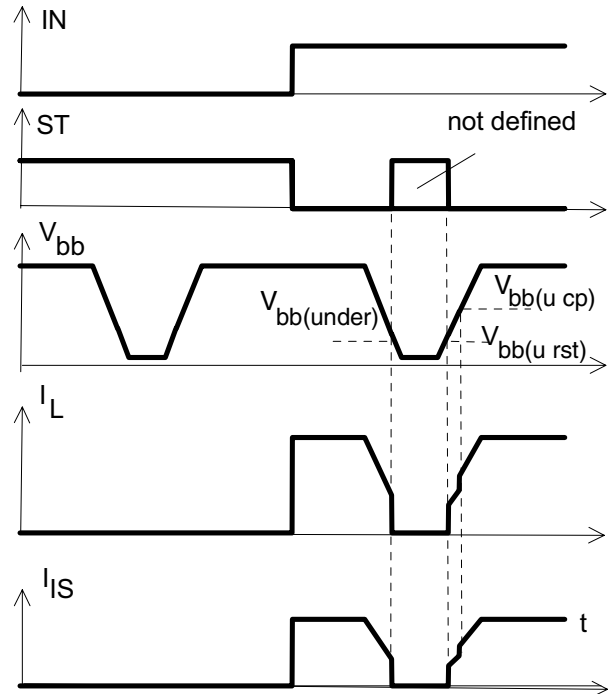
**Figure 4a: Overtemperature:**  
Reset if  $T_j < T_{jt}$



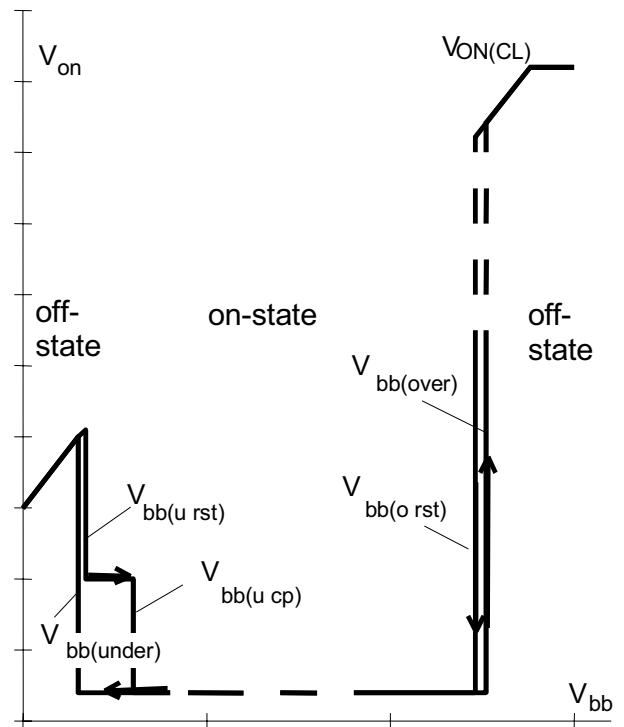
**Figure 5a: Open load: detection (with R<sub>EXT</sub>),**  
turn on/off to open load



**Figure 6a: Undervoltage:**



**Figure 6b: Undervoltage restart of charge pump**



charge pump starts at  $V_{bb(ucp)} = 4.7 \text{ V typ.}$

Figure 7a: Overvoltage:

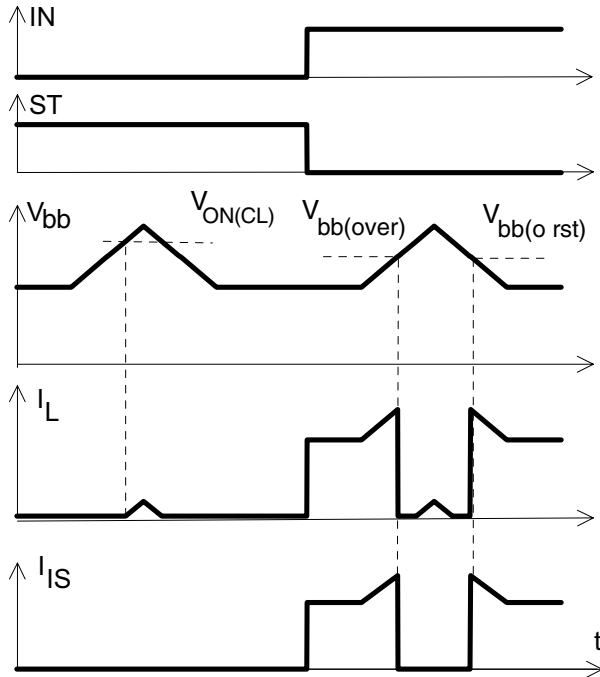


Figure 8b: Current sense ratio:

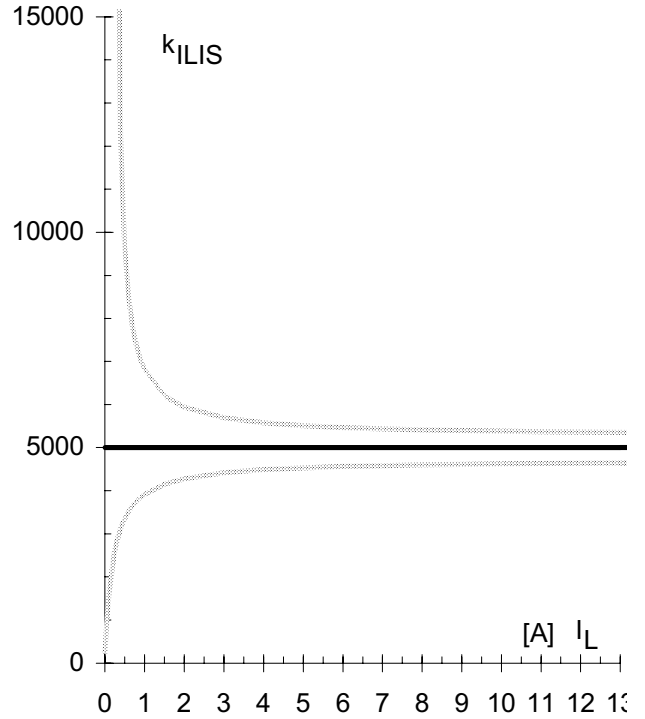


Figure 8a: Current sense versus load current<sup>26</sup>:

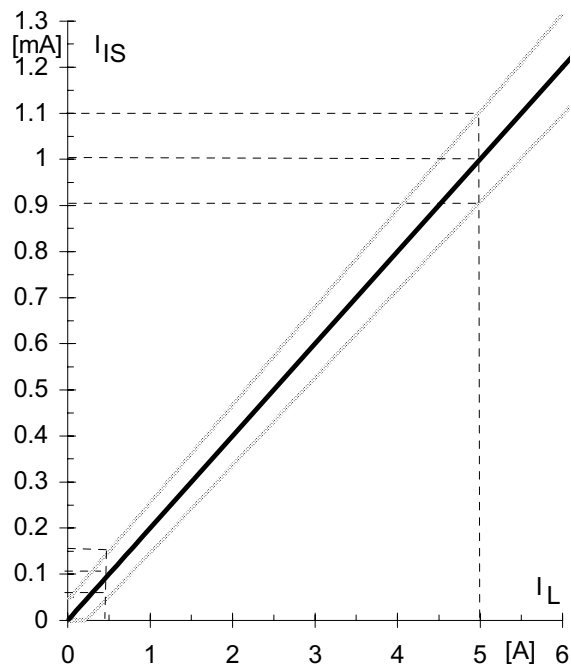
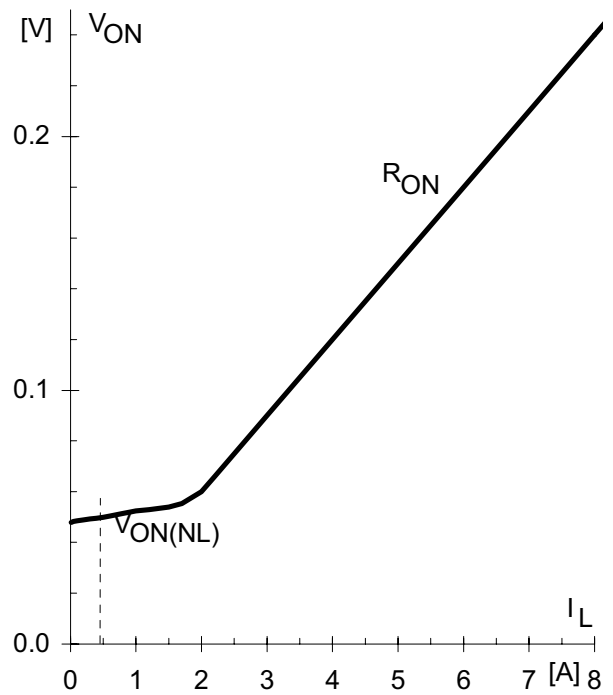


Figure 9a: Output voltage drop versus load current:



<sup>26</sup> This range for the current sense ratio refers to all devices. The accuracy of the  $k_{ILIS}$  can be raised at







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