

# EiceDRIVER™ 1ED020I12-B2 Enhanced

## Single channel isolated gate driver IC with DESAT, and Miller Clamp

### Features

- Single channel coreless transformer isolated gate driver IC
- For 600 V/1200 V IGBTs and SiC MOSFETs
- 2 A typical rail-to-rail output current
- Integrated protection features, e.g.
  - $V_{CEsat}$ -detection (DESAT)
  - Short circuit clamping
  - Active shut-down
  - Active Miller clamp
- 28 V absolute maximum output supply voltage
- 195/190 ns maximum propagation delay
- 100 kV/ $\mu$ s common mode transient immunity (CMTI)
- 12/11 V output undervoltage lockout (UVLO)
- Suitable for operation at high ambient temperature
- Certified according to UL 1577 with  $V_{ISO} = 3750$  V (rms) for 1 min
- Basic insulation tested

### Potential applications

- AC and brushless DC motor drives
- High voltage DC/DC-converter
- UPS-systems
- Solar inverter
- EV charging
- Commercial, construction and agricultural vehicles (CAV)
- Commercial air conditioner (CAC)
- Industrial power supply



PG-DSO-16-15

### Product validation

Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC20/22.

### Device information

Product type	Typical output current	Certification(File E311313)	Package	Evaluation board
<a href="#">1ED020I12-B2</a>	$\pm 2$ A	UL 1577	PG-DSO-16-15	<a href="#">EVAL-1ED020I12-B2</a>

**Table 1** Similar products

Product type	Typical output current	Certification(File E311313)	Package	Evaluation board
<a href="#">1ED020I12-F2</a>	$\pm 2$ A	–	PG-DSO-16-15	<a href="#">2ED100E12-F2</a>

**Description**

**Table 1 Similar products (continued)**

Product type	Typical output current	Certification(File E311313)	Package	Evaluation board
<a href="#">1ED020I12-BT</a>	± 2 A	UL 1577	PG-DSO-16-15	<a href="#">EVAL-1ED020I12-BT</a>
<a href="#">1ED020I12-FT</a>	± 2 A	–	PG-DSO-16-15	–
<a href="#">2ED020I12-F2</a>	± 2 A	–	PG-DSO-36-58	<a href="#">EVAL-2ED020I12-F2</a>

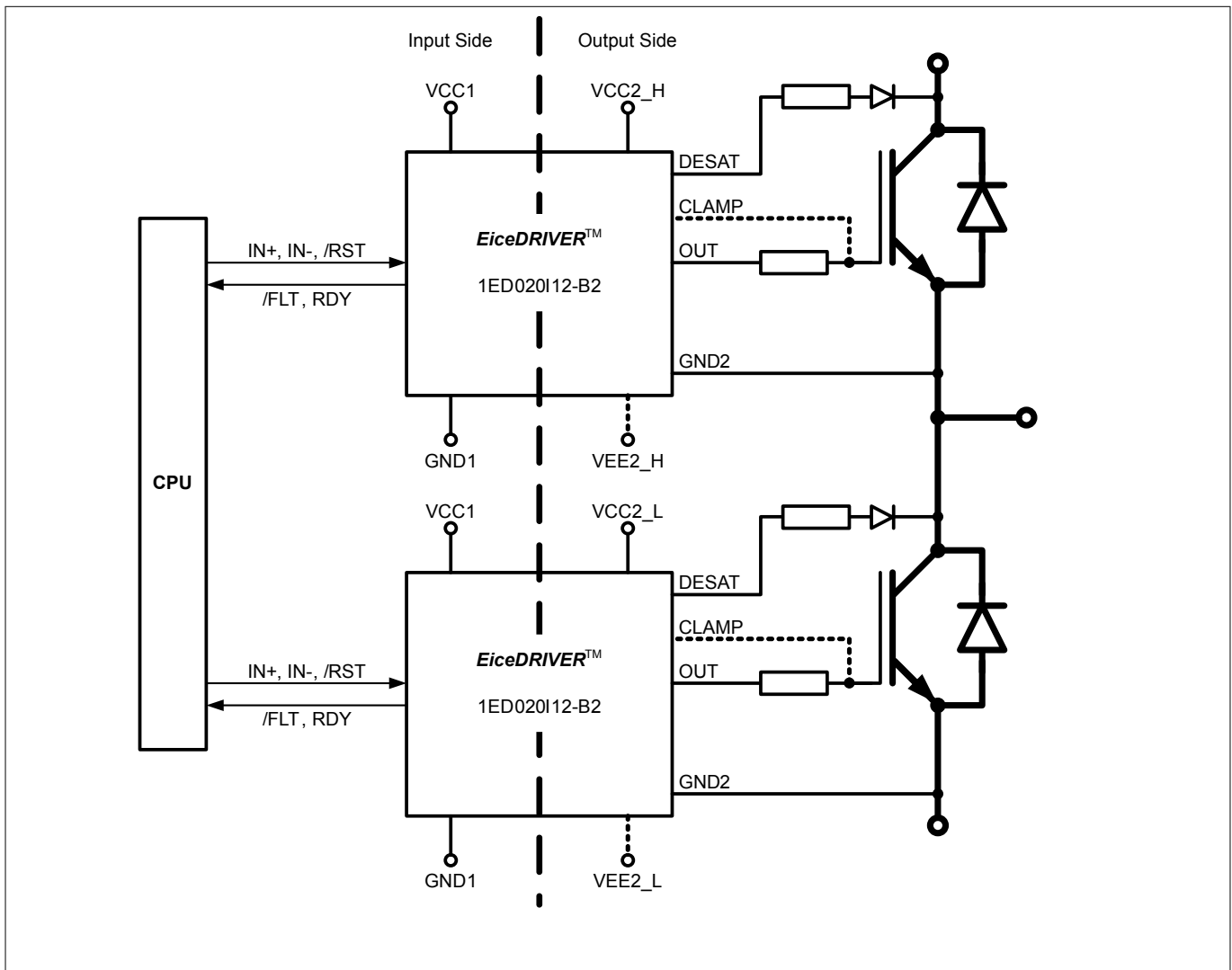
**Description**

The 1ED020I12-B2 is a galvanic isolated single channel driver in a PG-DSO-16-15 300 mil wide body package that provides an output current capability of typically 2 A.

All logic pins are 5 V CMOS compatible and could be directly connected to a microcontroller.

The data transfer across galvanic isolation is realized by the integrated coreless transformer technology.

The 1ED020I12-B2 provides several protection features like IGBT desaturation protection, active Miller clamping and active shut down.



**Figure 1 Typical application**

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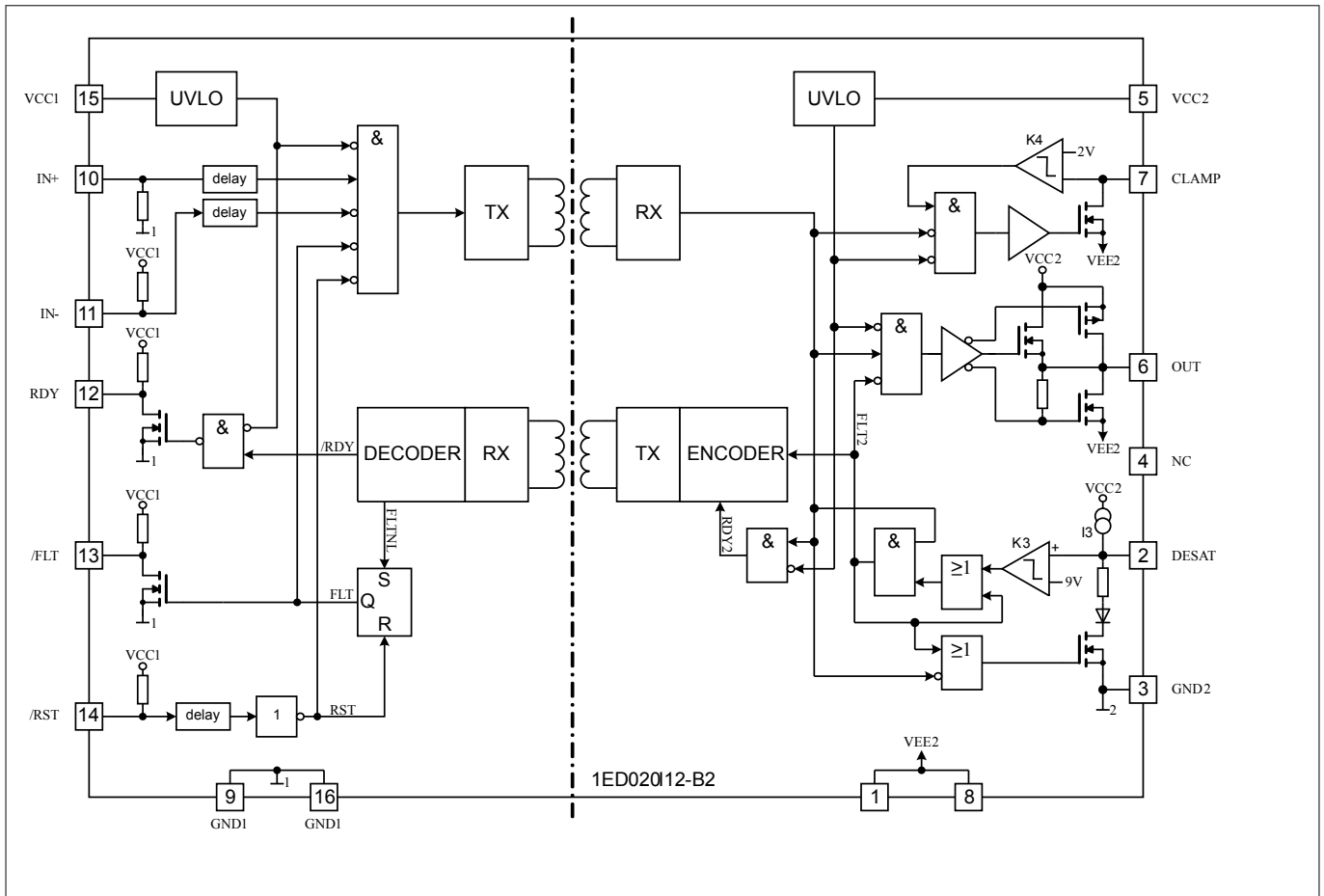
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**1 Block diagram**

**1 Block diagram**



**Figure 2** Block diagram 1ED020I12-B2

**2 Pin configuration and functionality**

**2.1 Pin configuration**

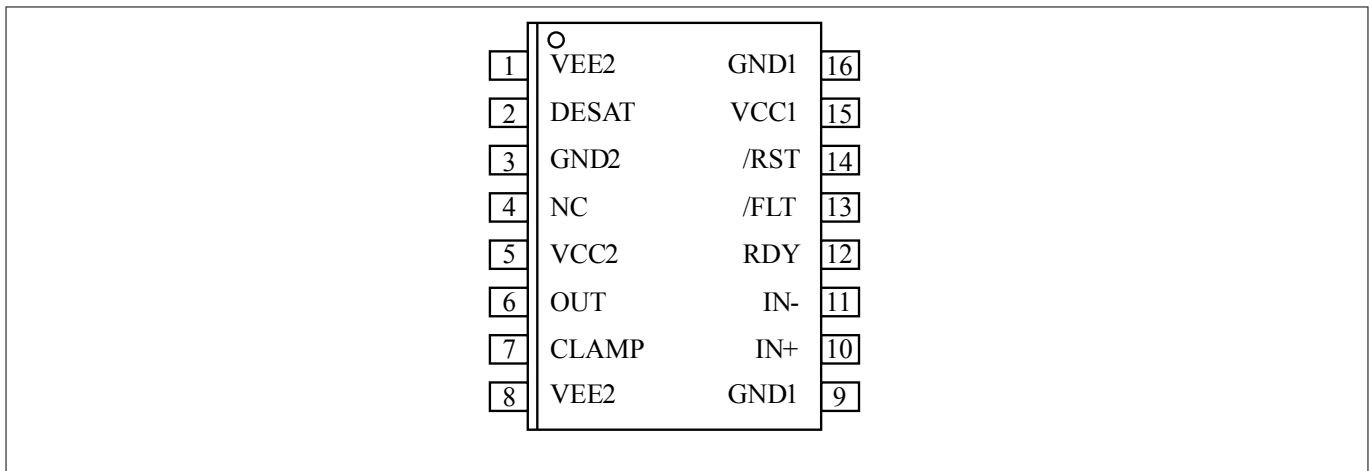
**Table 2** Pin configuration

Pin No.	Name	Function
1	VEE2	Negative power supply output side
2	DESAT	Desaturation protection
3	GND2	Signal ground output side
4	NC	Not connected
5	VCC2	Positive power supply output side
6	OUT	Driver output
7	CLAMP	Miller clamping
8	VEE2	Negative power supply output side
9	GND1	Ground input side

**2 Pin configuration and functionality**

**Table 2 Pin configuration (continued)**

Pin No.	Name	Function
10	<i>IN+</i>	Non inverted driver input
11	<i>IN-</i>	Inverted driver input
12	<i>RDY</i>	Ready output
13	<i>/FLT</i>	Fault output, low active
14	<i>/RST</i>	Reset input, low active
15	<i>VCC1</i>	Positive power supply input side
16	<i>GND1</i>	Ground input side



**Figure 3 1ED020I12-B2 (top view)**

**2.2 Pin functionality**

***GND1***

Ground connection of the input side.

***IN+* non-inverting gate driver input**

*IN+* control signal for the driver output if *IN-* is set to low. (The IGBT is on if *IN+* = high and *IN-* = low)

A minimum pulse width is defined to make the IC robust against glitches at *IN+*. An internal pull-down resistor ensures IGBT off-state.

***IN-* inverting gate driver input**

*IN-* control signal for driver output if *IN+* is set to high. (IGBT is on if *IN-* = low and *IN+* = high)

A minimum pulse width is defined to make the IC robust against glitches at *IN-*. An internal pull-up resistor ensures IGBT off-state.

***/RST* reset input**

Function 1: Enable/shutdown of the input chip. (The IGBT is off if */RST* = low). A minimum pulse width is defined to make the IC robust against glitches at */RST*.

Function 2: Resets the DESAT fault-state of the chip if */RST* is low for a time  $t_{RST}$ . An internal pull-up resistor is used to ensure */FLT* status output.

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### 3 Functional description

#### **/FLT fault output**

Open-drain output to report a desaturation error of the IGBT (/FLT is low if desaturation occurs)

#### **RDY ready status**

Open-drain output to report the correct operation of the device (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless).

#### **VCC1**

5 V power supply of the input chip

#### **VEE2**

Negative power supply pins of the output chip. If no negative supply voltage is available, all VEE2 pins have to be connected to GND2.

#### **DESAT desaturation detection input**

Monitoring of the IGBT saturation voltage ( $V_{CE}$ ) to detect desaturation caused by short circuits. If OUT is high,  $V_{CE}$  is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

#### **CLAMP Miller clamping**

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2 V (related to VEE2). The clamp is designed for a Miller current up to 2 A.

#### **GND2 reference ground**

Reference ground of the output chip.

#### **OUT driver output**

Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode  $V_{OUT}$  is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT)  $V_{OUT}$  is set to VEE2 independent of the input control signals.

#### **VCC2**

Positive power supply pin of the output side.

## 3 Functional description

The 1ED020I12-B2 is an advanced IGBT gate driver that can be also used for driving power MOS devices. Control and protection functions are included to enable the design of high reliability systems.

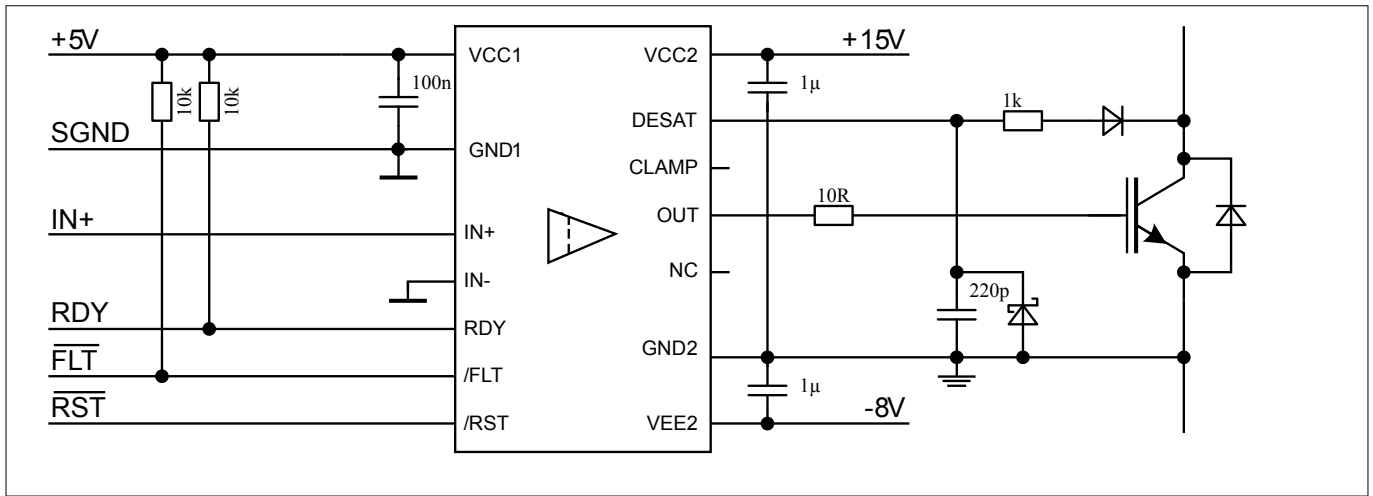
The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5 V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

The rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation on a system-level.

The device also includes IGBT desaturation protection with /FLT status output.

The RDY status output reports if the device is supplied and operates correctly.

**3 Functional description**



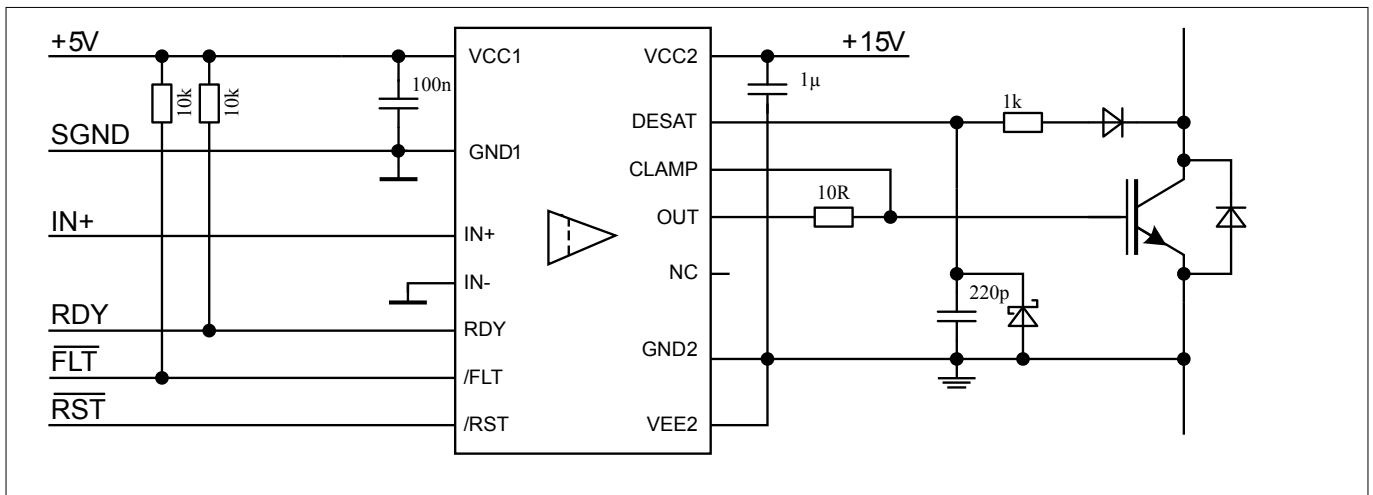
**Figure 4 Application example bipolar supply**

**3.1 Supply**

The driver 1ED020I12-B2 is designed to support two different supply configurations, bipolar supply and unipolar supply.

In bipolar supply the driver is typically supplied with a positive voltage of 15 V at VCC2 and a negative voltage of -8 V at VEE2. Negative supply prevents a dynamic turn on due to the additional charge which is generated from IGBT input capacitance times negative supply voltage. If an appropriate negative supply voltage is used, connecting CLAMP to IGBT gate is redundant and therefore typically not necessary.

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15 V at VCC2. Erratically dynamic turn on of the IGBT could be prevented with active Miller clamp function, so CLAMP output is directly connected to IGBT gate.



**Figure 5 Application example unipolar supply**

**3.2 Internal protection features**

**3.2.1 Undervoltage lockout (UVLO)**

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips, refer to [Figure 9](#).



### 3 Functional description

If the power supply voltage  $V_{VCC1}$  of the input chip drops below  $V_{UVLOL1}$  a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at  $IN+$  and  $IN-$  are ignored as long as  $V_{VCC1}$  reaches the power-up voltage  $V_{UVLOH1}$ .

If the power supply voltage  $V_{VCC2}$  of the output chip goes down below  $V_{UVLOL2}$  the IGBT is switched off and signals from the input chip are ignored as long as  $V_{VCC2}$  reaches the power-up voltage  $V_{UVLOH2}$ .  $VEE2$  is not monitored, otherwise negative supply voltage range from 0 V to -12 V would not be possible.

#### 3.2.2 RDY ready status output

The *RDY* output shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission after a short delay

It is not necessary to reset the *RDY* signal since its state only depends on the status of the former mentioned protection signals.

#### 3.2.3 Watchdog timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the *RDY* ready output reports an internal error.

#### 3.2.4 Active shut-down

The active shut-down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply, IGBT gate is clamped at *OUT* to  $VEE2$ .

### 3.3 Non-inverting and inverting inputs

There are two possible input modes to control the IGBT. At non-inverting mode  $IN+$  controls the driver output while  $IN-$  is set to low. At inverting mode  $IN-$  controls the driver output while  $IN+$  is set to high, please see [Figure 7](#). A minimum input pulse width is defined to filter occasional glitches.

### 3.4 Driver output

The output driver sections uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable.

Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

### 3.5 External protection features

#### 3.5.1 Desaturation protection

A desaturation protection ensures the protection of the IGBT at short circuit.

When the DESAT voltage goes up and reaches 9 V, the output is driven low. Further, the */FLT* output is activated after DESAT to fault-off delay, please refer to [Figure 8](#). An off command at  $IN$  during DESAT to fault-off delay is erasing the fault status. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

## 4 Electrical parameters

### 3.5.2 Active Miller clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high  $dV/dt$  situation. Therefore in many applications, the use of a negative supply voltage can be avoided. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below typical 2 V (related to  $V_{EE2}$ ). The clamp is designed for a Miller current up to 2 A.

### 3.5.3 Short circuit clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to  $OUT$  and  $CLAMP$  limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10  $\mu s$  may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

### 3.6 /RST reset

The reset input has two functions.

- /RST is in charge of setting back the /FLT output. If /RST is low longer than a given time, /FLT will be cleared at the rising edge of /RST, refer to [Figure 8](#); otherwise, it will remain unchanged
- /RST works as enable/shutdown of the input logic, refer to [Figure 7](#)

## 4 Electrical parameters

### 4.1 Absolute maximum ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.*

**Table 3 Absolute maximum ratings**

Parameter	Symbol	Values		Unit	Note / Test condition
		Min.	Max.		
Positive power supply output side	$V_{VCC2}$	-0.3	20	V	<sup>1)</sup>
Negative power supply output side	$V_{VEE2}$	-12	0.3	V	<sup>1)</sup>
Maximum power supply voltage output side ( $V_{VCC2} - V_{VEE2}$ )	$V_{max2}$	-	28	V	-
Gate driver output	$V_{OUT}$	$V_{VEE2}-0.3$	$V_{VCC2}+0.3$	V	-
Gate driver high output maximum current	$I_{OUT}$	-	2.4	A	$t = 2 \mu s$
Gate & clamp driver low output maximum current	$I_{OUT}$	-	2.4	A	$t = 2 \mu s$
Maximum short circuit clamping time	$t_{CLP}$	-	10	$\mu s$	$I_{CLAMP/OUT} = 500 \text{ mA}$
Positive power supply input side	$V_{VCC1}$	-0.3	6.5	V	-

<sup>1</sup> With respect to GND2.

## 4 Electrical parameters

**Table 3 Absolute maximum ratings (continued)**

Parameter	Symbol	Values		Unit	Note / Test condition
		Min.	Max.		
Logic input voltages ( $IN+$ , $IN-$ , $RST$ )	$V_{LogicIN}$	-0.3	6.5	V	–
Opendrain Logic output voltage ( $/FLT$ )	$V_{/FLT}$	-0.3	6.5	V	–
Opendrain Logic output voltage ( $RDY$ )	$V_{RDY}$	-0.3	6.5	V	–
Opendrain Logic output current ( $/FLT$ )	$I_{/FLT}$	–	10	mA	–
Opendrain Logic output current ( $RDY$ )	$I_{RDY}$	–	10	mA	–
Pin $DESAT$ voltage	$V_{DESAT}$	-0.3	$V_{VCC2} + 0.3$	V	<sup>1)</sup>
Pin $CLAMP$ voltage	$V_{CLAMP}$	-0.3	$V_{VCC2} + 0.3$ <sup>2)</sup>	V	<sup>3)</sup>
Input to output isolation voltage ( $GND2$ )	$V_{offset}$	-1200	1200	V	
Junction temperature	$T_J$	-40	150	°C	–
Storage temperature	$T_S$	-55	150	°C	–
Power dissipation, per input part	$P_{D, IN}$	–	100	mW	<sup>4)</sup> @ $T_A = 25^\circ\text{C}$
Power dissipation, at output side	$P_{D, OUT}$	–	700	mW	<sup>4)</sup> @ $T_A = 25^\circ\text{C}$
Thermal resistance (input side)	$R_{thJA, IN}$	–	160	K/W	<sup>4)</sup> @ $T_A = 25^\circ\text{C}$
Thermal resistance (output side)	$R_{thJA, OUT}$	–	125	K/W	<sup>4)</sup> @ $T_A = 25^\circ\text{C}$
ESD capability	$V_{ESD, HBM}$	–	1	kV	Human Body Model <sup>5)</sup>

## 4.2 Operating parameters

*Note:* Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to  $GND1$ .

**Table 4 Operating parameters**

Parameter	Symbol	Values		Unit	Note / Test condition
		Min.	Max.		
Positive power supply output side	$V_{VCC2}$	13	20	V	<sup>6)</sup>
Negative power supply output side	$V_{VEE2}$	-12	0	V	<sup>6)</sup>

<sup>1)</sup> With respect to  $GND2$ .

<sup>2)</sup> May be exceeded during short circuit clamping.

<sup>3)</sup> With respect to  $VEE2$ .

<sup>4)</sup> Output IC power dissipation is derated linearly at 10 mW/°C above 62°C. Input IC power dissipation does not require derating. See **Figure 11** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

<sup>5)</sup> According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

<sup>6)</sup> With respect to  $GND2$ .

## 4 Electrical parameters

**Table 4 Operating parameters (continued)**

Parameter	Symbol	Values		Unit	Note / Test condition
		Min.	Max.		
Maximum power supply voltage output side ( $V_{VCC2} - V_{VEE2}$ )	$V_{max2}$	–	28	V	–
Positive power supply input side	$V_{VCC1}$	4.5	5.5	V	–
Logic input voltages ( $IN+$ , $IN-$ , $RST$ )	$V_{LogicIN}$	-0.3	5.5	V	–
Pin <i>CLAMP</i> voltage	$V_{CLAMP}$	$V_{VEE2}-0.3$	$V_{VCC2}$ <sup>7)</sup>	V	–
Pin <i>DESAT</i> voltage	$V_{DESAT}$	-0.3	$V_{VCC2}$	V	<sup>6)</sup>
Ambient temperature	$T_A$	-40	105	°C	–
Common mode transient immunity <sup>8)</sup>	$ dV_{ISO}/dt $	–	100	kV/μs	@ 1200 V

### 4.3 Recommended operating parameters

Note: Unless otherwise noted all parameters refer to *GND1*.

**Table 5 Recommended operating parameters**

Parameter	Symbol	Value	Unit	Note / Test condition
Positive power supply output side	$V_{VCC2}$	15	V	<sup>9)</sup>
Negative power supply output side	$V_{VEE2}$	-8	V	<sup>9)</sup>
Positive power supply input side	$V_{VCC1}$	5	V	–

<sup>7</sup> May be exceeded during short circuit clamping.

<sup>6</sup> With respect to *GND2*.

<sup>8</sup> The parameter is not subject to production test - verified by design/characterization

<sup>9</sup> With respect to *GND2*.

## 4 Electrical parameters

### 4.4 Electrical characteristics

*Note:* The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at  $T_A = 25^\circ\text{C}$ . Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 9 to 16, GND2 for pins 1 to 8).

#### 4.4.1 Voltage supply

**Table 6** Voltage supply

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
UVLO threshold input chip	$V_{UVLOH1}$	–	4.1	4.3	V	–
	$V_{UVLOL1}$	3.5	3.8	–	V	–
UVLO hysteresis input chip ( $V_{UVLOH1} - V_{UVLOL1}$ )	$V_{HYS1}$	0.15	–	–	V	–
UVLO threshold output chip	$V_{UVLOH2}$	–	12.0	12.6	V	–
	$V_{UVLOL2}$	10.4	11.0	–	V	–
UVLO hysteresis output chip ( $V_{UVLOH2} - V_{UVLOL2}$ )	$V_{HYS2}$	0.7	0.9	–	V	–
Quiescent current input chip	$I_{Q1}$	–	7	9	mA	$V_{CC1} = 5\text{ V}$ $IN+ = \text{High}$ , $IN- = \text{Low}$ $\Rightarrow OUT = \text{High}$ , $RDY = \text{High}$ , $/FLT = \text{High}$
Quiescent current output chip	$I_{Q2}$	–	4	6	mA	$V_{CC2} = 15\text{ V}$ $V_{VEE2} = -8\text{ V}$ $IN+ = \text{High}$ , $IN- = \text{Low}$ $\Rightarrow OUT = \text{High}$ , $RDY = \text{High}$ , $/FLT = \text{High}$

## 4 Electrical parameters

### 4.4.2 Logic input and output

**Table 7** Logic input and output

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
<i>IN+</i> , <i>IN-</i> , <i>/RST</i> low input voltage	$V_{IN+,L}$ , $V_{IN-,L}$ , $V_{/RST,L}$	–	–	1.5	V	–
<i>IN+</i> , <i>IN-</i> , <i>/RST</i> high input voltage	$V_{IN+,H}$ , $V_{IN-,H}$ , $V_{/RST,H}$	3.5	–	–	V	–
<i>IN-</i> , <i>/RST</i> input current	$I_{IN-}$ , $I_{/RST}$	-400	-100	–	μA	$V_{IN-} = GND1$ $V_{/RST} = GND1$
<i>IN+</i> input current	$I_{IN+}$	–	100	400	μA	$V_{IN+} = VCC1$
<i>RDY</i> , <i>/FLT</i> pull-up current	$I_{P,RDY}$ , $I_{P,/FLT}$	-400	-100	–	μA	$V_{RDY} = GND1$ $V_{/FLT} = GND1$
Input pulse suppression <i>IN+</i> , <i>IN-</i>	$t_{MININ+}$ , $t_{MININ-}$	30	40	–	ns	–
Input pulse suppression <i>/RST</i> for enable/shutdown	$t_{MINRST}$	30	40	–	ns	–
Pulse width <i>/RST</i> for resetting <i>/FLT</i>	$t_{/RST}$	800	–	–	ns	–
<i>/FLT</i> low voltage	$V_{/FLT,L}$	–	–	300	mV	$I_{SINK,/FLT} = 5 \text{ mA}$
<i>RDY</i> low voltage	$V_{RDY,L}$	–	–	300	mV	$I_{SINK,RDY} = 5 \text{ mA}$

## 4 Electrical parameters

### 4.4.3 Gate driver

**Table 8 Gate driver**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
High level output voltage	$V_{\text{OUTH1}}$	$V_{\text{CC2}} - 1.2$	$V_{\text{CC2}} - 0.8$	–	V	$I_{\text{OUTH}} = -20 \text{ mA}$
	$V_{\text{OUTH2}}$	$V_{\text{CC2}} - 2.5$	$V_{\text{CC2}} - 2.0$	–	V	$I_{\text{OUTH}} = -200 \text{ mA}$
	$V_{\text{OUTH3}}$	$V_{\text{CC2}} - 9$	$V_{\text{CC2}} - 5$	–	V	$I_{\text{OUTH}} = -1 \text{ A}$
	$V_{\text{OUTH4}}$		$V_{\text{CC2}} - 10$	–	V	$I_{\text{OUTH}} = -2 \text{ A}$
High level output peak current	$I_{\text{OUTH}}$	-1.5	-2.0	–	A	$I_{\text{N+}} = \text{High}$ , $I_{\text{N-}} = \text{Low}$ ; $\text{OUT} = \text{High}$
Low level output voltage	$V_{\text{OUTL1}}$	–	$V_{\text{VEE2}} + 0.04$	$V_{\text{VEE2}} + 0.09$	V	$I_{\text{OUTL}} = 20 \text{ mA}$
	$V_{\text{OUTL2}}$	–	$V_{\text{VEE2}} + 0.3$	$V_{\text{VEE2}} + 0.85$	V	$I_{\text{OUTL}} = 200 \text{ mA}$
	$V_{\text{OUTL3}}$	–	$V_{\text{VEE2}} + 2.1$	$V_{\text{VEE2}} + 5$	V	$I_{\text{OUTL}} = 1 \text{ A}$
	$V_{\text{OUTL4}}$	–	$V_{\text{VEE2}} + 7$	–	V	$I_{\text{OUTL}} = 2 \text{ A}$
Low level output peak current	$I_{\text{OUTL}}$	1.5	2.0	–	A	$I_{\text{N+}} = \text{Low}$ , $I_{\text{N-}} = \text{Low}$ ; $\text{OUT} = \text{Low}$ , $V_{\text{CC2}} = 15 \text{ V}$ , $V_{\text{VEE2}} = -8 \text{ V}$

### 4.4.4 Active Miller clamp

**Table 9 Active Miller clamp**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Low level clamp voltage	$V_{\text{CLAMPL1}}$	–	$V_{\text{VEE2}} + 0.03$	$V_{\text{VEE2}} + 0.08$	V	$I_{\text{OUTL}} = 20 \text{ mA}$
	$V_{\text{CLAMPL2}}$	–	$V_{\text{VEE2}} + 0.3$	$V_{\text{VEE2}} + 0.8$	V	$I_{\text{OUTL}} = 200 \text{ mA}$
	$V_{\text{CLAMPL3}}$	–	$V_{\text{VEE2}} + 1.9$	$V_{\text{VEE2}} + 4.8$	V	$I_{\text{OUTL}} = 1 \text{ A}$
Low level clamp current	$I_{\text{CLAMPL}}$	2	–	–	A	<sup>10)</sup>
Clamp threshold voltage	$V_{\text{CLAMP}}$	1.6	2.1	2.4	V	Related to $V_{\text{EE2}}$

<sup>10)</sup> The parameter is not subject to production test - verified by design/characterization

## 4 Electrical parameters

### 4.4.5 Short circuit clamping

**Table 10** Short circuit clamping

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Clamping voltage (OUT) ( $V_{OUT} - V_{VCC2}$ )	$V_{CLPout}$	-	0.8	1.3	V	$IN+$ = High, $IN-$ = Low, $OUT$ = High $I_{OUT}$ = 500 mA pulse test, $t_{CLPmax}$ = 10 $\mu$ s)
Clamping voltage (CLAMP) ( $V_{VCLAMP} - V_{VCC2}$ )	$V_{CLPclamp}$	-	1.3	-	V	$IN+$ = High, $IN-$ = Low, $OUT$ = High $I_{CLAMP}$ = 500 mA (pulse test, $t_{CLPmax}$ = 10 $\mu$ s)
Clamping voltage (CLAMP)	$V_{CLPclamp}$	-	0.7	1.1	V	$IN+$ = High, $IN-$ = Low, $OUT$ = High $I_{CLAMP}$ = 20 mA

### 4.4.6 Dynamic characteristics

Dynamic characteristics are measured with  $V_{VCC1}$  = 5 V,  $V_{VCC2}$  = 15 V and  $V_{VEE2}$  = -8 V.

**Table 11** Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input $IN+$ , $IN-$ to output propagation delay ON	$t_{PDON}$	145	170	195	ns	$C_{LOAD}$ = 100 pF $V_{IN+}$ = 50%, $V_{OUT}$ = 50% @ 25°C
Input $IN+$ , $IN-$ to output propagation delay OFF	$t_{PD OFF}$	145	165	190	ns	
Input $IN+$ , $IN-$ to output propagation delay distortion ( $t_{PD OFF} - t_{PD ON}$ )	$t_{PDISTO}$	-35	-5	25	ns	
$IN+$ , $IN-$ input to output propagation delay ON variation due to temp	$t_{PD ON,t}$	-	-	25	ns	<sup>11)</sup> $C_{LOAD}$ = 100 pF $V_{IN+}$ = 50%, $V_{OUT}$ = 50%

<sup>11</sup> The parameter is not subject to production test - verified by design/characterization



#### 4 Electrical parameters

**Table 11** Dynamic characteristics (continued)

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
$I_{N+}$ , $I_{N-}$ input to output propagation delay OFF variation due to temp	$t_{P\text{DOFF},t}$	-	-	40	ns	<sup>11)</sup> $C_{\text{LOAD}} = 100 \text{ pF}$ $V_{\text{IN}+} = 50\%$ , $V_{\text{OUT}} = 50\%$
$I_{N+}$ , $I_{N-}$ input to output propagation delay distortion variation due to temp ( $t_{P\text{DOFF}} - t_{P\text{DON}}$ )	$t_{P\text{DISTO},t}$	-	-	20	ns	<sup>11)</sup> $C_{\text{LOAD}} = 100 \text{ pF}$ $V_{\text{IN}+} = 50\%$ , $V_{\text{OUT}} = 50\%$
Rise time	$t_{\text{RISE}}$	10	30	60	ns	$C_{\text{LOAD}} = 1 \text{ nF}$ $V_{\text{L}} 10\%$ , $V_{\text{H}} 90\%$
		200	400	800	ns	$C_{\text{LOAD}} = 34 \text{ nF}$ $V_{\text{L}} 10\%$ , $V_{\text{H}} 90\%$
Fall time	$t_{\text{FALL}}$	10	50	90	ns	$C_{\text{LOAD}} = 1 \text{ nF}$ $V_{\text{L}} 10\%$ , $V_{\text{H}} 90\%$
		200	350	600	ns	$C_{\text{LOAD}} = 34 \text{ nF}$ $V_{\text{L}} 10\%$ , $V_{\text{H}} 90\%$

#### 4.4.7 Desaturation protection

**Table 12** Desaturation protection

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Blanking capacitor charge current	$I_{\text{DESATC}}$	450	500	550	$\mu\text{A}$	$V_{\text{CC2}} = 15 \text{ V}$ , $V_{\text{VEE2}} = -8 \text{ V}$ $V_{\text{DESAT}} = 2 \text{ V}$
Blanking capacitor discharge current	$I_{\text{DESATD}}$	9	14	-	$\text{mA}$	$V_{\text{CC2}} = 15 \text{ V}$ , $V_{\text{VEE2}} = -8 \text{ V}$ $V_{\text{DESAT}} = 6 \text{ V}$
Desaturation reference level	$V_{\text{DESAT}}$	8.3	9	9.5	$\text{V}$	$V_{\text{CC2}} = 15 \text{ V}$

<sup>11)</sup> The parameter is not subject to production test - verified by design/characterization

**4 Electrical parameters**

**Table 12 Desaturation protection (continued)**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Desaturation filter time	$t_{\text{DESATfilter}}$	–	250	–	ns	$V_{\text{VCC2}} = 15 \text{ V}$ , $V_{\text{VEE2}} = -8 \text{ V}$ $V_{\text{DESAT}} = 9 \text{ V}$
Desaturation sense to <i>OUT</i> low delay	$t_{\text{DESATOUT}}$	–	350	430	ns	$V_{\text{OUT}} = 90\%$ $C_{\text{LOAD}} = 1 \text{ nF}$
Desaturation sense to <i>/FLT</i> low delay	$t_{\text{DESATFLT}}$	–	–	2.25	$\mu\text{s}$	$V_{\text{/FLT}} = 10\%$ ; $I_{\text{/FLT}} = 5 \text{ mA}$
Desaturation low voltage	$V_{\text{DESATL}}$	0.4	0.6	0.95	V	$IN+ = \text{low}$ , $IN- = \text{low}$ , $OUT = \text{low}$
Leading edge blanking	$t_{\text{DESATleb}}$	–	400	–	ns	Not subject of production test

**4 Electrical parameters**

**4.4.8 Active shut-down**

**Table 13 Active shut-down**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Active shut-down voltage	$V_{ACTSD}^{12)}$	–	–	2.0	V	$I_{OUT} = -200 \text{ mA}$ , $V_{VCC2}$ open

<sup>12)</sup> With reference to  $V_{EE2}$

## 5 Insulation characteristics

### 5 Insulation characteristics

Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.

This coupler is suitable for rated insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

#### 5.1 Tested according to VDE 0884-10 (Standard expired on Dec. 31, 2019)

Since the standard has expired on December 31, 2019, the product and its testing has not been changed.

**Table 14** According to VDE 0884-10 (Standard expired on Dec. 31, 2019)

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage $\leq 150$ V (rms) for rated mains voltage $\leq 300$ V (rms) for rated mains voltage $\leq 600$ V (rms)		I-IV I-III I-II	–
Climatic classification (IEC68-1)		40/105/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	CLR	8.12	mm
Minimum external creepage	CPG	8.24	mm
Minimum comparative tracking index	CTI	175	–
Maximum repetitive insulation voltage	$V_{IORM}$	1420	V (pk)
Input to output test voltage, method b <sup>13)</sup> $V_{IORM} * 1.875 = V_{PR}$ , 100% production test with $t_m = 1$ sec, partial discharge $< 5$ pC	$V_{PR}$	2663	V (pk)
Input to output test voltage, method a <sup>13)</sup> $V_{IORM} * 1.6 = V_{PR}$ , 100% production test with $t_m = 60$ sec, partial discharge $< 5$ pC	$V_{PR}$	2272	V (pk)
Highest allowable overvoltage	$V_{IOTM}$	6000	V (pk)
Maximum surge insulation voltage	$V_{IOSM}$	6000	V
Insulation resistance at $T_S$ , $V_{IO} = 500$ V	$R_{IO}$	$> 10^9$	$\Omega$

#### 5.2 Recognized under UL 1577 (File E311313)

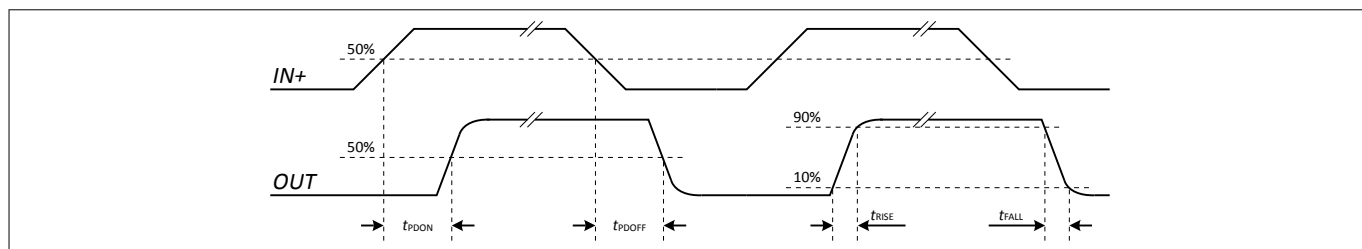
**Table 15** Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	$V_{ISO}$	3750	V (rms)
Insulation test voltage / 1 s	$V_{ISO,test}$	4500	V (rms)

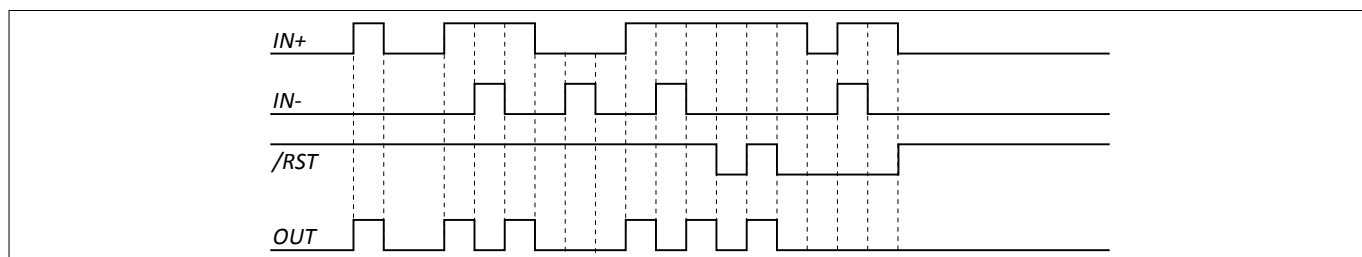
<sup>13</sup> Refer to VDE 0884 for a detailed description of Method a and Method b partial discharge test profiles.

6 Timing diagrams

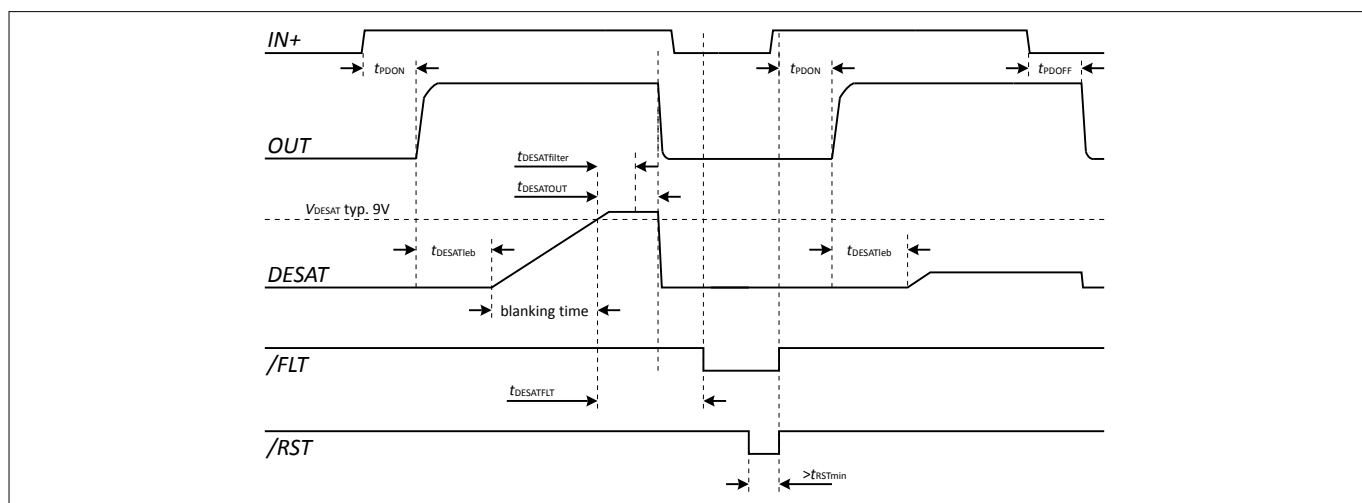
**6 Timing diagrams**



**Figure 6 Propagation delay, rise and fall time**

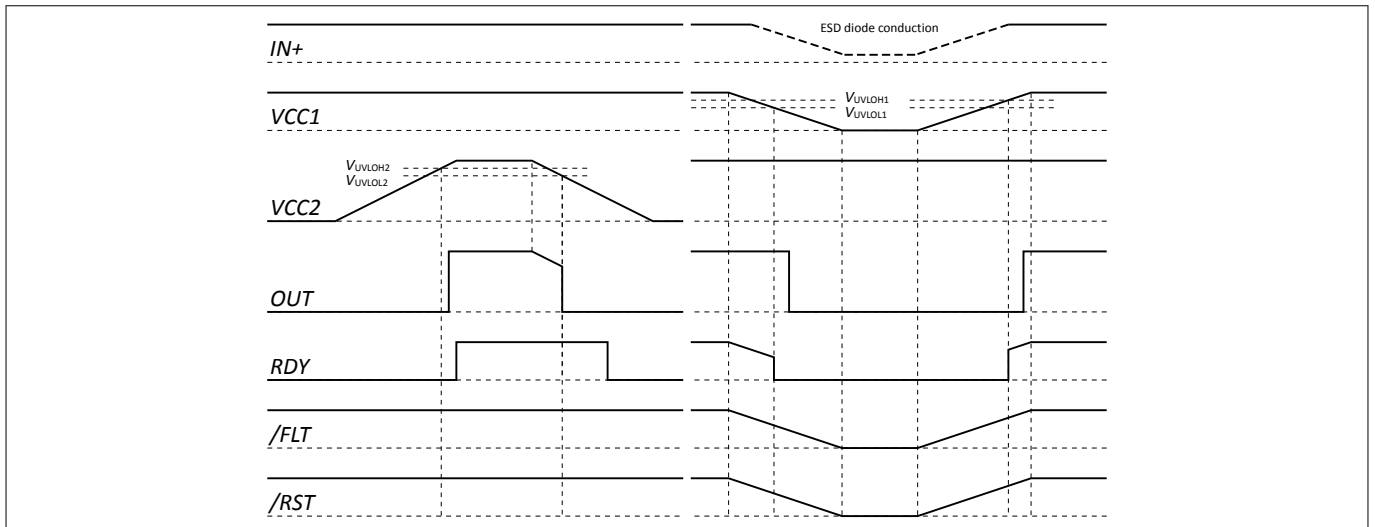


**Figure 7 Typical switching behavior**



**Figure 8 DESAT switch-off behavior**

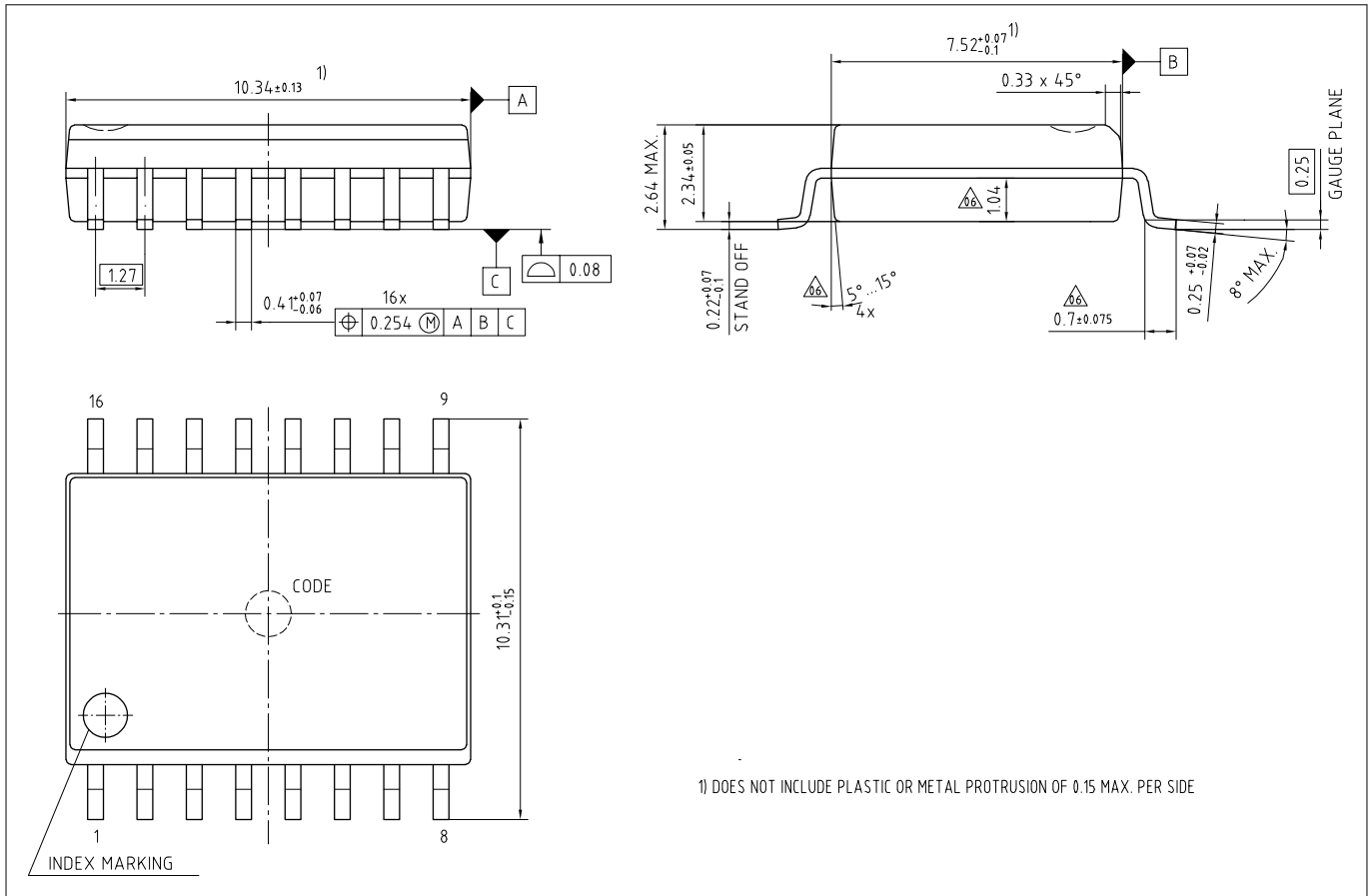
**6 Timing diagrams**



**Figure 9** UVLO behavior

**7 Package outline**

**7 Package outline**



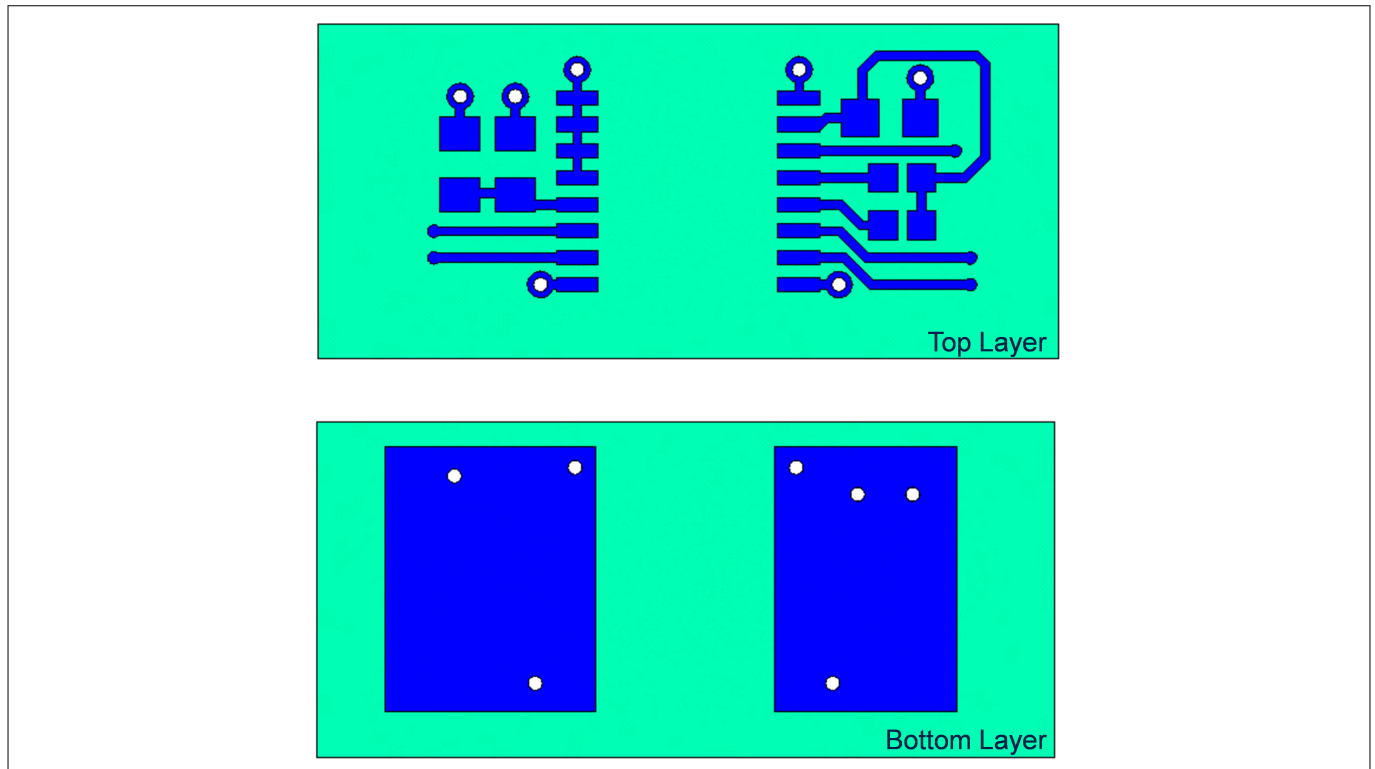
**Figure 10** PG-DSO-16-15 300 mil body

**8 Application notes**

**8.1 Reference layout for thermal data**

The PCB layout shown in [Figure 11](#) represents the reference layout used for the thermal characterization. Pins 9 and 16 (*GND1*) and pins 1 and 8 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The 1ED020I12-B2 is conceived to dissipate most of the heat generated through this pins.

## 8 Application notes



**Figure 11** Reference layout for thermal data (Copper thickness 102  $\mu\text{m}$ )

### 8.2 Printed circuit board guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.
- Lowest trace length for *VEE2* to *GND2* decoupling could be achieved with capacitor closed to pins 1 and 3.



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**9 Revision history**

## **9 Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
v2.2	2020-01-01	<ul style="list-style-type: none"><li>• Update to new template</li><li>• Editorial changes to headlines, descriptions and figures</li><li>• Update to VDE 0884-10 expiration date, product and testing have not been changed</li></ul>
v2.1	2017-09-28	<ul style="list-style-type: none"><li>• Upgrade common mode transient immunity rating to 100 kV/μs, change typo <math> DV_{ISO}/dt </math> to <math> dV_{ISO}/dt </math></li><li>• Editorial changes to headlines, descriptions and figures</li></ul>

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