

MOSFET

600V CoolMOS™ C7 Power Transistor

CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)} \cdot A$ below $10\text{Ohm} \cdot \text{mm}^2$.

Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- SMD package with very low parasitic inductance for easy device control
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- 4pin kelvin source concept

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Optimized PCB assembly and layout solutions
- Suitable for applications such as server, telecom and solar
- Up to 0.5% better full load efficiency @100kHz compared to conventional 3pin package

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	65	mΩ
$Q_{g,typ}$	68	nC
$I_{D,pulse}$	135	A
$I_{D,continuous} @ T_j < 150^\circ\text{C}$	51	A
$E_{oss} @ 400\text{V}$	8.1	μJ
Body diode di_f/dt	370	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPL60R065C7	PG-VSON-4	60C7065	see Appendix A

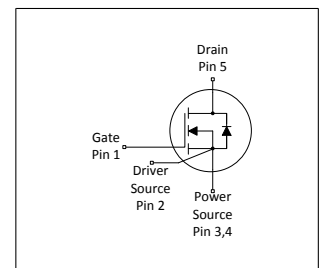
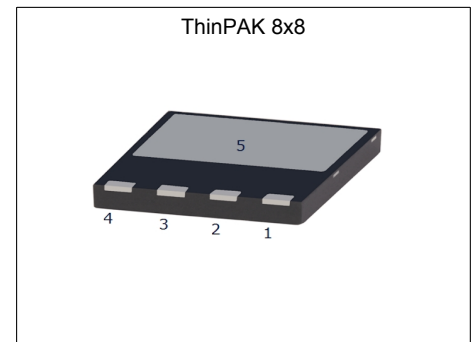


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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	29 22	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	135	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	159	mJ	$I_D=6.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.80	mJ	$I_D=6.4\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	6.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	180	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	29	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	135	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	20	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9.9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _F /dt	-	-	370	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 9.9\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.696	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL2a

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}, I_D=0.8mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=600, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.056 0.125	0.065	Ω	$V_{GS}=10V, I_D=15.9A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=15.9A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2850	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	C_{oss}	-	54	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	101	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	1050	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=15.9A,$ $R_G=3.3\Omega$; see table 9
Rise time	t_r	-	5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=15.9A,$ $R_G=3.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	57	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=15.9A,$ $R_G=3.3\Omega$; see table 9
Fall time	t_f	-	3.5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=15.9A,$ $R_G=3.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	14	-	nC	$V_{DD}=400V, I_D=15.9A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	23	-	nC	$V_{DD}=400V, I_D=15.9A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	68	-	nC	$V_{DD}=400V, I_D=15.9A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400V, I_D=15.9A, V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=15.9A, T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	390	-	ns	$V_R=400V, I_F=15.9A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	6	-	μC	$V_R=400V, I_F=15.9A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	32	-	A	$V_R=400V, I_F=15.9A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

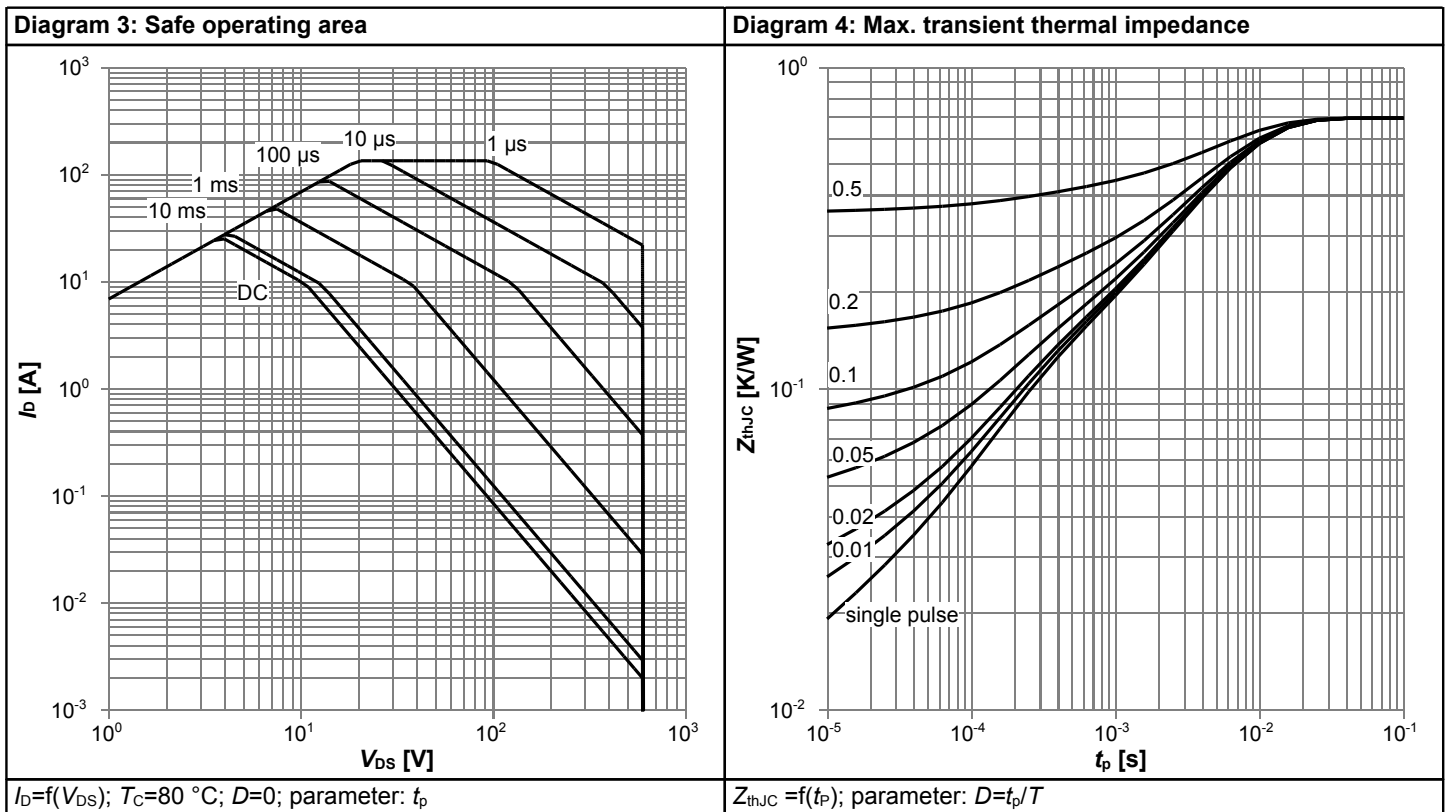
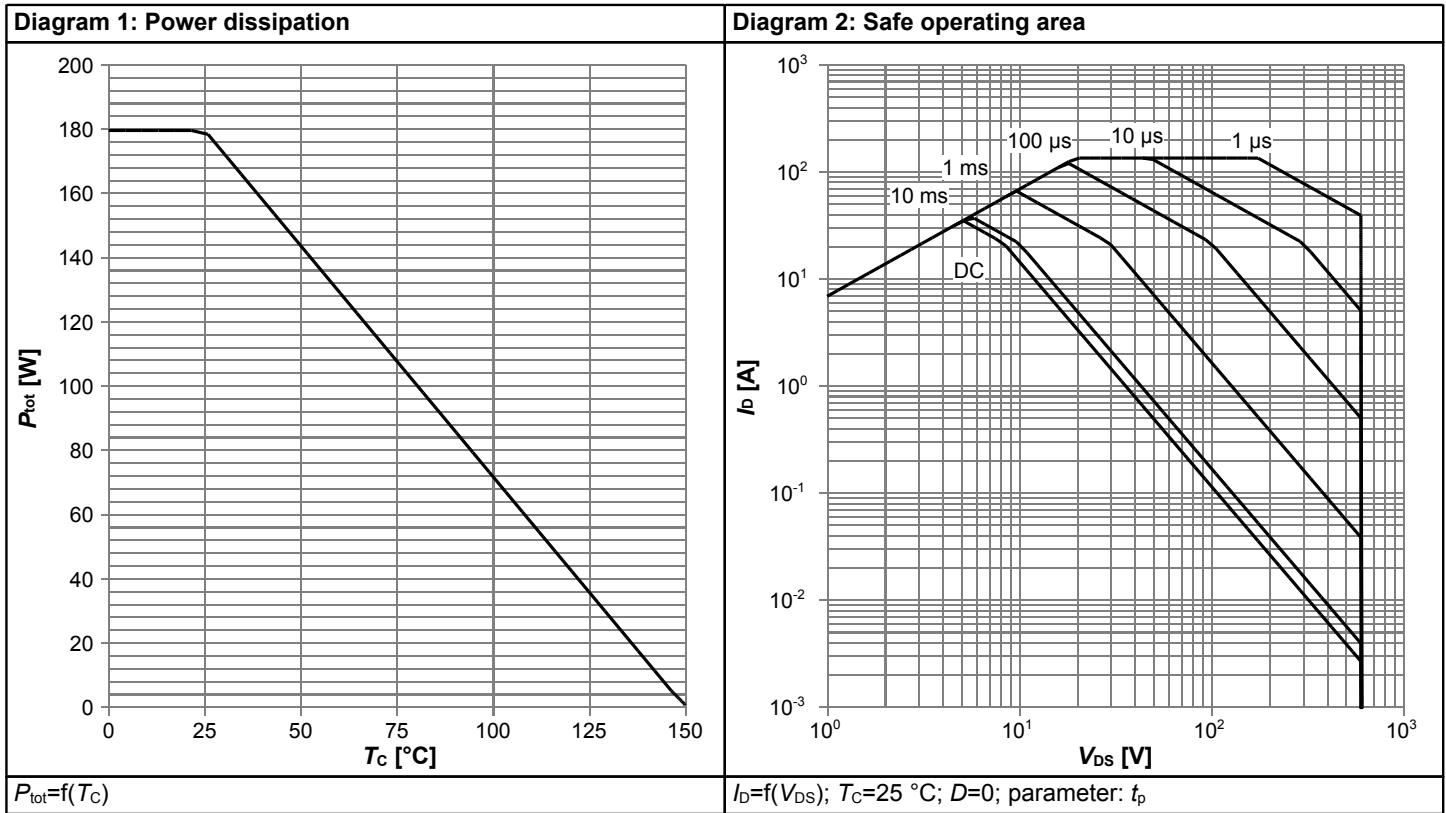
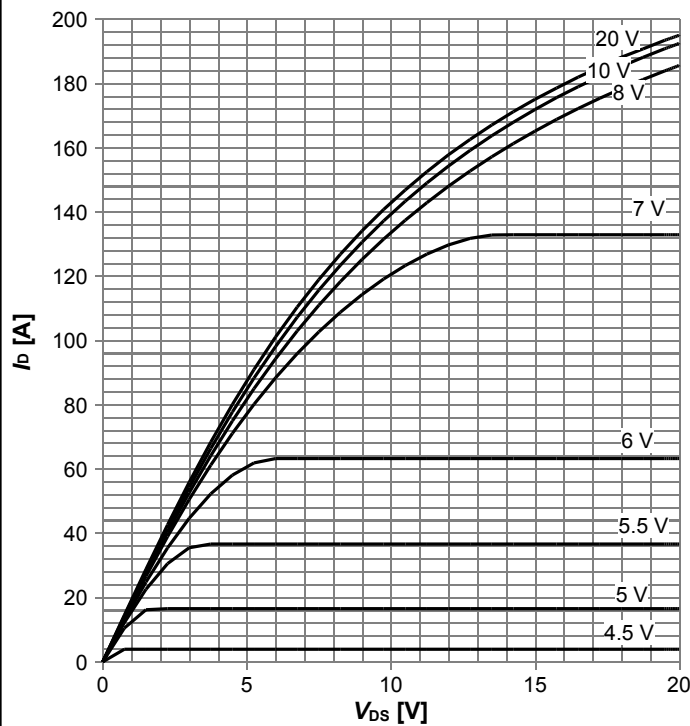
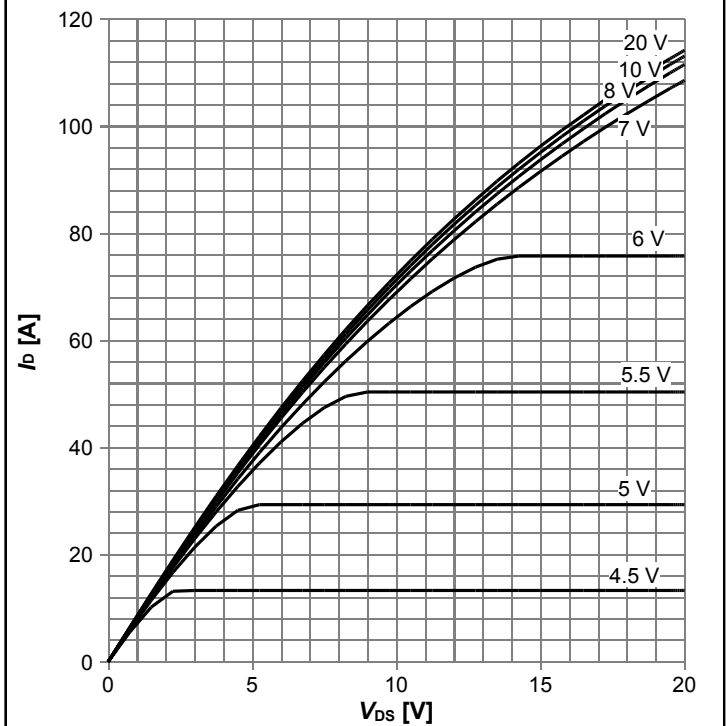


Diagram 5: Typ. output characteristics



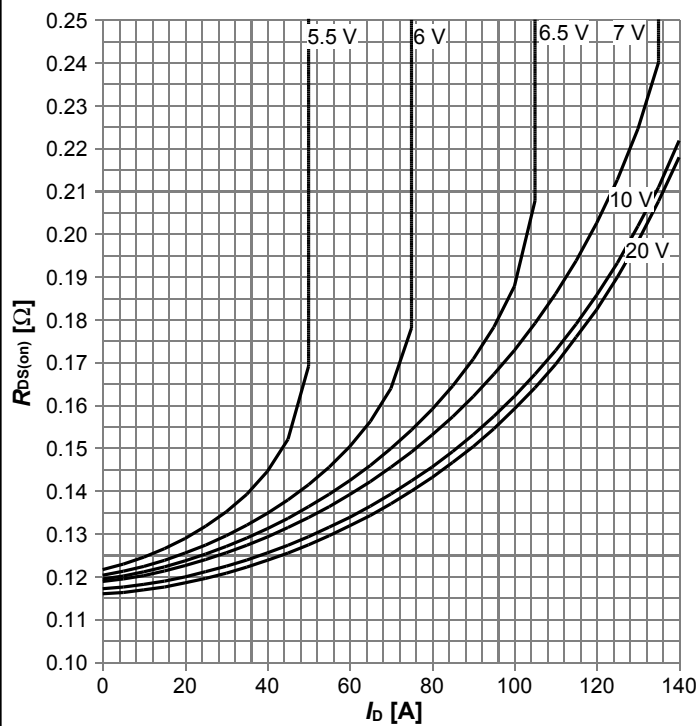
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



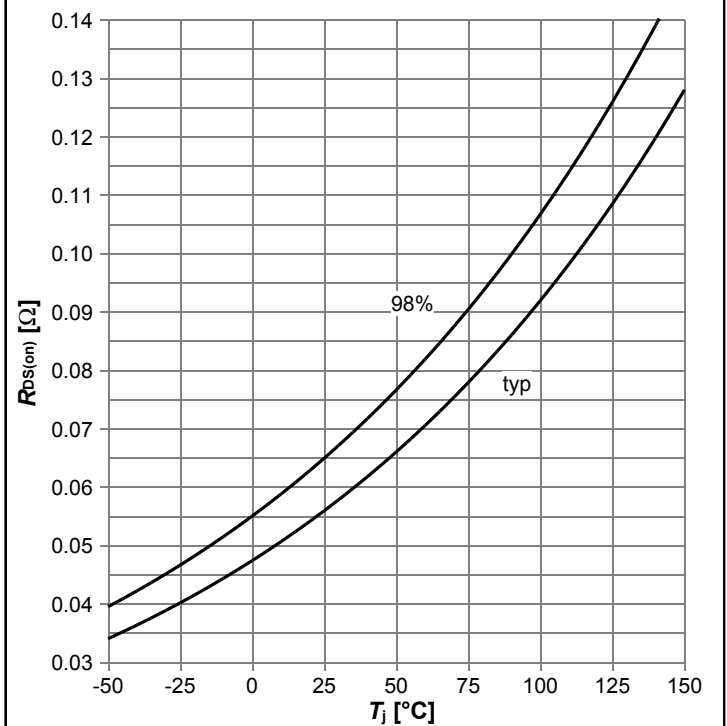
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



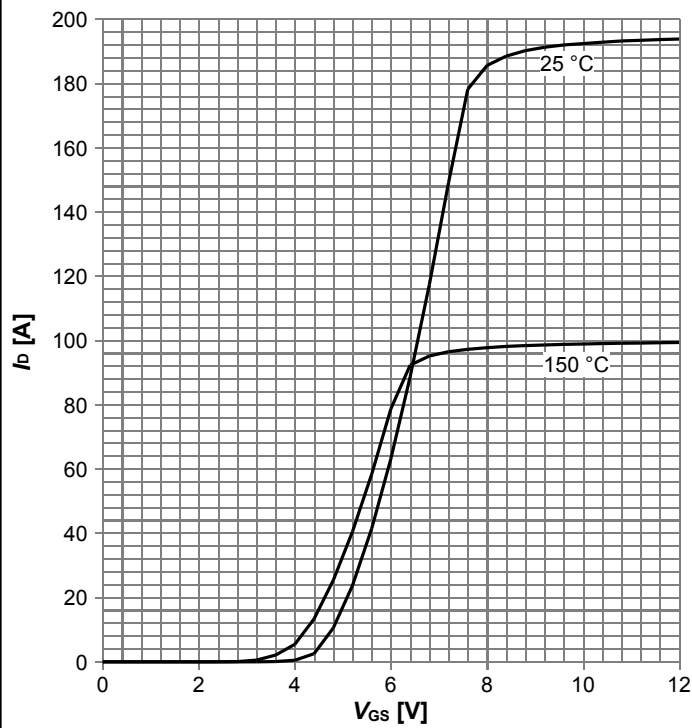
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



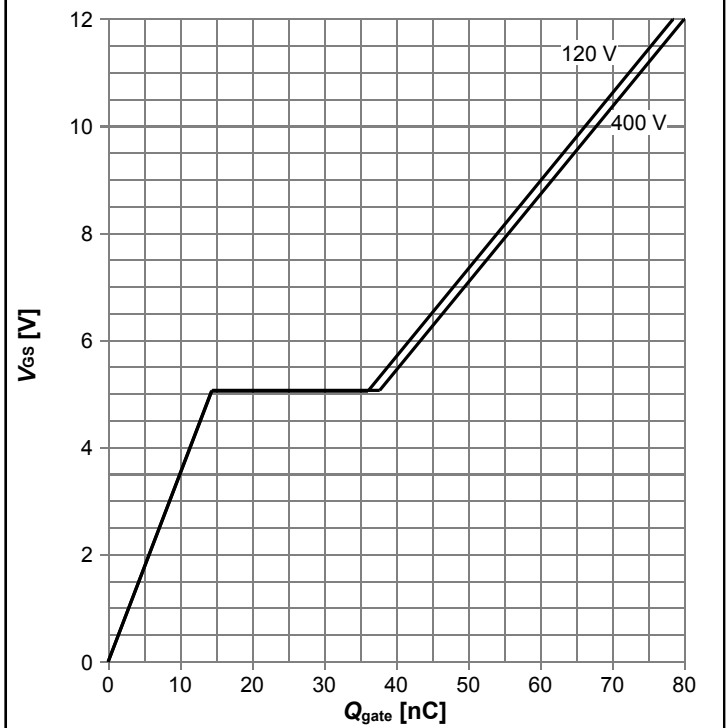
$R_{DS(on)}=f(T_j)$; $I_D=15.9\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



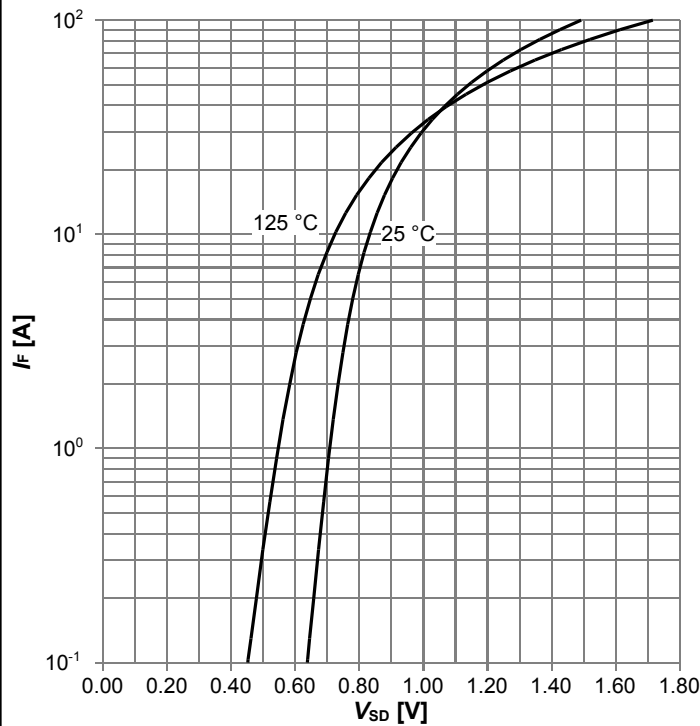
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



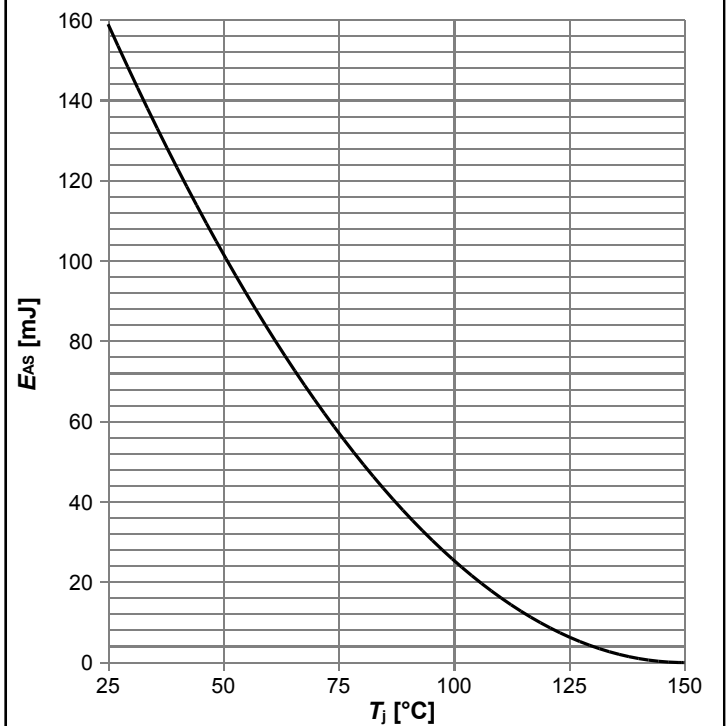
$V_{GS} = f(Q_{gate}); I_D = 15.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



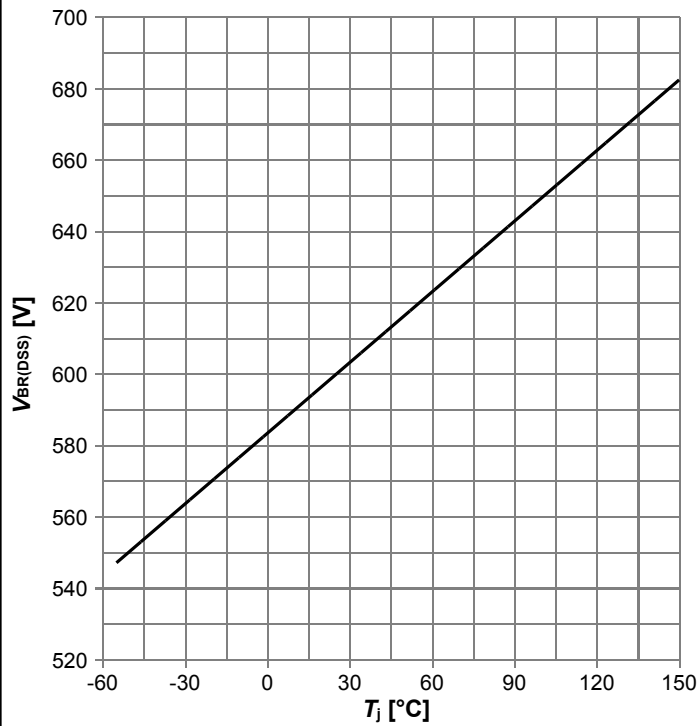
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



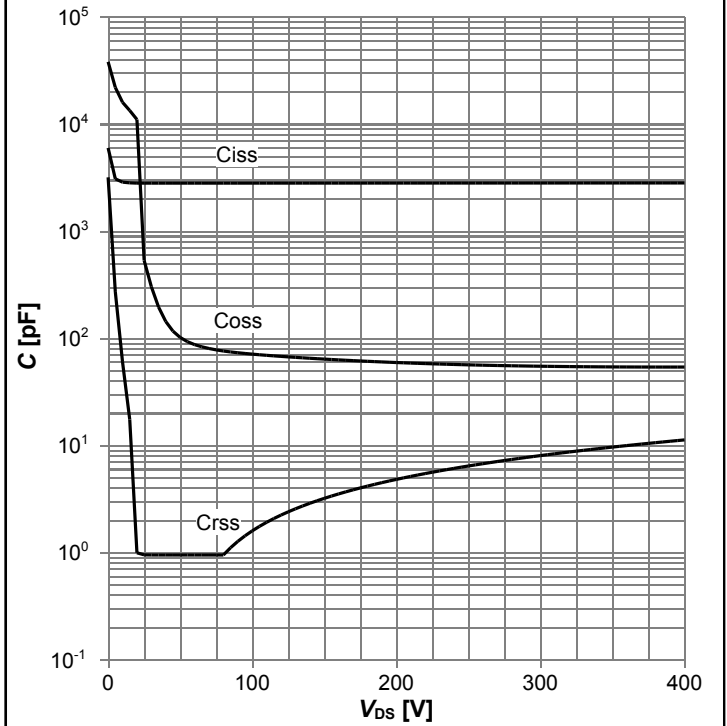
$E_{AS} = f(T_j); I_D = 6.4 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



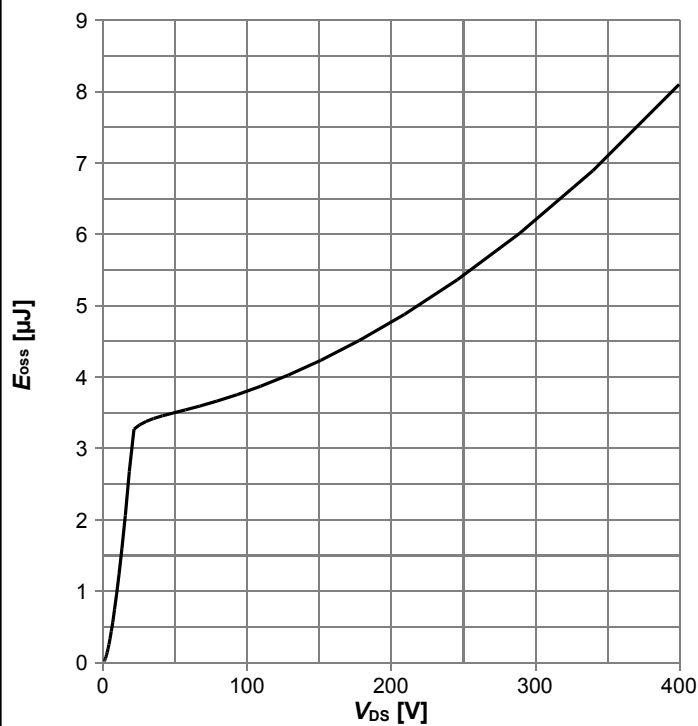
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

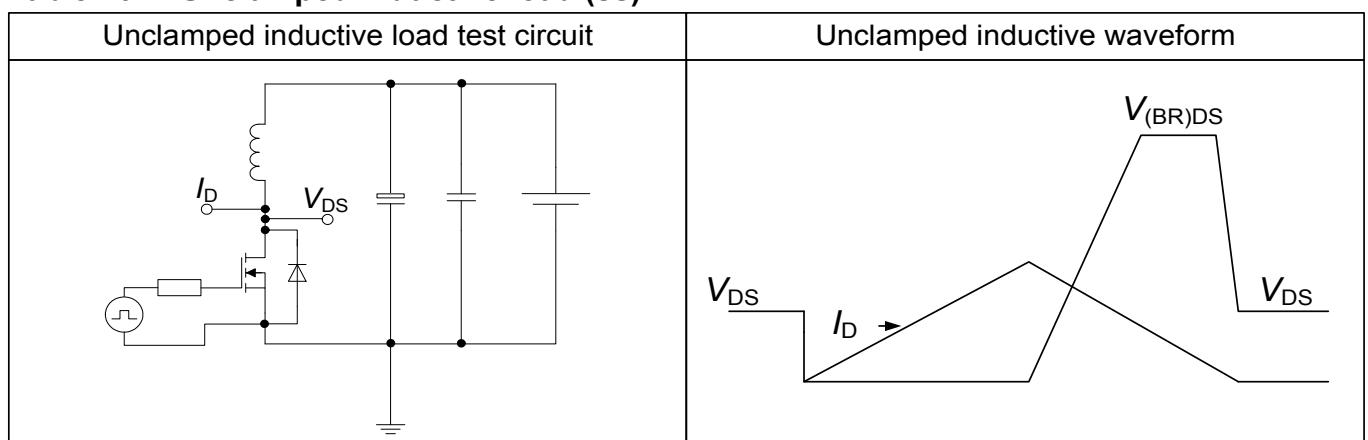
Table 8 Diode characteristics



Table 9 switching times (ss)



Table 10 Unclamped inductive load (ss)



6 Package Outlines



Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPL60R065C7

Revision: 2017-08-30, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-12-11	Release of final version
2.1	2017-08-30	Updated MSL

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