

## MOSFET

### 600V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

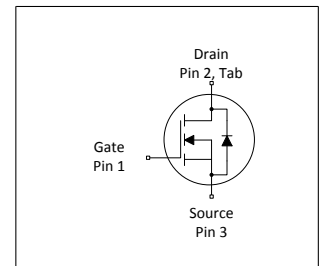
#### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

#### Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	1500	$m\Omega$
$I_d$	5	A
$Q_{g,typ}$	9.4	nC
$I_{D,pulse}$	8	A
$E_{oss@400V}$	1	$\mu J$

Type / Ordering Code	Package	Marking	Related Links
IPA60R1K5CE	PG-TO 220 FullPAK	60S1K5CE	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	5 3.2	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	8	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	26	mJ	$I_D=0.6\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 11
Avalanche energy, repetitive	$E_{AR}$	-	-	0.09	mJ	$I_D=0.6\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 11
Avalanche current, repetitive	$I_{AR}$	-	-	0.6	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation (FullPAK) TO-220FP	$P_{tot}$	-	-	20	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	$I_S$	-	-	3.5	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	8	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 9
Maximum diode commutation speed	di/dt	-	-	500	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 9
Insulation withstand voltage for TO-220FP	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$
Power dissipation TO-252	$P_{tot}$	-	-	49	W	$T_C=25^\circ\text{C}$

## 2 Thermal characteristics

**Table 3 Thermal characteristics (FullPAK) TO-220FP**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	6.4	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	$^\circ\text{C/W}$	leaded
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	$^\circ\text{C}$	1.6mm (0.063 in.) from case for 10s

<sup>1)</sup> Limited by  $T_{j,max}$ , TO252 equivalent, Maximum duty cycle  $D=0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=0.25mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.09mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=600, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=600, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.26 3.28	1.50	$\Omega$	$V_{GS}=10V, I_D=1.1A, T_j=25^\circ C$ $V_{GS}=10V, I_D=1.1A, T_j=150^\circ C$
Gate resistance	$R_G$	-	14	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	200	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	16	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	11	-	pF	$V_{GS}=0V, V_{DS}=0...480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	41.3	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A,$ $R_G=12.2\Omega; \text{see table 10}$
Rise time	$t_r$	-	7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A,$ $R_G=12.2\Omega; \text{see table 10}$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A,$ $R_G=12.2\Omega; \text{see table 10}$
Fall time	$t_f$	-	20	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.4A,$ $R_G=12.2\Omega; \text{see table 10}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.1	-	nC	$V_{DD}=480V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	5	-	nC	$V_{DD}=480V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	9.4	-	nC	$V_{DD}=480V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480V, I_D=1.4A, V_{GS}=0 \text{ to } 10V$

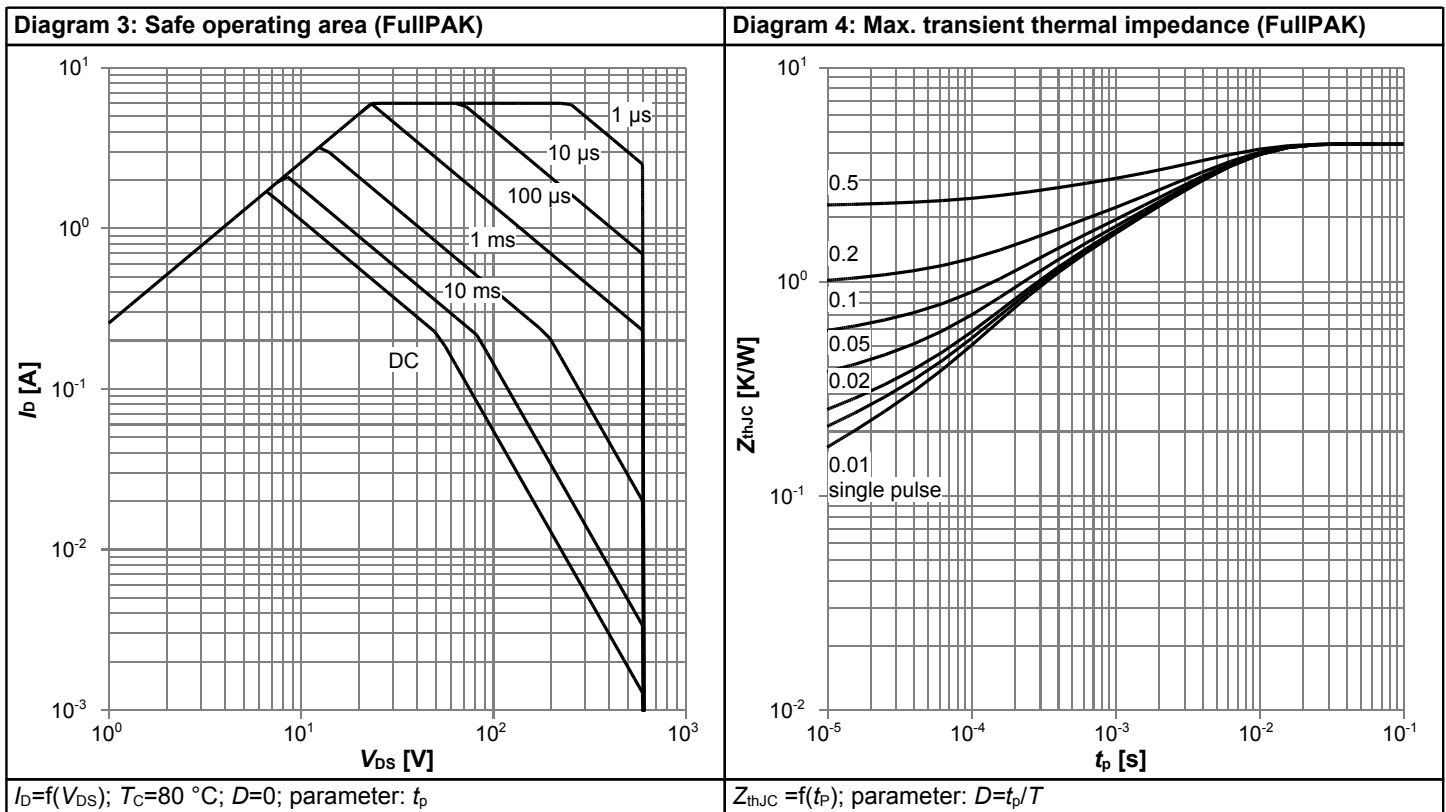
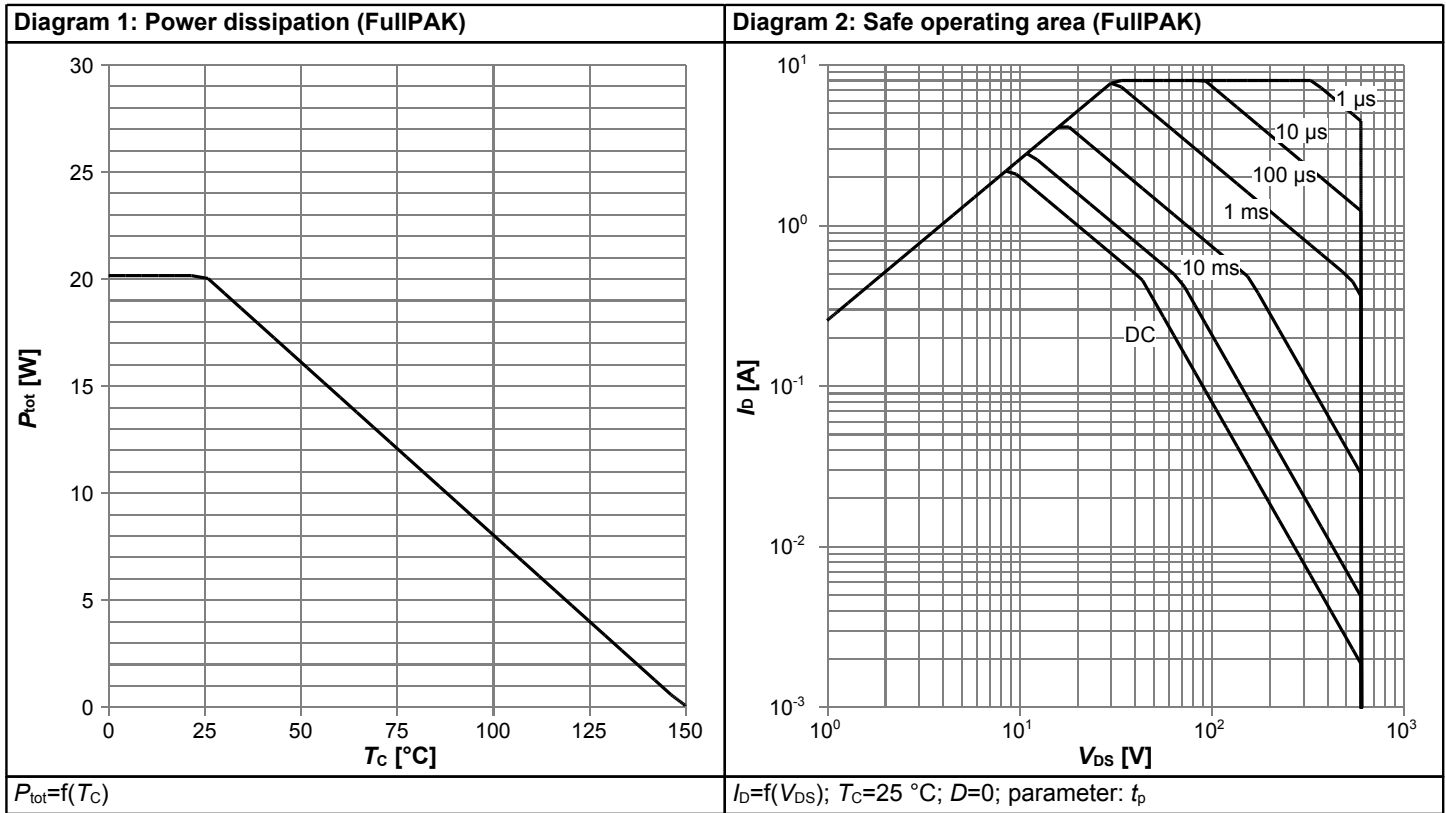
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{o(BR)DSS}$

**Table 7 Reverse diode characteristics**

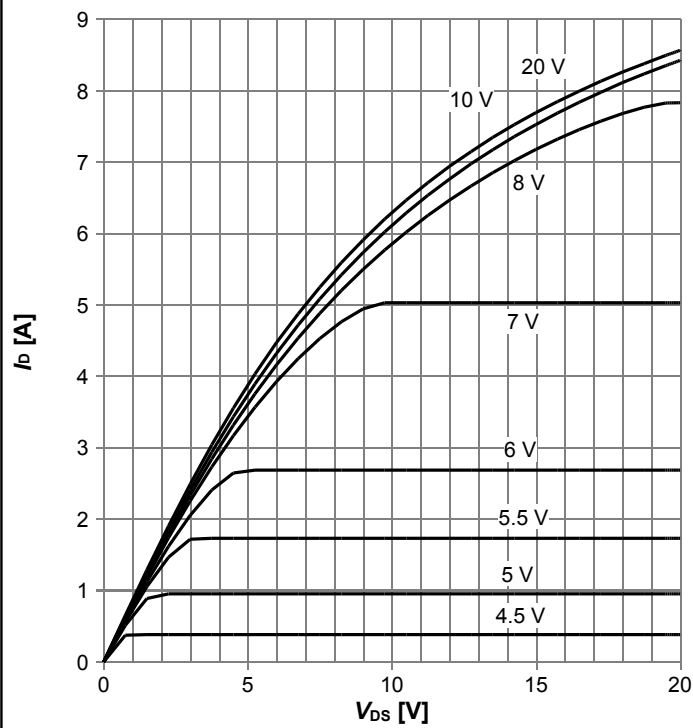
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=1.4A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	230	-	ns	$V_R=400V, I_F=1.4A, di_F/dt=100A/\mu s$ ; see table 9
Reverse recovery charge	$Q_{rr}$	-	1.1	-	$\mu C$	$V_R=400V, I_F=1.4A, di_F/dt=100A/\mu s$ ; see table 9
Peak reverse recovery current	$I_{rrm}$	-	9.8	-	A	$V_R=400V, I_F=1.4A, di_F/dt=100A/\mu s$ ; see table 9

**4 Electrical characteristics diagrams**



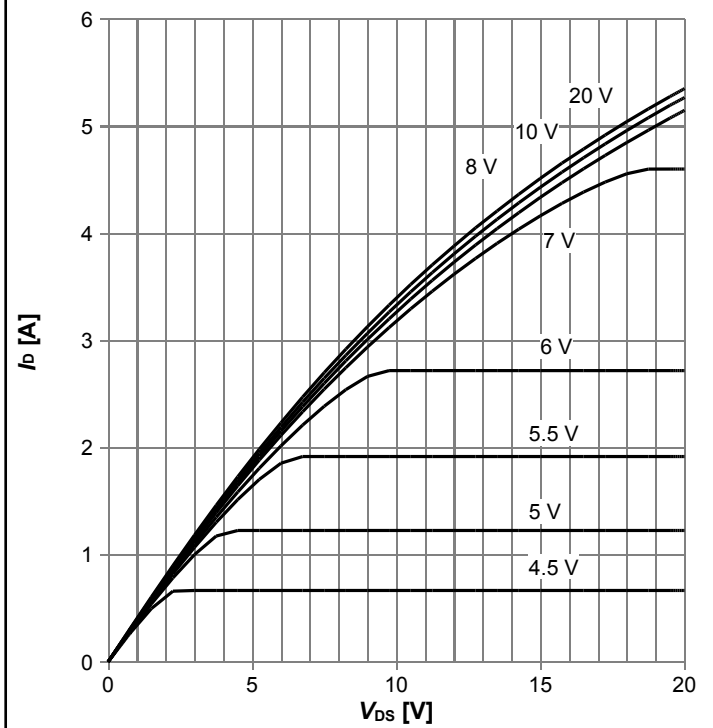
# 600V CoolMOS™ CE Power Transistor IPA60R1K5CE

Diagram 5: Typ. output characteristics



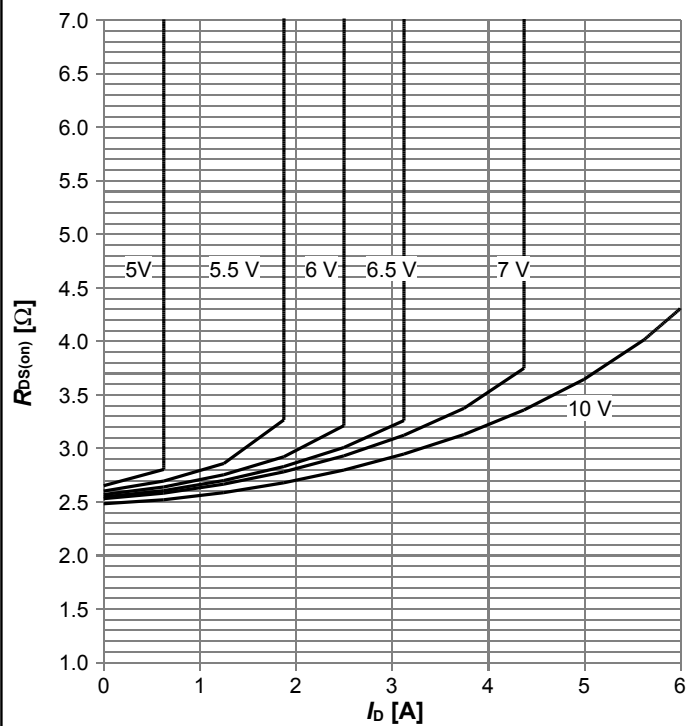
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



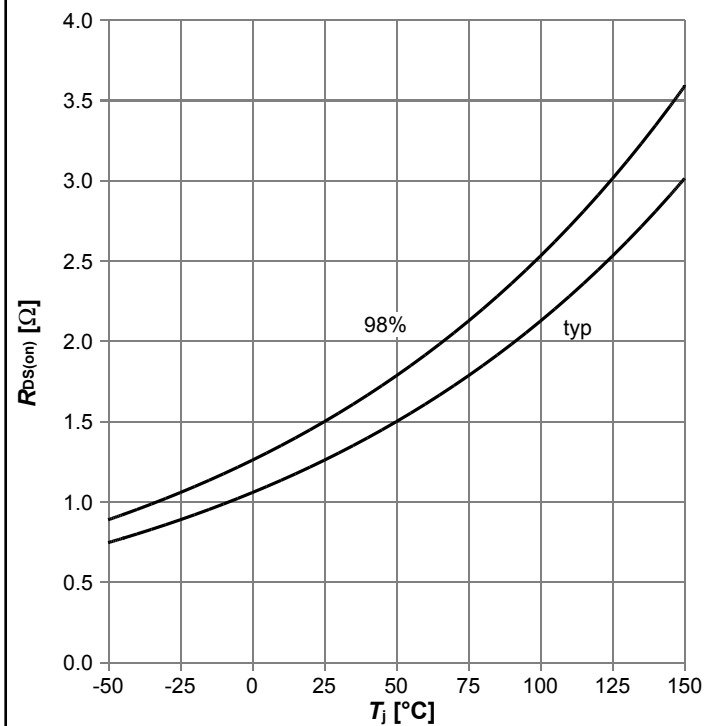
$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance

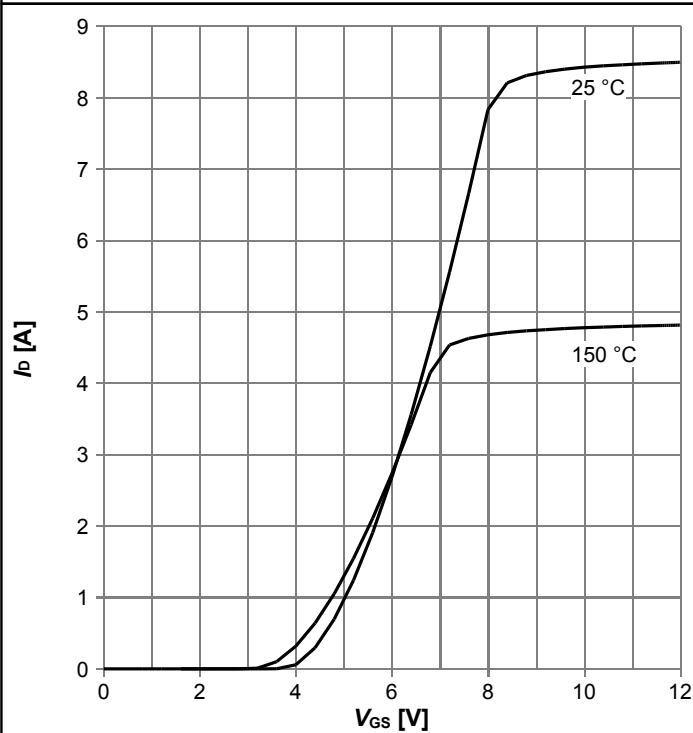


$R_{DS(on)}=f(T_j); I_D=1.1\text{ A}; V_{GS}=10\text{ V}$

# 600V CoolMOS™ CE Power Transistor

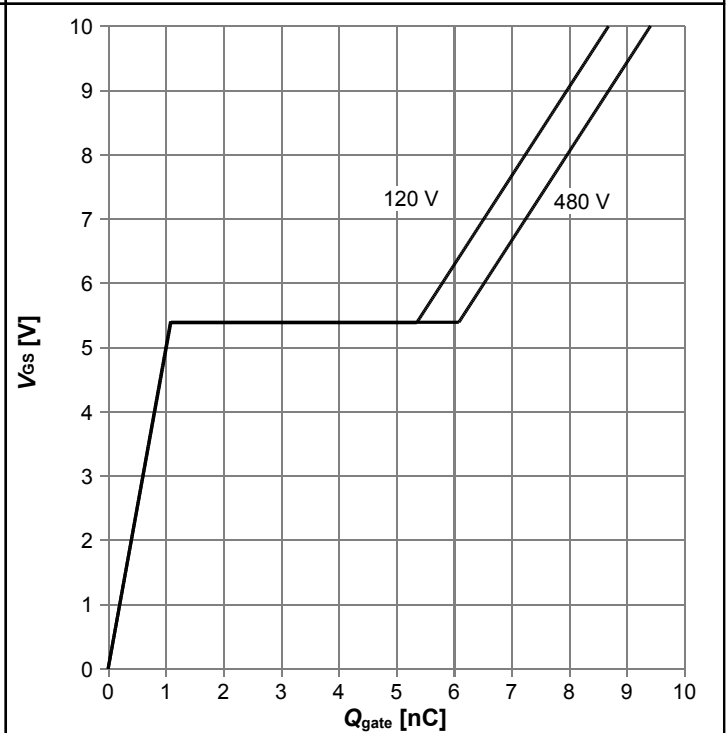
## IPA60R1K5CE

Diagram 9: Typ. transfer characteristics



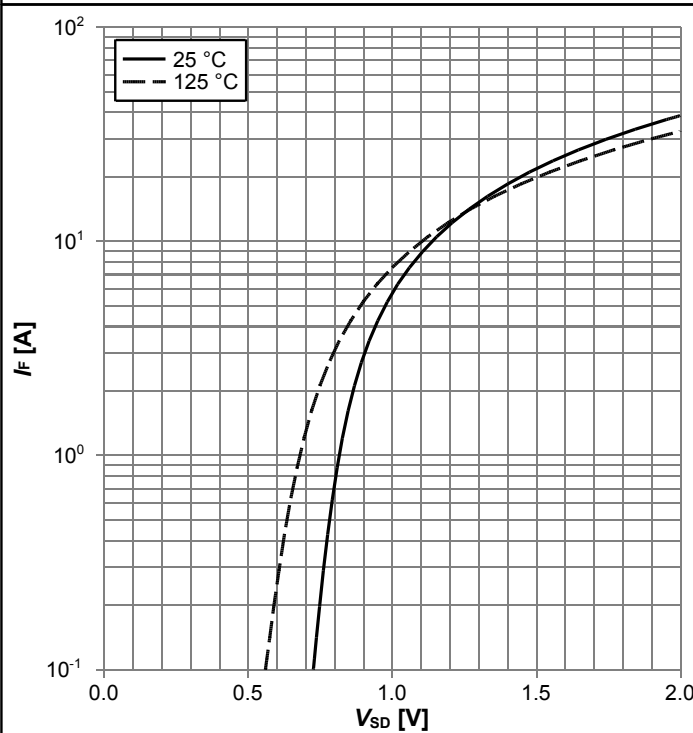
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



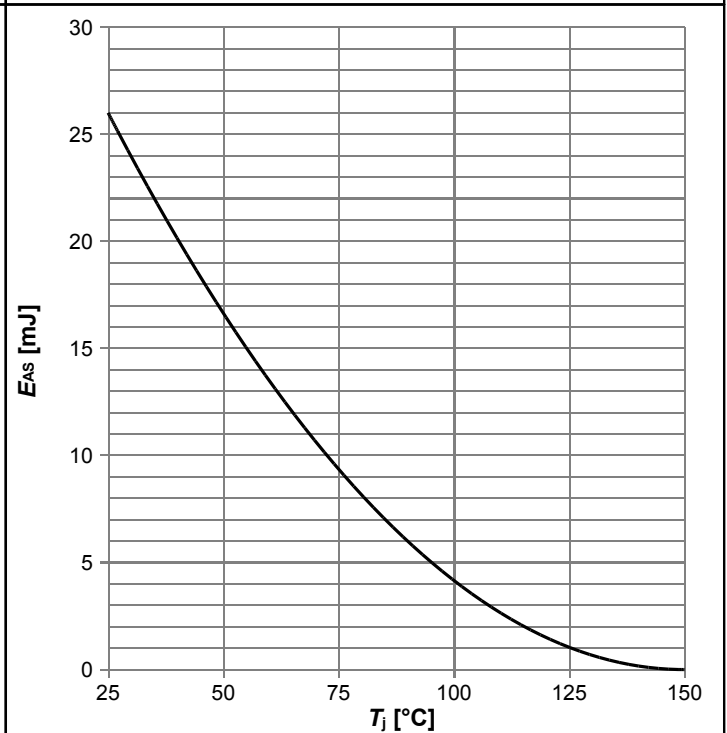
$V_{GS} = f(Q_{gate})$ ;  $I_D = 1.4 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy

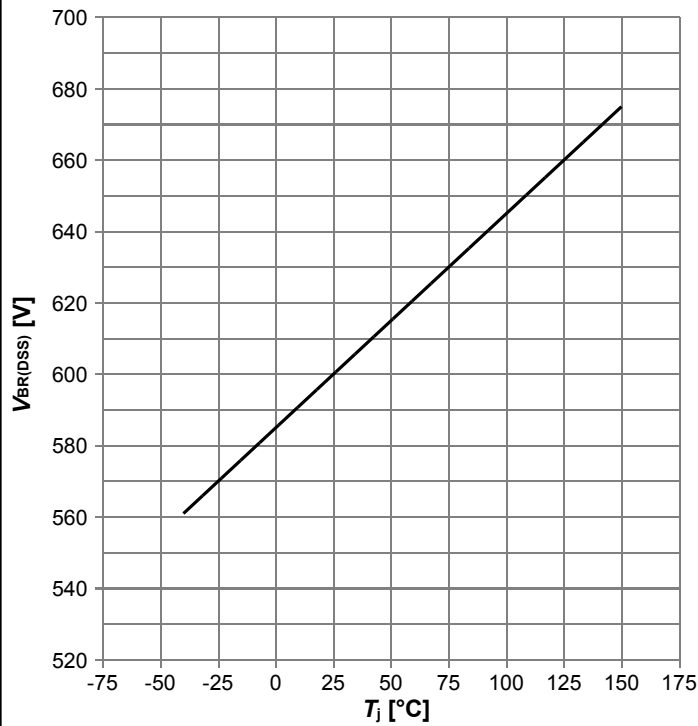


$E_{AS} = f(T_j)$ ;  $I_D = 0.6 A$ ;  $V_{DD} = 50 V$



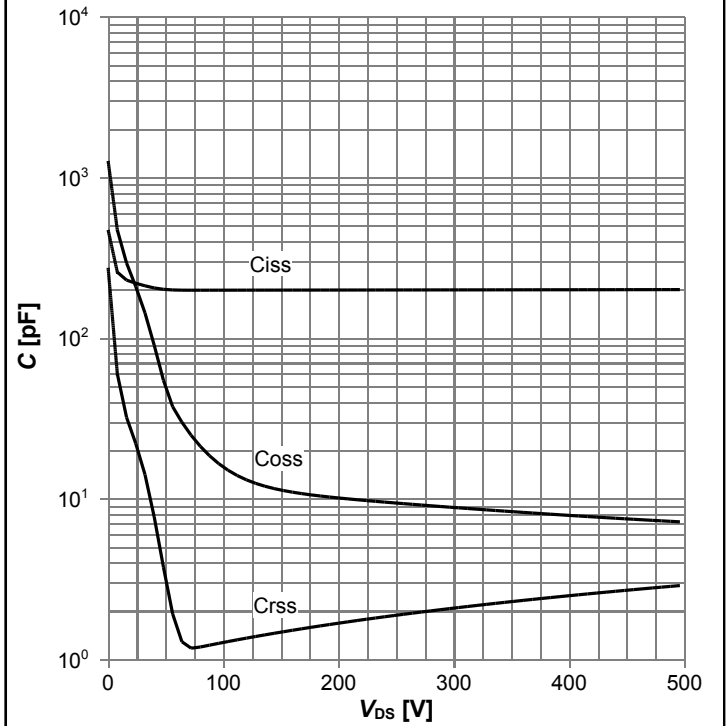
**600V CoolMOS™ CE Power Transistor**  
**IPA60R1K5CE**

**Diagram 13: Drain-source breakdown voltage**



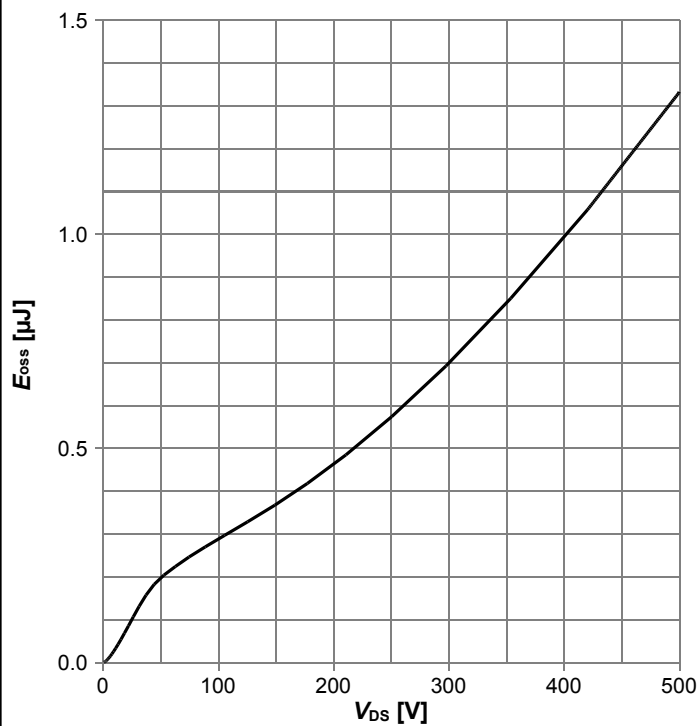
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{tr} = t_F + t_S</math>  <math>Q_{tr} = Q_F + Q_S</math></p>

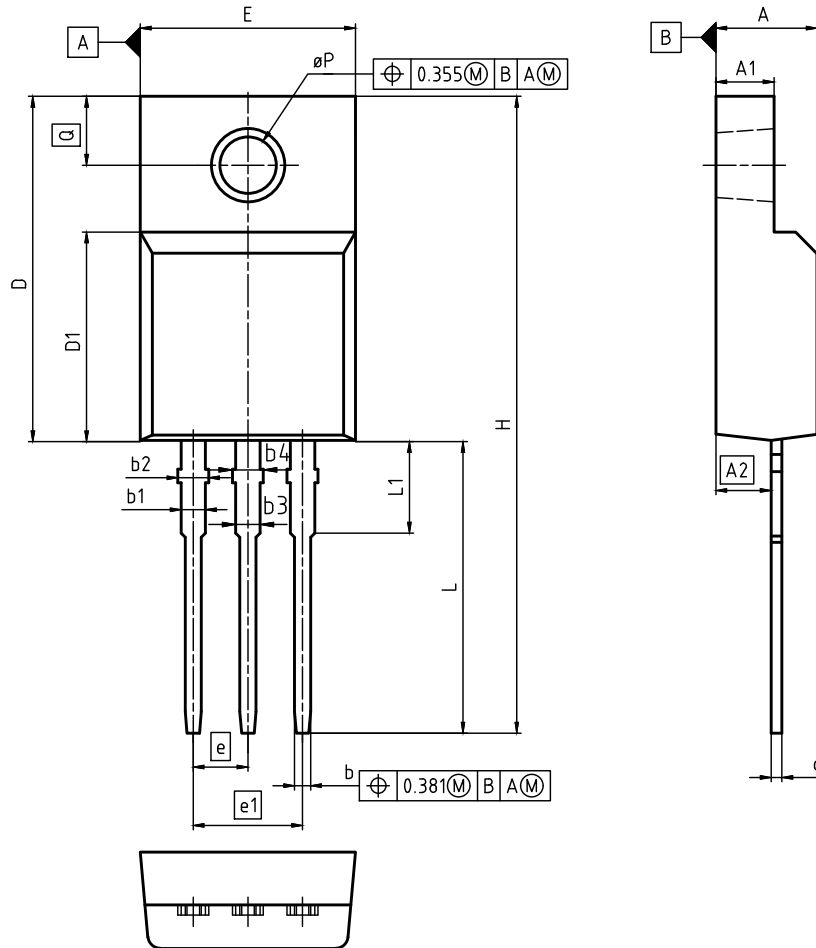
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
$\varnothing P$	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

Dimensions do not include mold flash, protrusions or gate burrs

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EUROPEAN PROJECTION

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04

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

## 7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ CE simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPA60R1K5CE

Revision: 2016-02-26, Rev. 2.0

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-02-26	Release of final version

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