OptiMOS®2 Power-Transistor

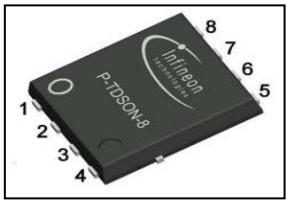
Features

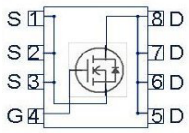
- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC converters
- Qualified according to JEDEC[1] for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- Avalanche rated
- dv/dt rated

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	2.2	mΩ
I_D	50	A

P-TDSON-8





Type	Package	Ordering Code	Marking
BSC022N03S	P-TDSON-8	Q67042-S4218	22N03S

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	50	A
		T_C=100 °C	50	
		T_A=25 °C, R_{thJA}=45 K/W[2]	28	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[3]	200	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	800	mJ
Reverse diode dv/dt	dv/dt	I_D=50 A, V_{DS}=24 V, di/dt=200 A/µs, $T_{j,max}$=150 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	104	W
		T_A=25 °C, R_{thJA}=45 K/W[2]	2.8	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.2	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[2)]	-	-	45	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=100 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	2.6	3.3	mΩ
		V_{GS}=10 V, I_D=50 A	-	1.8	2.2	
Gate resistance	R_G		0.3	0.6	1.2	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	70	140	-	S

[1)] J-STD20 and JESD22

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

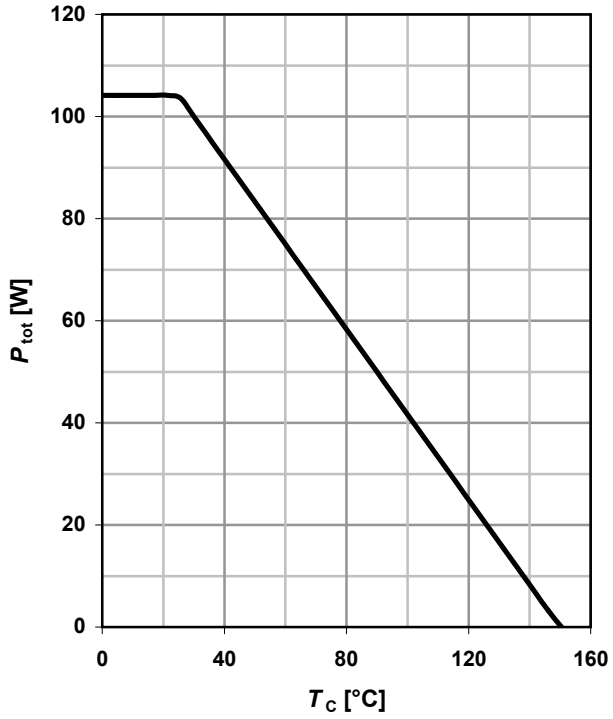
[3)] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	5630	7490	pF
Output capacitance	C_{oss}		-	2000	2660	
Reverse transfer capacitance	C_{rss}		-	251	376	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=25 A, R_G=2.7 Ω	-	9.7	14	ns
Rise time	t_r		-	9	13	
Turn-off delay time	$t_{d(off)}$		-	42	62	
Fall time	t_f		-	7	11	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=25 A, V_{GS}=0 to 5 V	-	16	21	nC
Gate charge at threshold	$Q_{g(th)}$		-	9	12	
Gate to drain charge	Q_{gd}		-	11	16	
Switching charge	Q_{sw}		-	17	25	
Gate charge total	Q_g		-	43	58	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 5 V	-	38	51	nC
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	48	63	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.81	1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	20	nC

[4)] See figure 16 for gate charge parameter definition

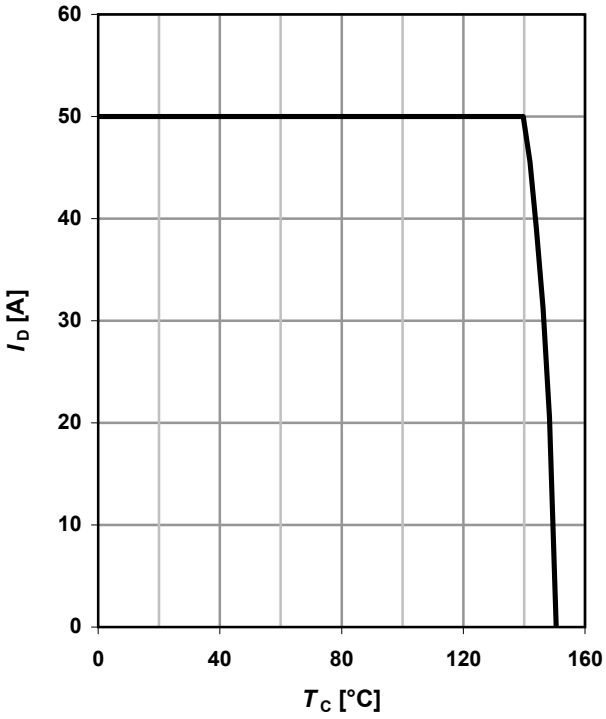
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

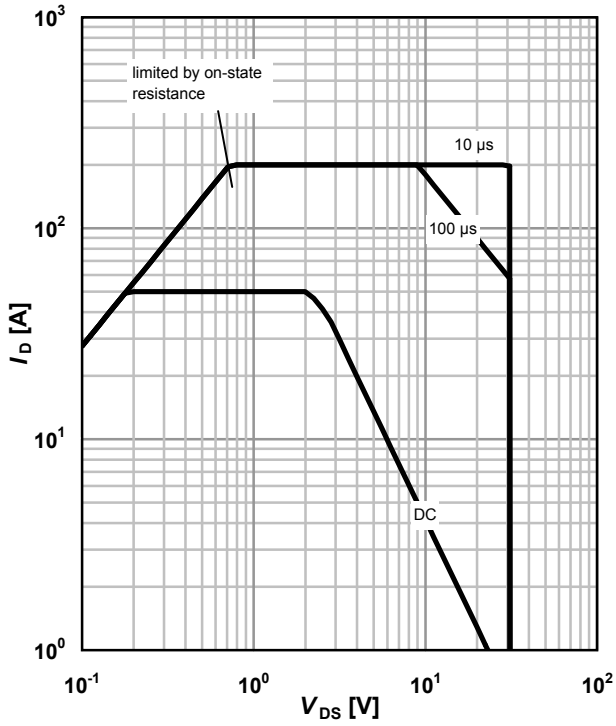
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

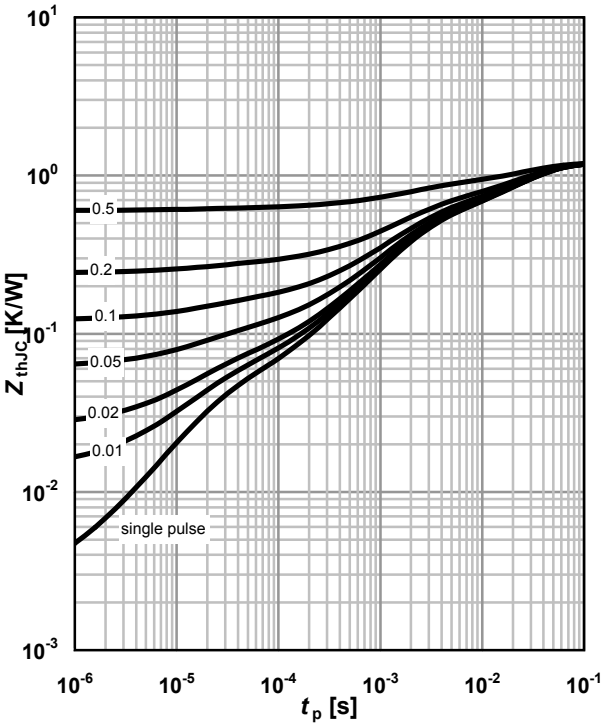
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

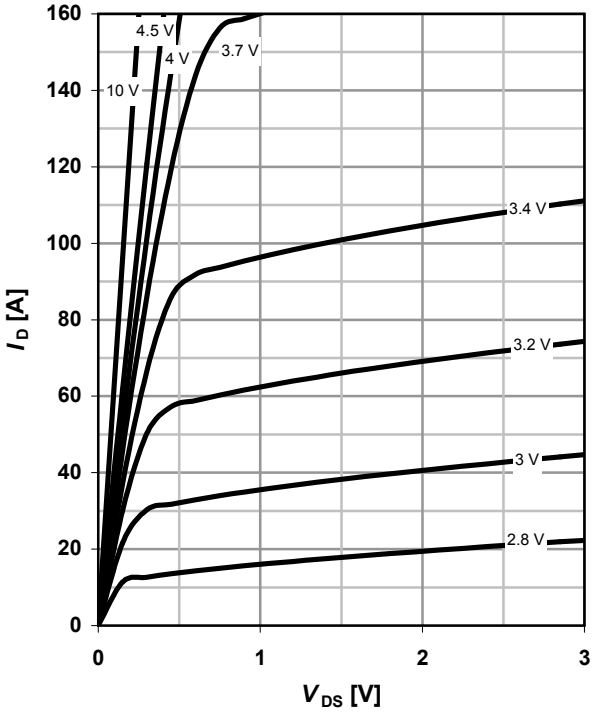
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

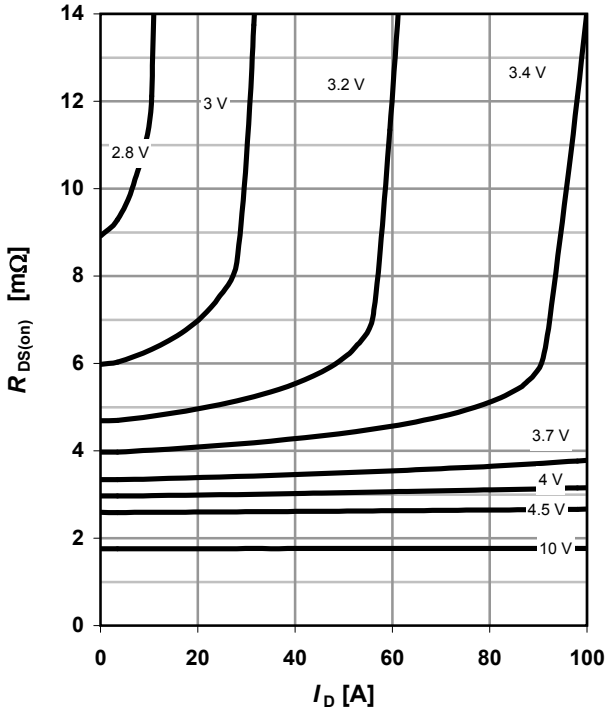
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

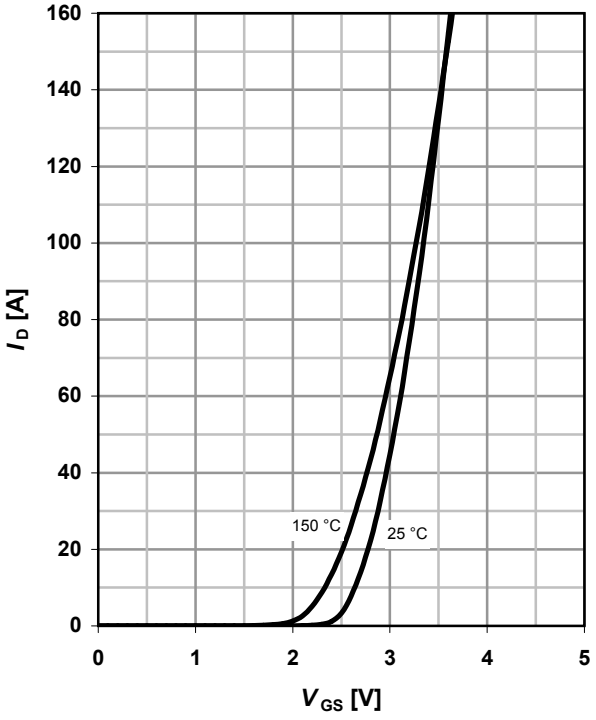
parameter: V_{GS}



7 Typ. transfer characteristics

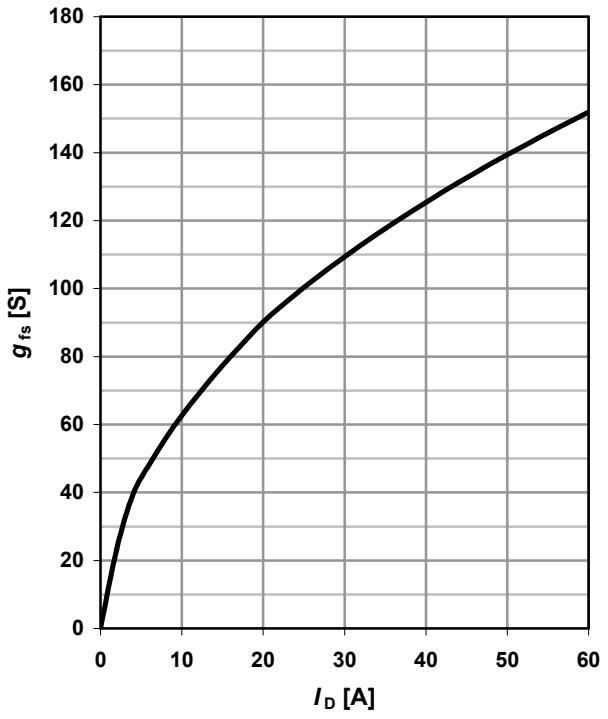
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



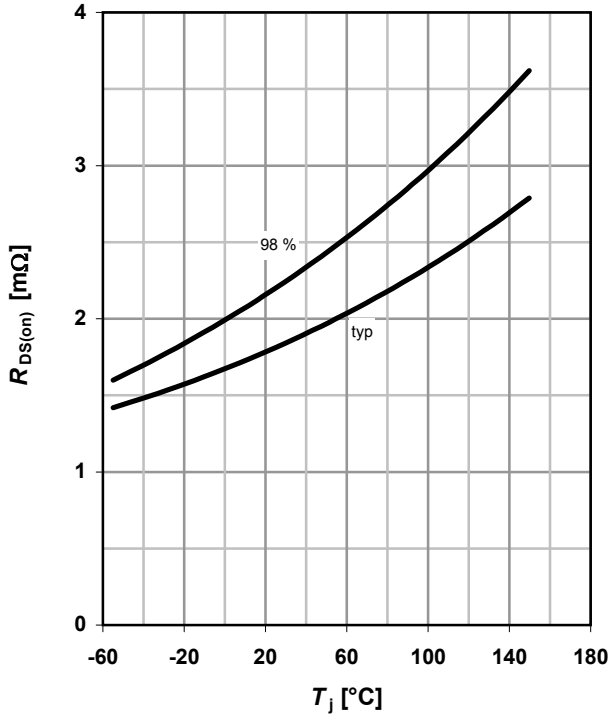
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

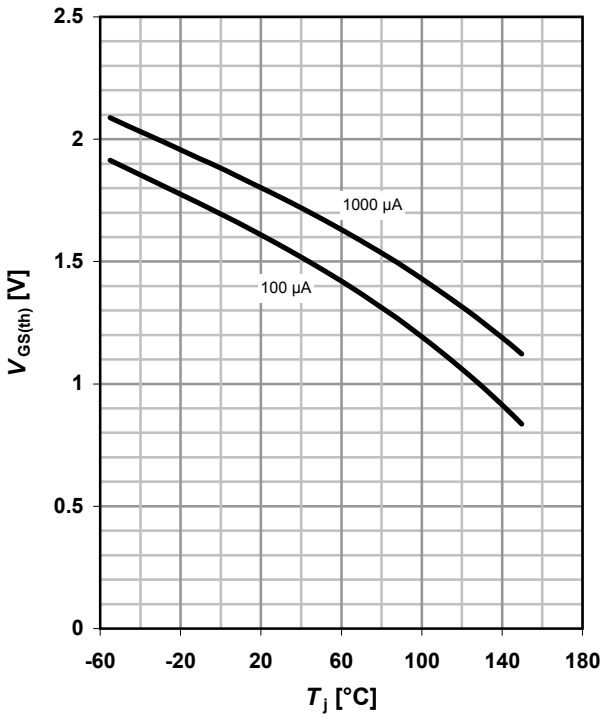
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



10 Typ. gate threshold voltage

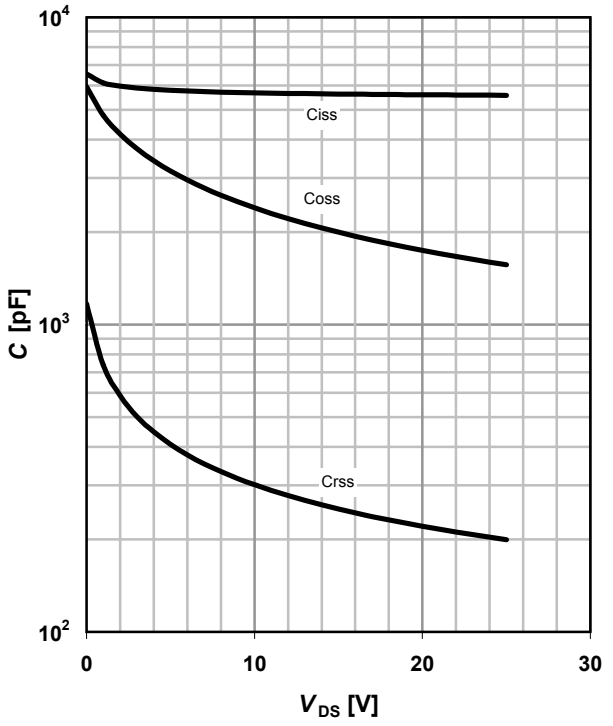
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

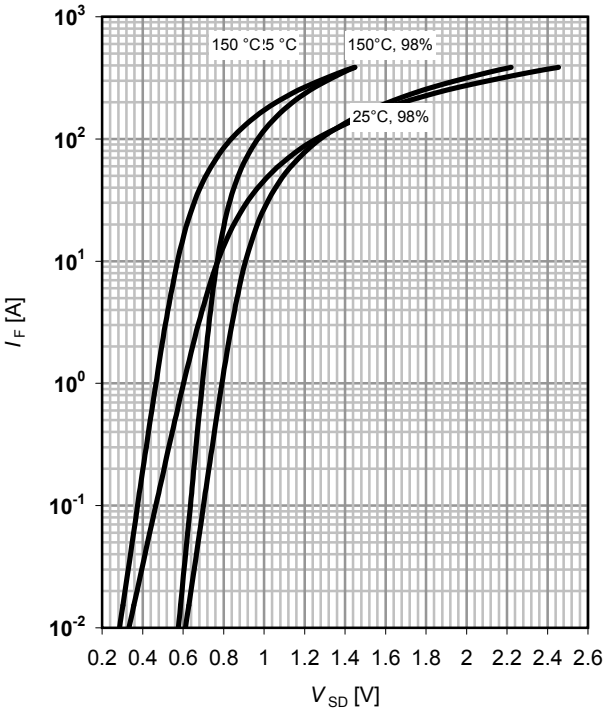
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

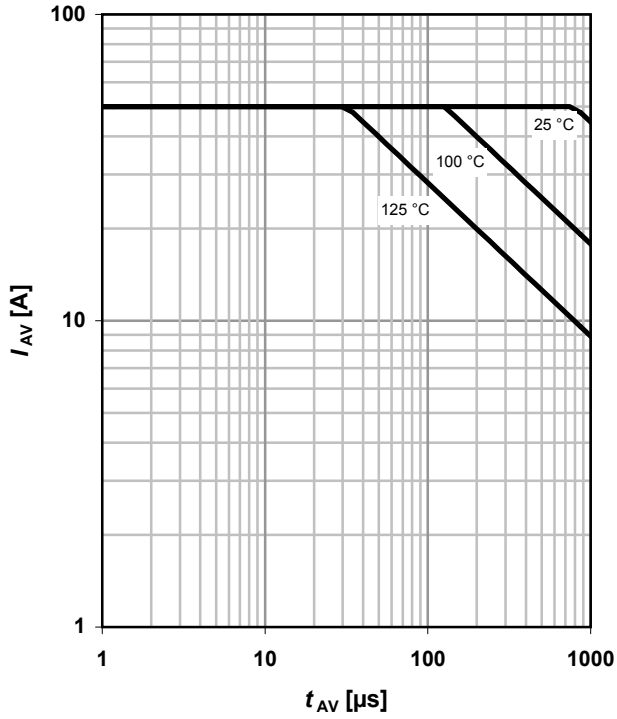
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

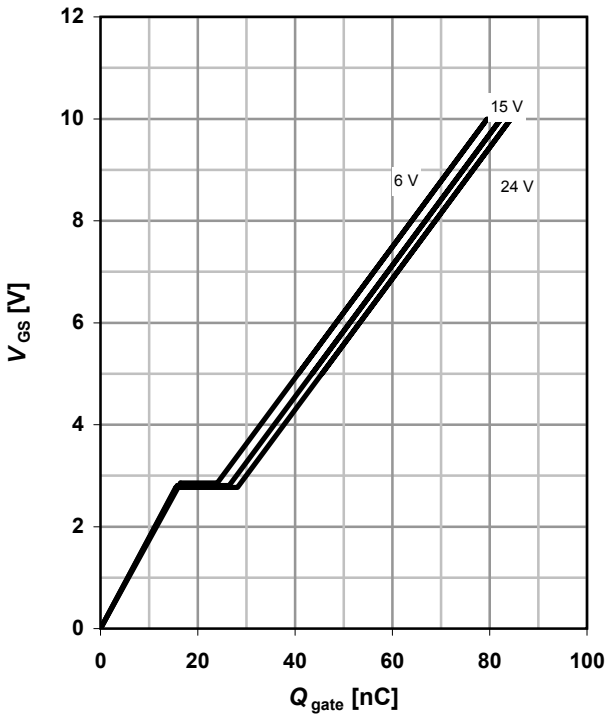
parameter: $T_{j(start)}$



14 Typ. gate charge

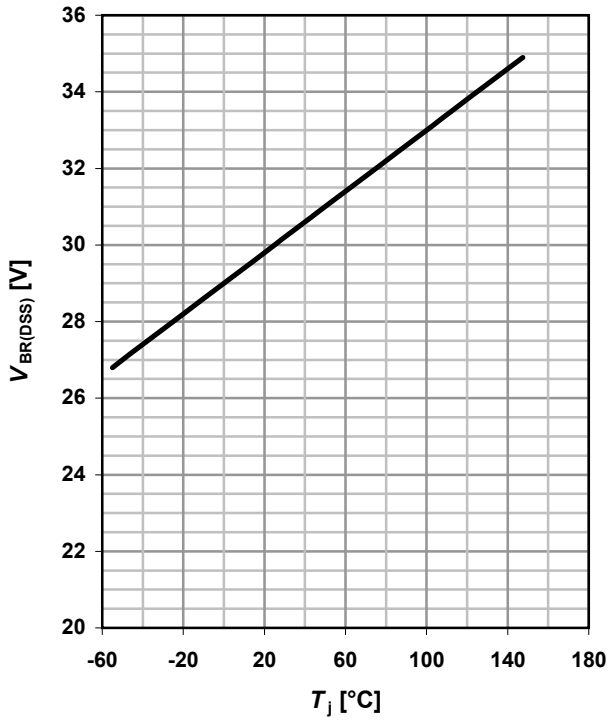
V_{GS}=f(Q_{gate}); I_D=25 A pulsed

parameter: V_{DD}

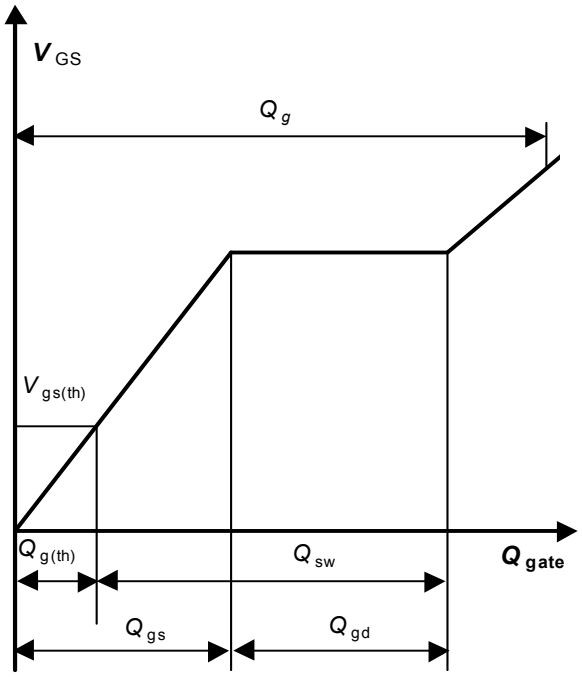


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

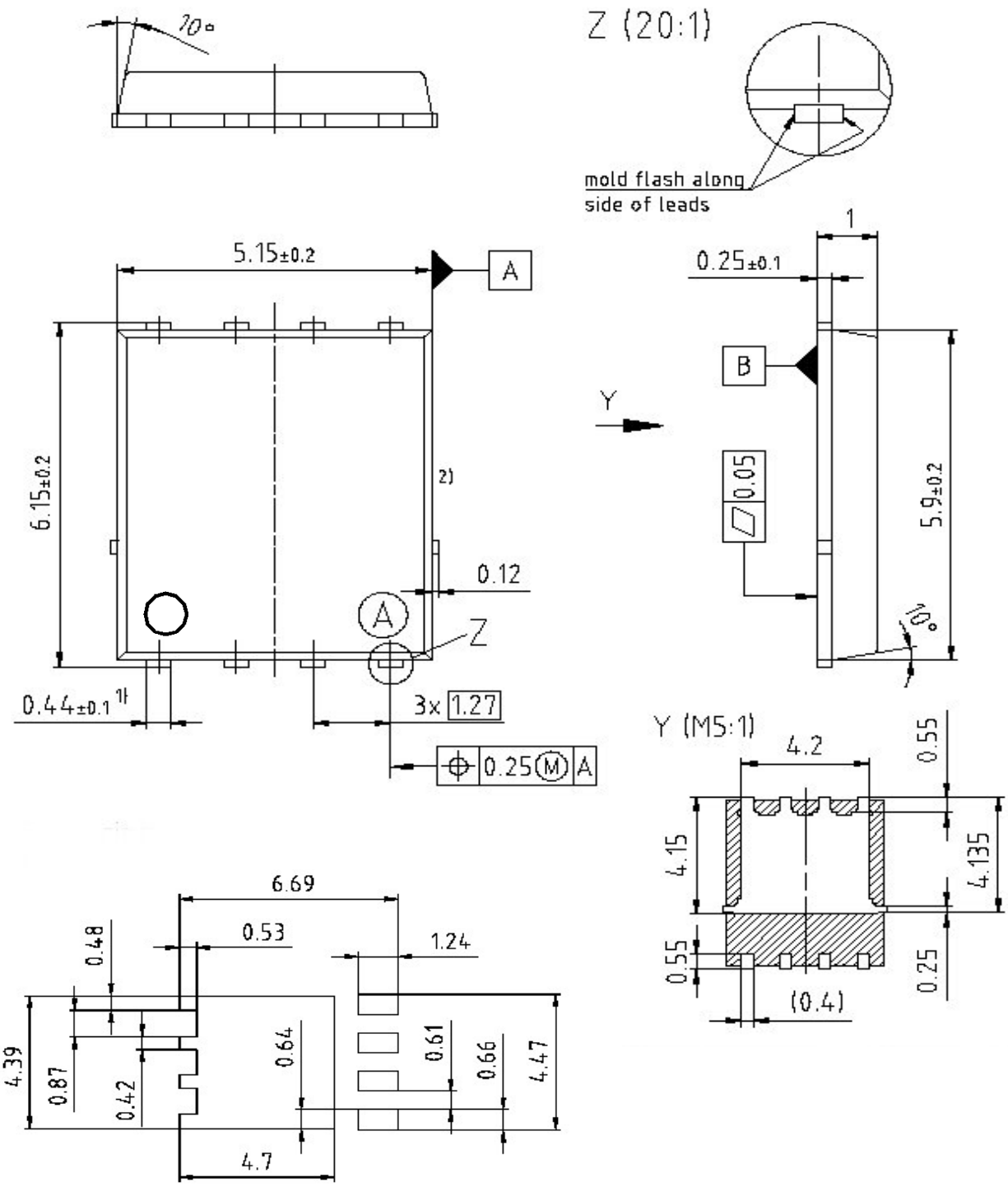


16 Gate charge waveforms



Package Outline

P-TDSON-8: Outline

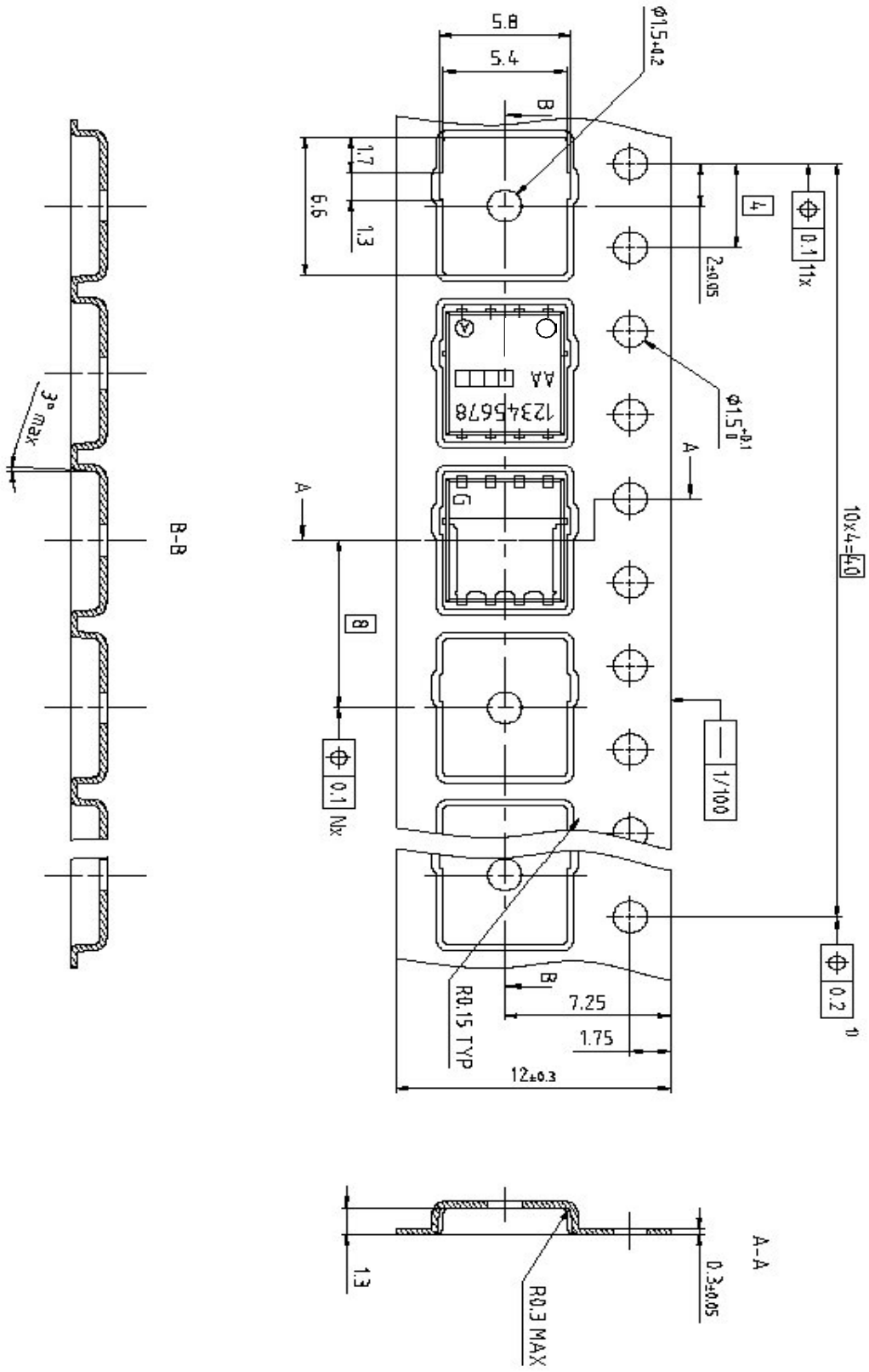


Drawing according to ISO 8015; general tolerances ±0.1 / 1°30'

Footprint
Dimensions in mm

Package Outline

P-TDSON-8: Tape



Dimensions in mm

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