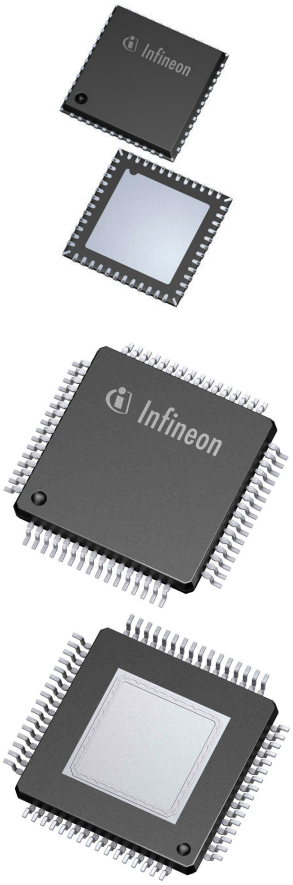
OPTIREG™ PMIC TLF35584

Functional Safety PMIC

AEC Qualified RoHS ISO26262 compliant

Features



- High efficient power management integrated circuit (PMIC)
- Serial step up and step down pre regulator for wide input voltage range from 3.0 to 40 V with full performance and low over all power loss
- Low drop post regulator 5.0 V/200 mA for communication supply (QCO)
- Low drop post regulator 5.0 V/600 mA (TLF35584QxVS1) or 3.3 V/600 mA (TLF35584QxVS2) for µC supply (QUC)
- Voltage reference 5.0 V ±1% for ADC supply, 150 mA current capability (QVR)
- Two trackers for sensor supply following voltage reference 150 mA current capability each (QT1 and QT2)
- Standby regulator 5.0 V/10 mA (TLF35584QxVS1) or 3.3 V/10 mA (TLF35584QxVS2) (QST)
- Provides enable, sync out signal and voltage monitoring for an optional external post regulator for core supply
- Independent voltage monitoring block and error pin monitoring
- Configurable window and functional watchdog
- Safe State Control with two safe state signals with programmable delay
- 16-bit SPI, interrupt and reset function
- PRO-SIL™ Features:
  - ISO 26262 compliant supporting up to ASIL-D
  - Safety Documentation (Safety Manual & Safety Analysis Summary Report)
- Green Product (RoHS compliant)

Potential applications

- Electric Power Steering
- Battery Management
- Inverter
- Transmission
- Engine Management
- Domain Control

Product validation

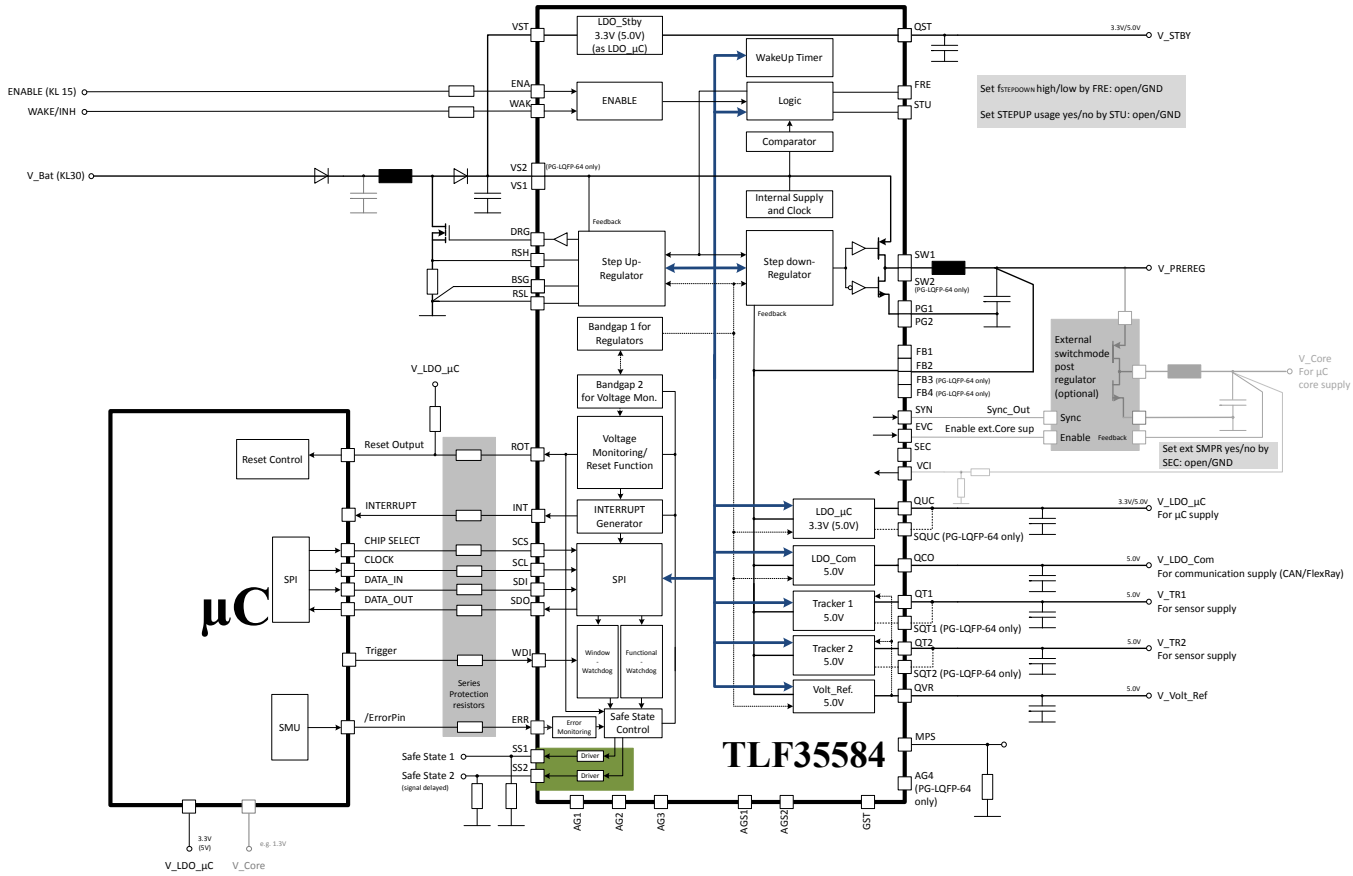
Qualified for Automotive Applications.
Product validation according to AEC-Q100/101.

Description

The OPTIREG™ PMIC TLF35584 is a high efficient Functional Safety PMIC (Power Management Integrated Circuit).

Type	Package
TLF35584QVVS1 (5.0 V Variant)	PG-VQFN-48
TLF35584QVVS2 (3.3 V Variant)	PG-VQFN-48
TLF35584QKVS1 (5.0 V Variant)	PG-LQFP-64
TLF35584QKVS2 (3.3 V Variant)	PG-LQFP-64

Application Example



Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact us for additional supportive documentation.
- For further information you may contact ***http://www.infineon.com/OPTIREG-PMIC***

Note: This figure is a very simplyfied example on an application circuit. The function must be verified in the real application.

1 Absolute maximum ratings

Table 1 Absolute maximum ratings[2)]

T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltages						
Boost driver ground	V_{BSG}	-0.3	–	0.3	V	–
Input standby LDO	V_{VST}	-0.3	–	40	V	3)4)
Input voltage pin 1 (pre regulator)	V_{VS1}	-0.3	–	40	V	–
Input voltage pin 2 (pre regulator)	V_{VS2}	-0.3	–	40	V	PG-LQFP-64 only
External step up power stage, gate	V_{DRG}	-0.3	–	40	V	–
External power stage, sense resistor high	V_{RSH}	-0.3	–	40	V	–
External power stage, sense resistor low	V_{RSL}	-0.3	–	6.0	V	–
Enable input	V_{ENA}	-0.3	–	40	V	–
Enable input	I_{ENA}	-5	–	–	mA	5)
Wake input	V_{WAK}	-0.3	–	40	V	–
Wake input	I_{WAK}	-5	–	–	mA	–
Reset output	V_{ROT}	-0.3	–	6.0	V	–
SPI chip select input	V_{SCS}	-0.3	–	6.0	V	–
SPI clock input	V_{SCL}	-0.3	–	6.0	V	–
SPI data in (MOSI) input	V_{SDI}	-0.3	–	6.0	V	–
SPI data out (MISO output)	V_{SDO}	-0.3	–	6.0	V	–
Interrupt output	V_{INT}	-0.3	–	6.0	V	–
Window watchdog trigger input	V_{WDI}	-0.3	–	6.0	V	–
Error pin input	V_{ERR}	-0.3	–	6.0	V	–
Safe state 1 output	V_{SS1}	-0.3	–	6.0	V	–
Safe state 2 output	V_{SS2}	-0.3	–	6.0	V	–
Output voltage reference LDO	V_{QVR}	-0.3	–	6.0	V	–
Output tracker 2	V_{QT2}	-1.0	–	40	V	–

2 Not subject to production test, specified by design.
3 Maximum rating is 60 V, if rise time from 0 to 60 V is longer than 10 ms
4 Maximum rating is 49 V, for an overall time of 10 s (in the range of 40 V to 49 V) during the lifetime of the product independent from the rise time.
5 Consider external series resistor for negative voltages < -0.3 V to ensure maximum rating of current

1 Absolute maximum ratings

Table 1 Absolute maximum ratings[2] (continued)

T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sense Pin for tracker 2	V_{SQT2}	-0.3	–	40	V	PG-LQFP-64 only
Output tracker 1	V_{QT1}	-1.0	–	40	V	–
Sense Pin for tracker 1	V_{SQT1}	-0.3	–	40	V	PG-LQFP-64 only
Output communication LDO	V_{QCO}	-0.3	–	6.0	V	–
Output microcontroller LDO	V_{QUC}	-0.3	–	6.0	V	–
Sense Pin for microcontroller LDO	V_{SQUC}	-0.3	–	6.0	V	PG-LQFP-64 only
External core voltage monitor input	V_{VCI}	-0.3	–	6.0	V	–
HW config: ext. core voltage monitor	V_{SEC}	-0.3	–	6.0	V	–
Synchronization output	V_{SYN}	-0.3	–	6.0	V	–
Enable output for ext. core supply	V_{EVC}	-0.3	–	6.0	V	–
Step down feedback input 4	V_{FB4}	-0.3	–	7.0	V	PG-LQFP-64 only
Step down feedback input 3	V_{FB3}	-0.3	–	7.0	V	PG-LQFP-64 only
Step down feedback input 2	V_{FB2}	-0.3	–	7.0	V	–
Step down feedback input 1	V_{FB1}	-0.3	–	7.0	V	–
Step down power ground 2	V_{PG2}	-0.3	–	0.3	V	–
Step down power ground 1	V_{PG1}	-0.3	–	0.3	V	–
Step down switching node 2	V_{SW2}	-0.3	–	40	V	PG-LQFP-64 only
Step down switching node 1	V_{SW1}	-0.3	–	40	V	–
HW config: step up pre regulator	V_{STU}	-0.3	–	6.0	V	–
HW config: step down frequency	V_{FRE}	-0.3	–	6.0	V	–
Output standby LDO	V_{QST}	-0.3	–	6.0	V	–
Input MPS	V_{MPS}	-0.3	–	6.0	V	–
Temperatures						
Junction temperature	T_j	-40	–	150	°C	–
Storage temperature	T_{stg}	-55	–	150	°C	–
ESD susceptibility						
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	HBM[6]

2 Not subject to production test, specified by design.

6 ESD susceptibility, HBM according to JEDEC HBM Human Body Model ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

1 Absolute maximum ratings

Table 1 Absolute maximum ratings[2] (continued)

T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	CDM[7]
ESD susceptibility (corner pins) to GND	$V_{ESD,Corner}$	-750	–	750	V	CDM

2 Not subject to production test, specified by design.
7 ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

2 Package information [8)]

8 Dimensions in mm

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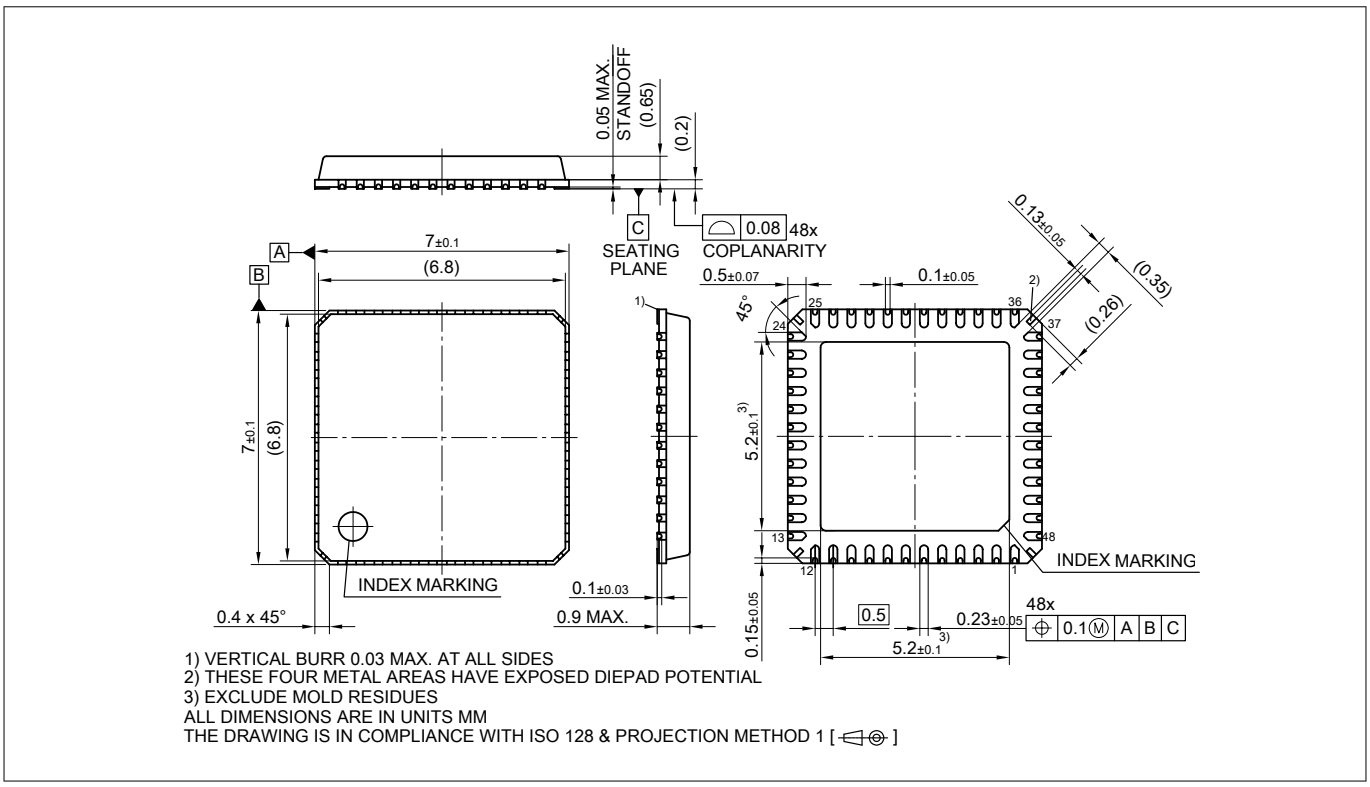
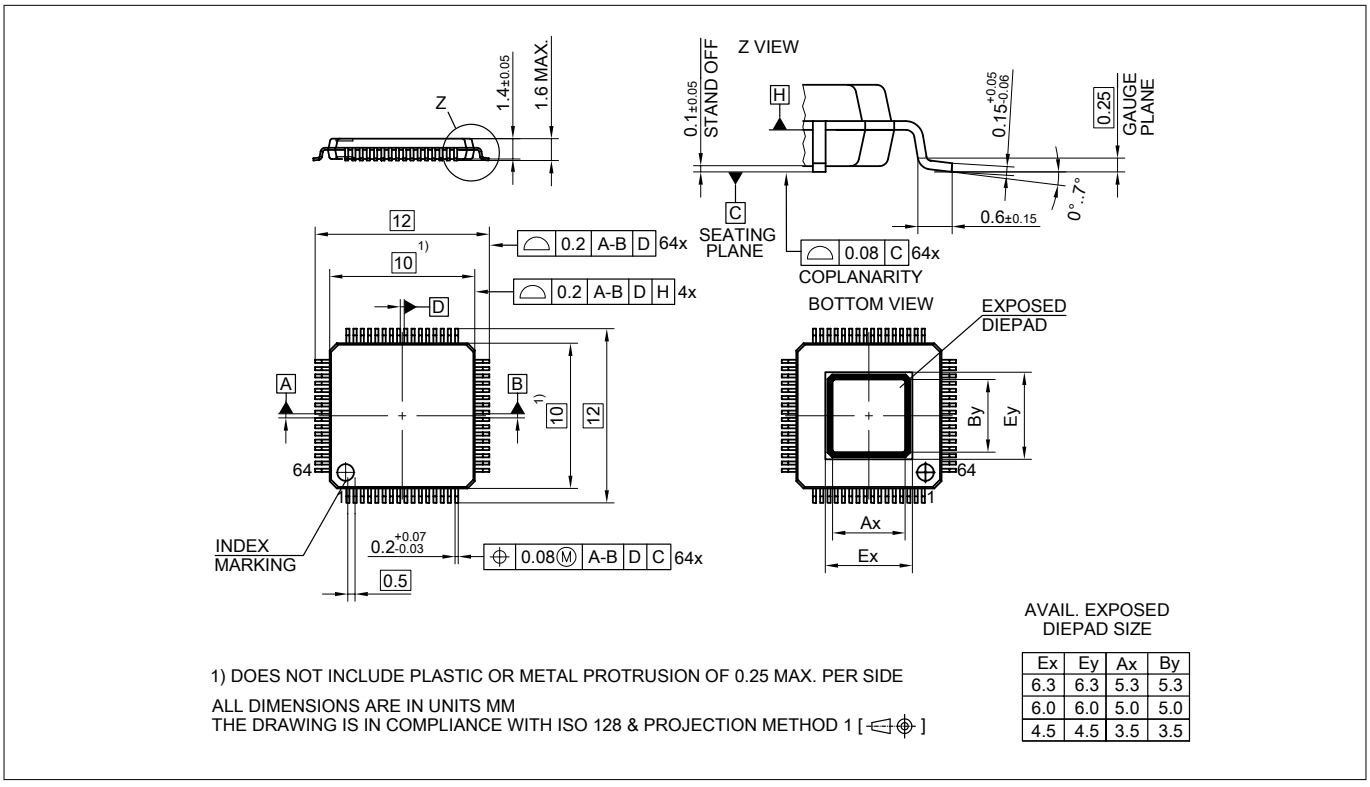


Figure 1 PG-VQFN-48 package outline



Ex	Ey	Ax	By
6.3	6.3	5.3	5.3
6.0	6.0	5.0	5.0
4.5	4.5	3.5	3.5

Figure 2 PG-LQFP-64 package outline

8 Dimensions in mm

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Edition 2019-03-25

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-jmv1546509847065

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