

# ESD5V5U5ULC

## Ultra-low capacitance ESD / transient / surge protection array

TVS (transient voltage suppressor)

5.5 V, 0.45 pF, RoHS compliant

### Feature list

- ESD/transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD):  $\pm 25$  kV (air/contact)
  - IEC61000-4-4 (EFT):  $\pm 2.5$  kV/ $\pm 50$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 6$  A (8/20  $\mu$ s)
- Maximum working voltage:  $V_{RWM} = 5.5$  V
- Extremely low capacitance:  $C_L = 0.45$  pF I/O to GND (typical)
- Very low dynamic resistance:  $R_{DYN} = 0.2 \Omega$  (typical) I/O to GND
- Very low reverse clamping voltage:  $V_{CL} = 9$  V (typical) at  $I_{PP} = 16$  A
- Protection of  $V_{BUS}$  with one line freely selectable



### Potential applications

- Protection of all I/O and  $V_{BUS}$  lines in dual USB2.0 ports
- 10/100/1000 Ethernet
- DVI, HDMI, FireWire

### Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

### Device information

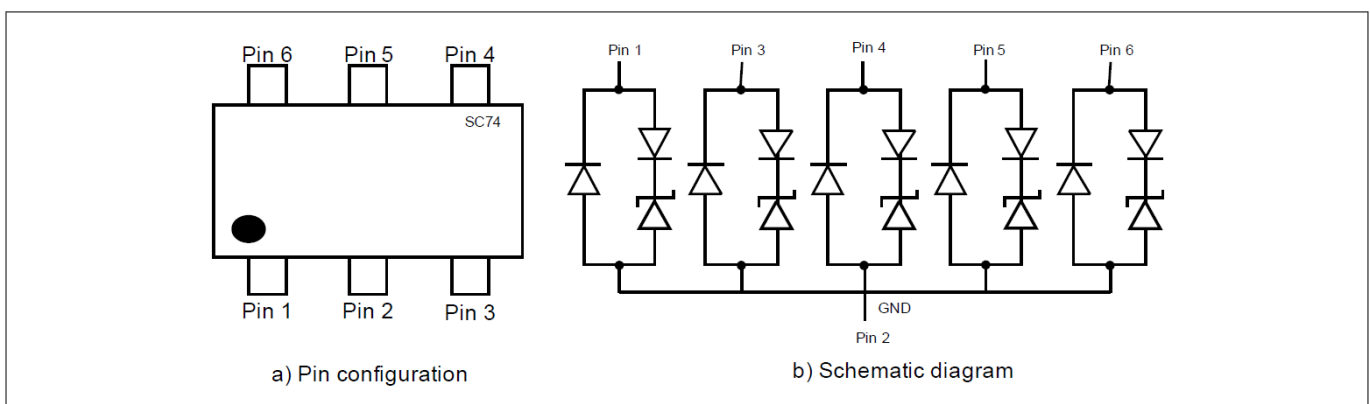


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD5V5U5ULC	PG-SC74-6-2	5 lines, uni-directional	20

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**Maximum ratings**

## 1 Maximum ratings

Note:  $T_A = 25\text{ °C}$ , unless otherwise specified.

**Table 2 Maximum ratings**

Parameter	Symbol	Values	Unit	Note or test condition
ESD contact discharge <sup>1)</sup>	$V_{ESD}$	$\pm 25$	kV	–
Peak pulse current <sup>2)</sup>	$I_{PP}$	$\pm 6$	A	$t_p = 8/20\ \mu\text{s}$
Operating temperature range	$T_{OP}$	-40 to 125	°C	–
Storage temperature	$T_{stg}$	-65 to 150	°C	–

**Attention:** *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.*

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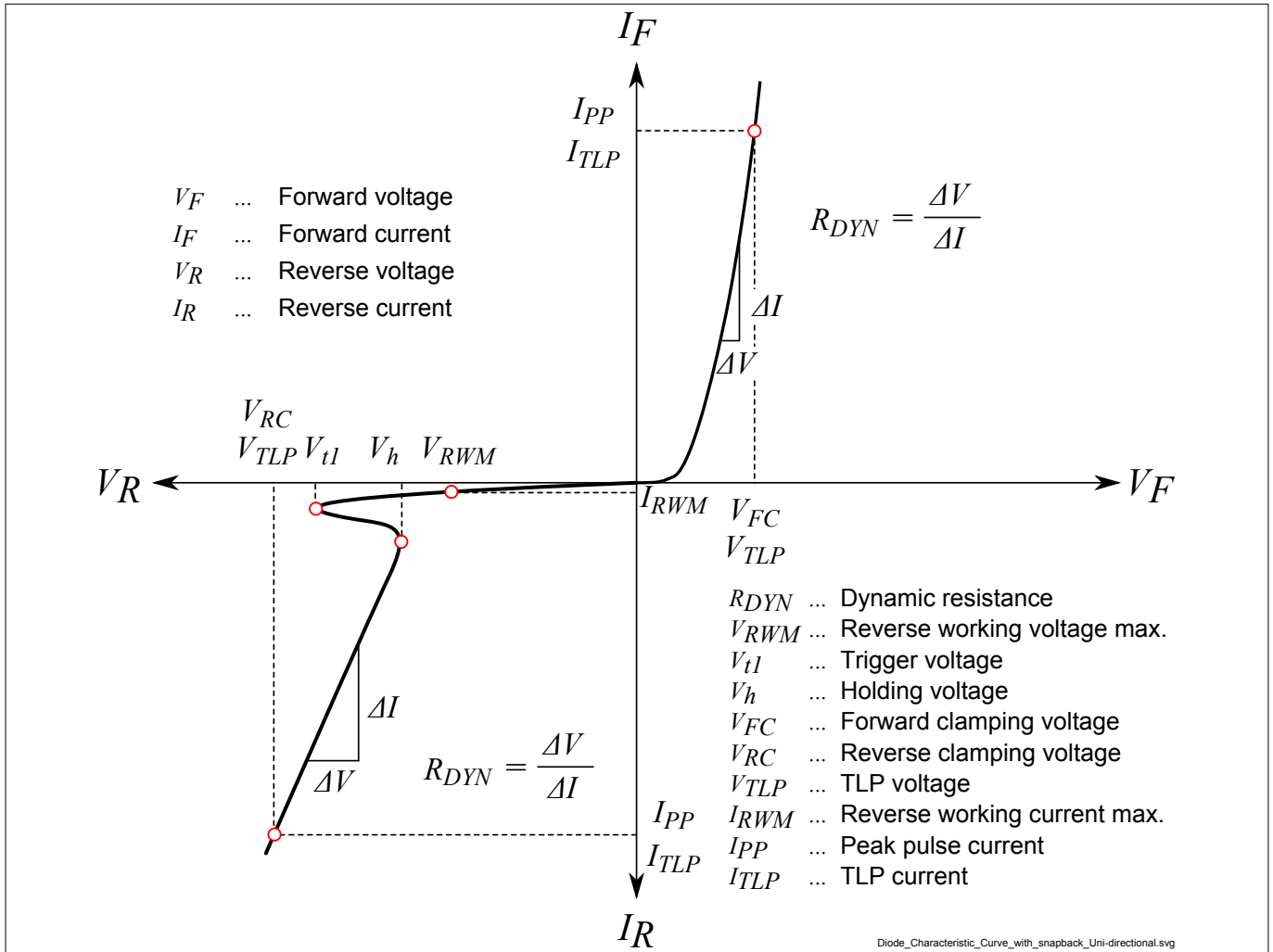
<sup>1</sup>  $V_{ESD}$  according to IEC61000-4-2

<sup>2</sup>  $I_{PP}$  according to IEC61000-4-5

**Electrical characteristics**

**2 Electrical characteristics**

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.



**Figure 2** Definitions of electrical characteristics

**Table 3** DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	-	-	5.5	V	I/O to GND
Reverse current	$I_R$	-	<1	100	nA	$V_R = 5.5\text{ V}$ , I/O to GND

**Electrical characteristics**

**Table 4 RF characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	–	0.45	1	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
		–	0.23	0.5		$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O
Line capacitance	$C_L$	–	0.25	–	pF	$V_R = 0\text{ V}$ , $f = 825\text{ MHz}$ , I/O to GND
		–	0.13	–		$V_R = 0\text{ V}$ , $f = 825\text{ MHz}$ , I/O to I/O
Capacitance variation between I/O and GND	$\Delta C_{i/o-GND}$	–	0.02	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to GND
Capacitance variation between I/O	$\Delta C_{i/o-i/o}$	–	0.01	–	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , I/O to I/O

**Table 5 ESD and surge characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Reverse clamping voltage <sup>1)</sup>	$V_{CL}$	–	9	–	V	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , I/O pin to GND
		–	12	–		$I_{PP} = 3\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , I/O pin to GND
Reverse clamping voltage <sup>2)</sup>	$V_{CL}$	–	8.9	–	V	$I_{TLP} = 16\text{ A}$ , $t_p = 100\text{ ns}$ , I/O pin to GND
		–	11.5	–		$I_{TLP} = 30\text{ A}$ , $t_p = 100\text{ ns}$ , I/O pin to GND
Forward clamping voltage <sup>1)</sup>	$V_{FC}$	–	1.75	–	V	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , GND pin to I/O
		–	2.5	–		$I_{PP} = 3\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , GND pin to I/O
Forward clamping voltage <sup>2)</sup>	$V_{FC}$	–	5.4	–	V	$I_{TLP} = 16\text{ A}$ , $t_p = 100\text{ ns}$ , GND pin to I/O
		–	9.2	–		$I_{TLP} = 30\text{ A}$ , $t_p = 100\text{ ns}$ , GND pin to I/O
Dynamic resistance <sup>2)</sup>	$R_{DYN}$	–	0.2	–	$\Omega$	I/O to GND
Dynamic resistance <sup>2)</sup>	$R_{DYN}$	–	0.3	–	$\Omega$	GND to I/O

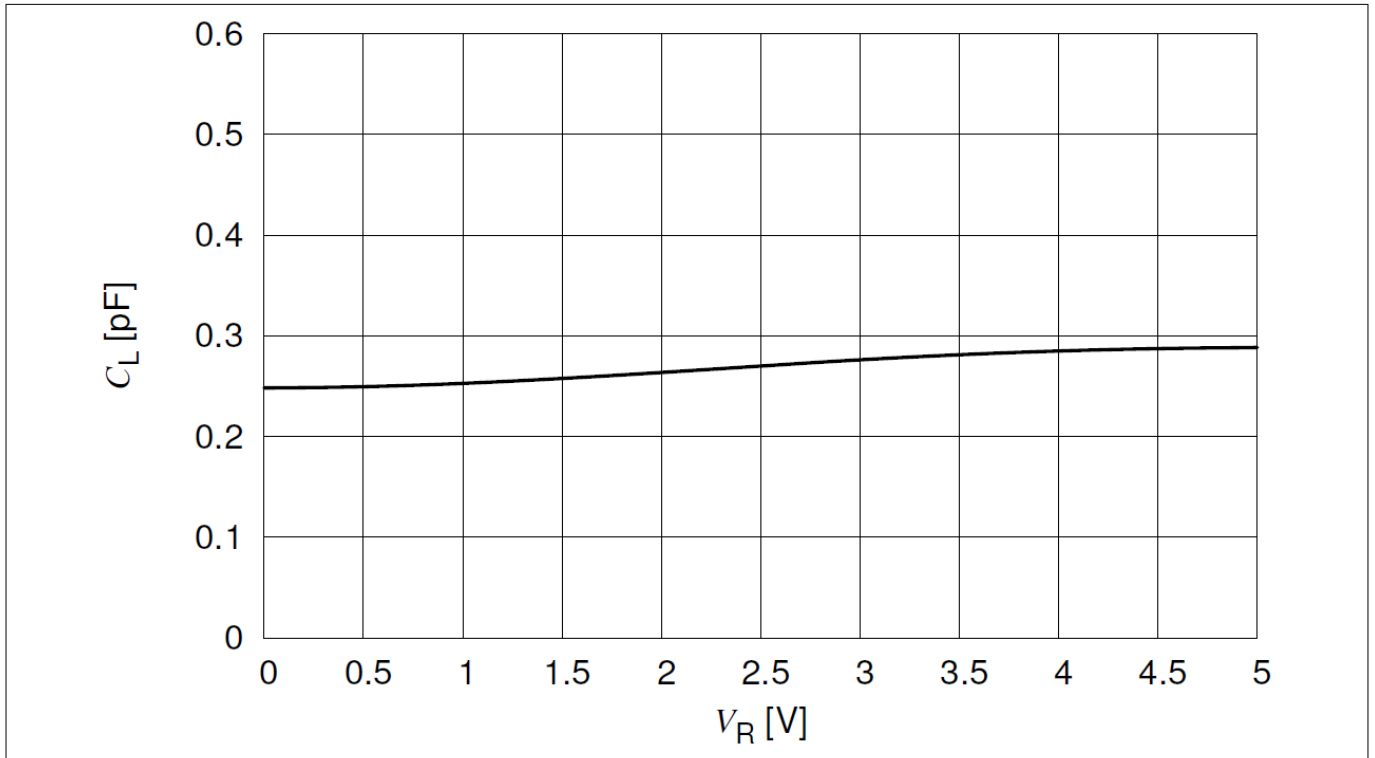
<sup>1)</sup>  $I_{PP}$  according to IEC61000-4-5

<sup>2)</sup> Please refer to application note AN210, TLP parameters:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10\text{ A}$  and  $I_{PP2} = 40\text{ A}$ .

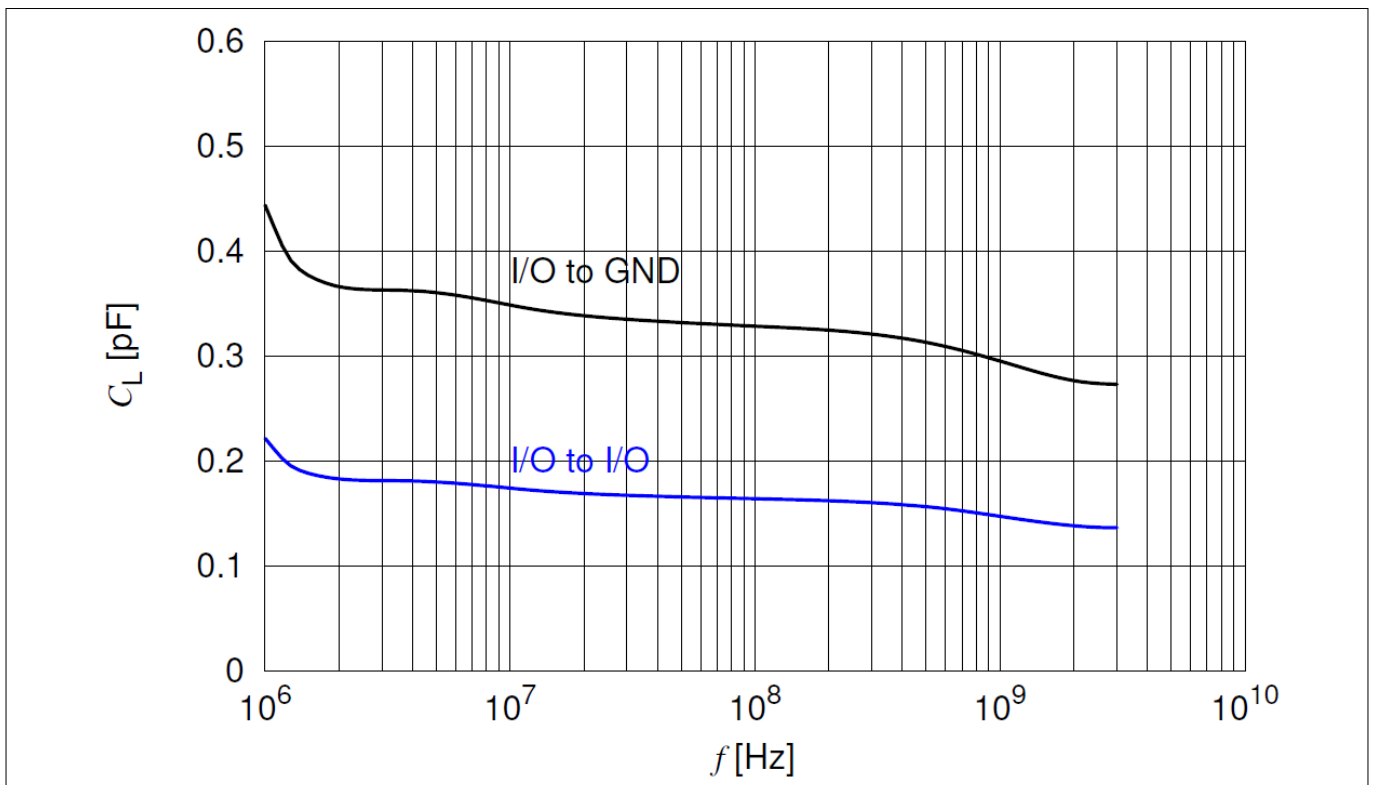
Typical characteristic diagrams

### 3 Typical characteristic diagrams

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.



**Figure 3** Line capacitance  $C_L = f(V_R)$  at  $f = 825\text{ MHz}$



**Figure 4** Line capacitance  $C_L = f(f)$ ,  $V_R = 0\text{ V}$

Typical characteristic diagrams

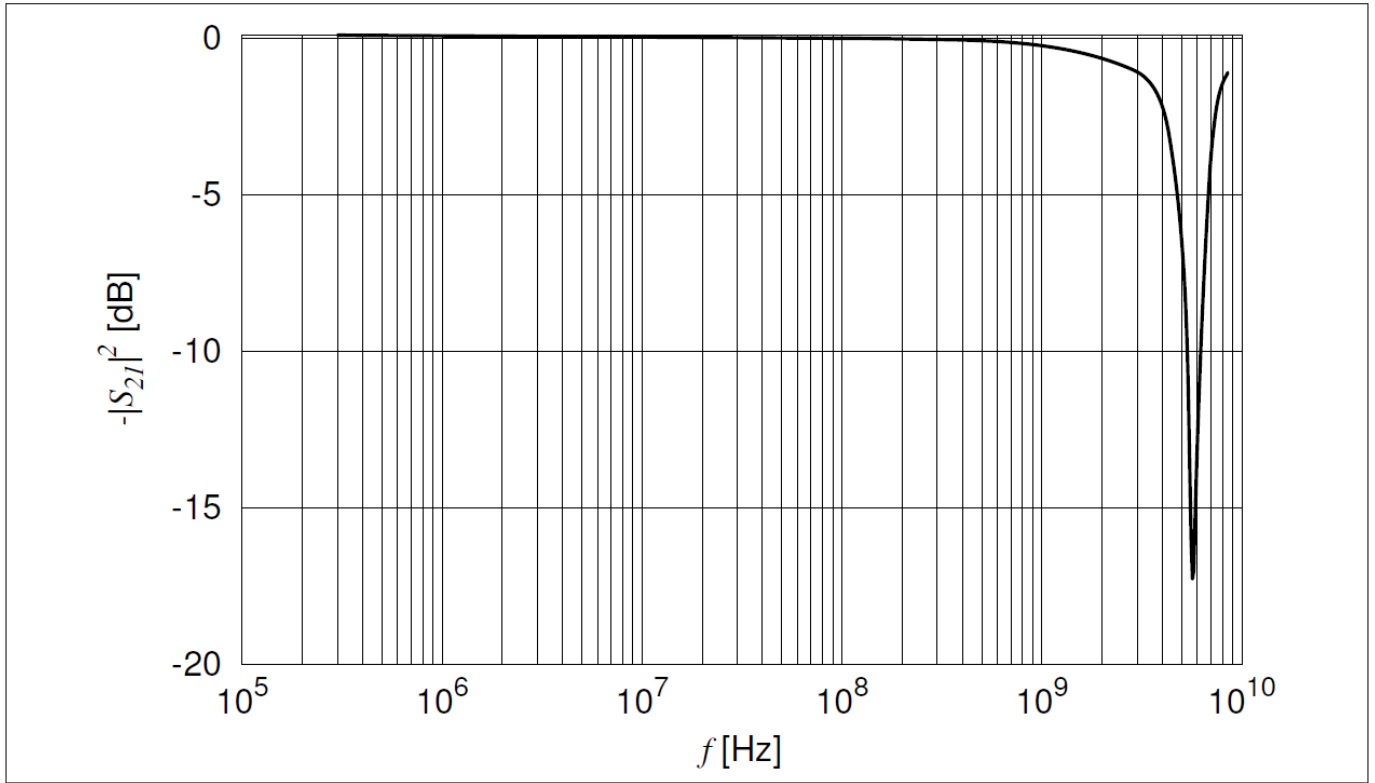


Figure 5 Insertion loss  $I_L = f(f)$ ,  $V_R = 0$  V

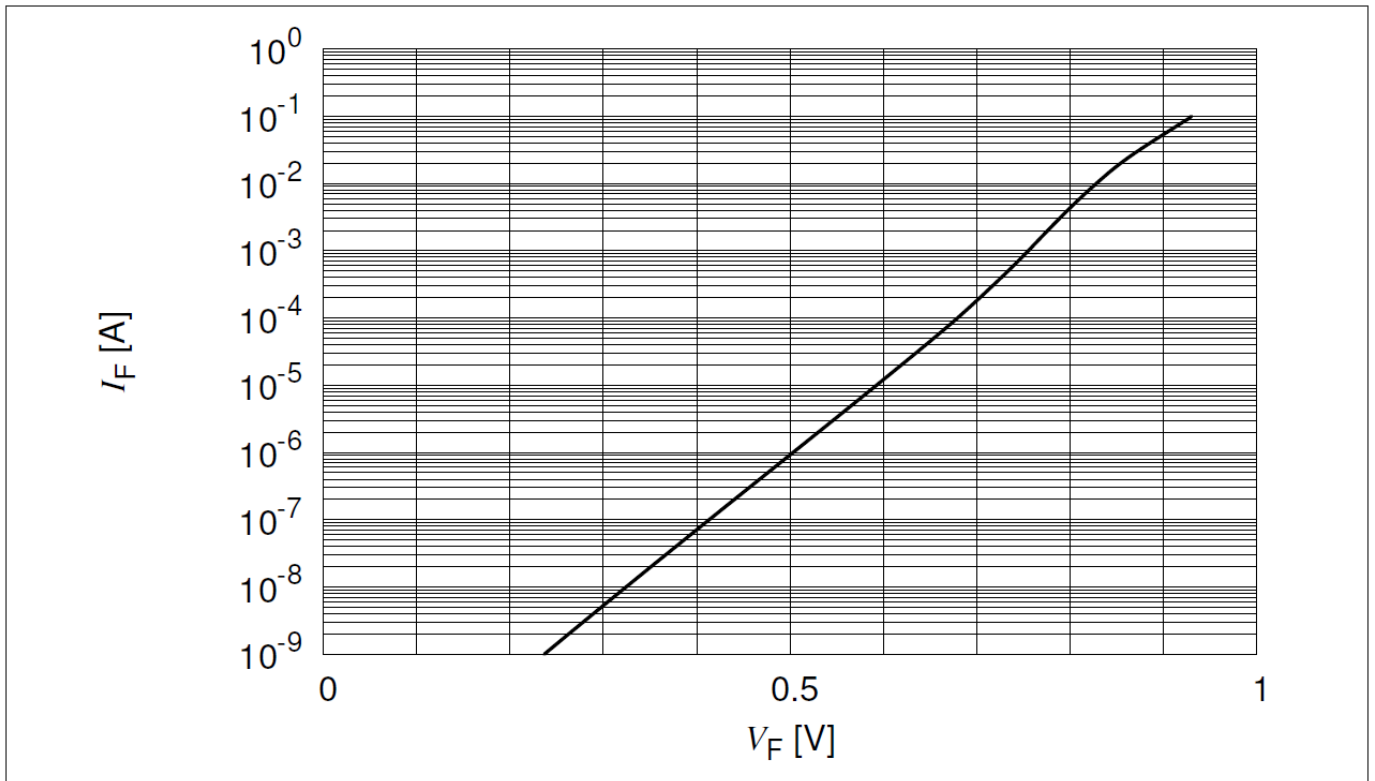


Figure 6 Forward characteristic,  $I_F = f(V_F)$ , current forced

Typical characteristic diagrams

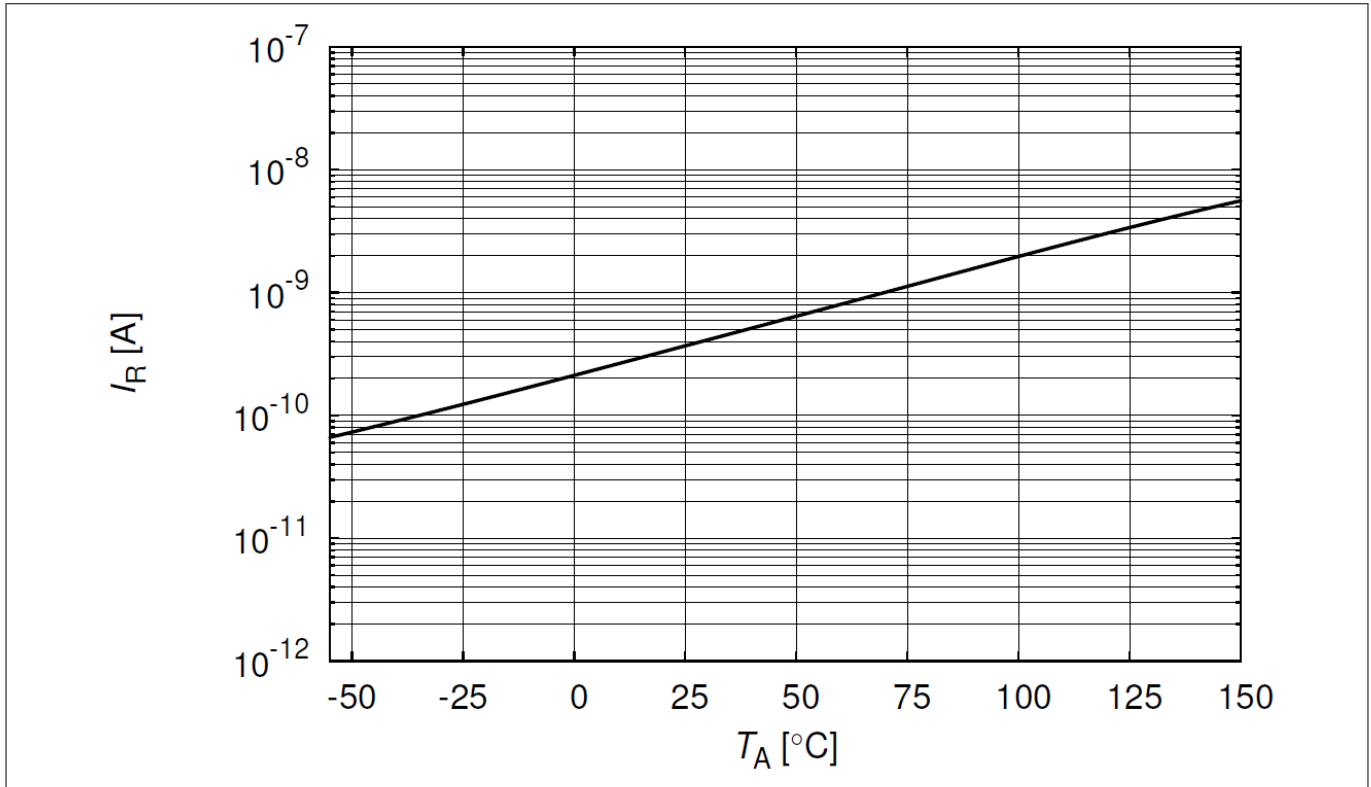


Figure 7 Reverse current  $I_R = f(T_A)$ ,  $V_R = 5.5$  V (typical)

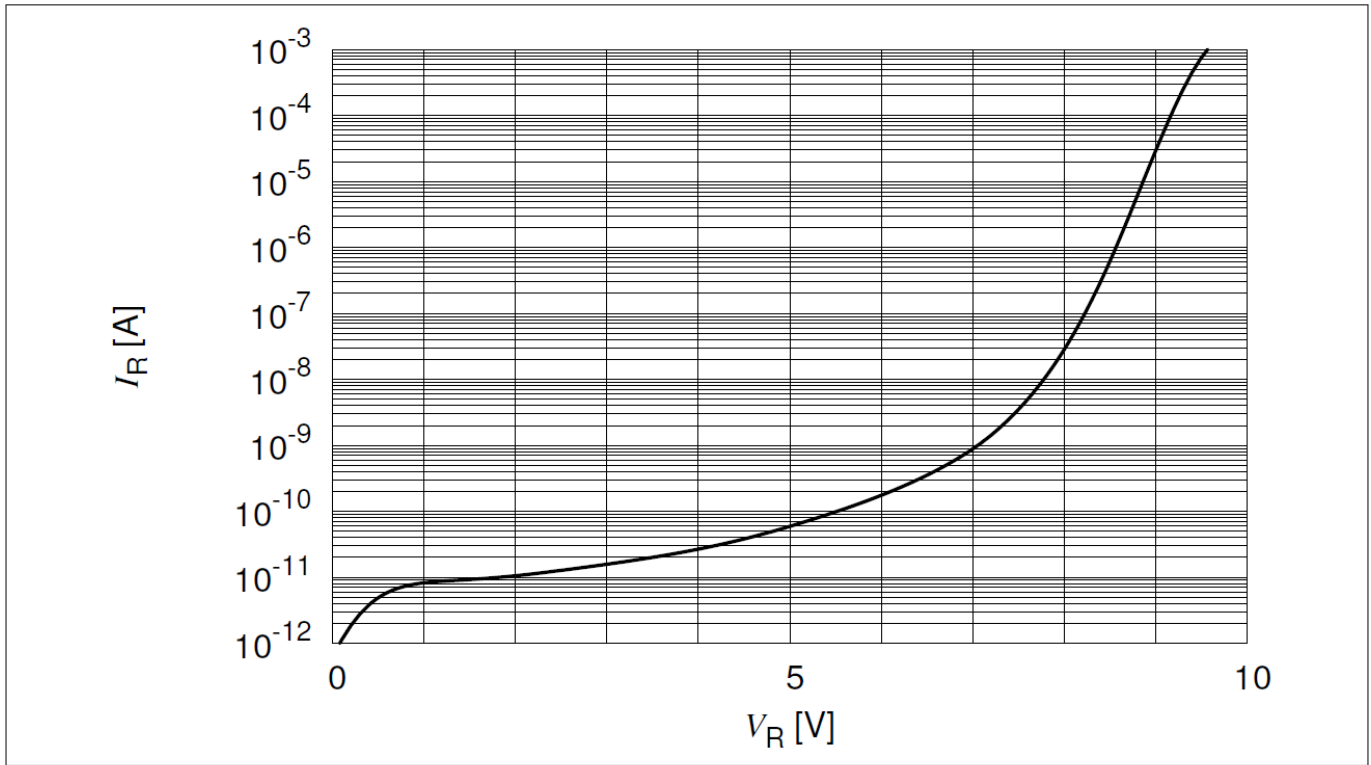
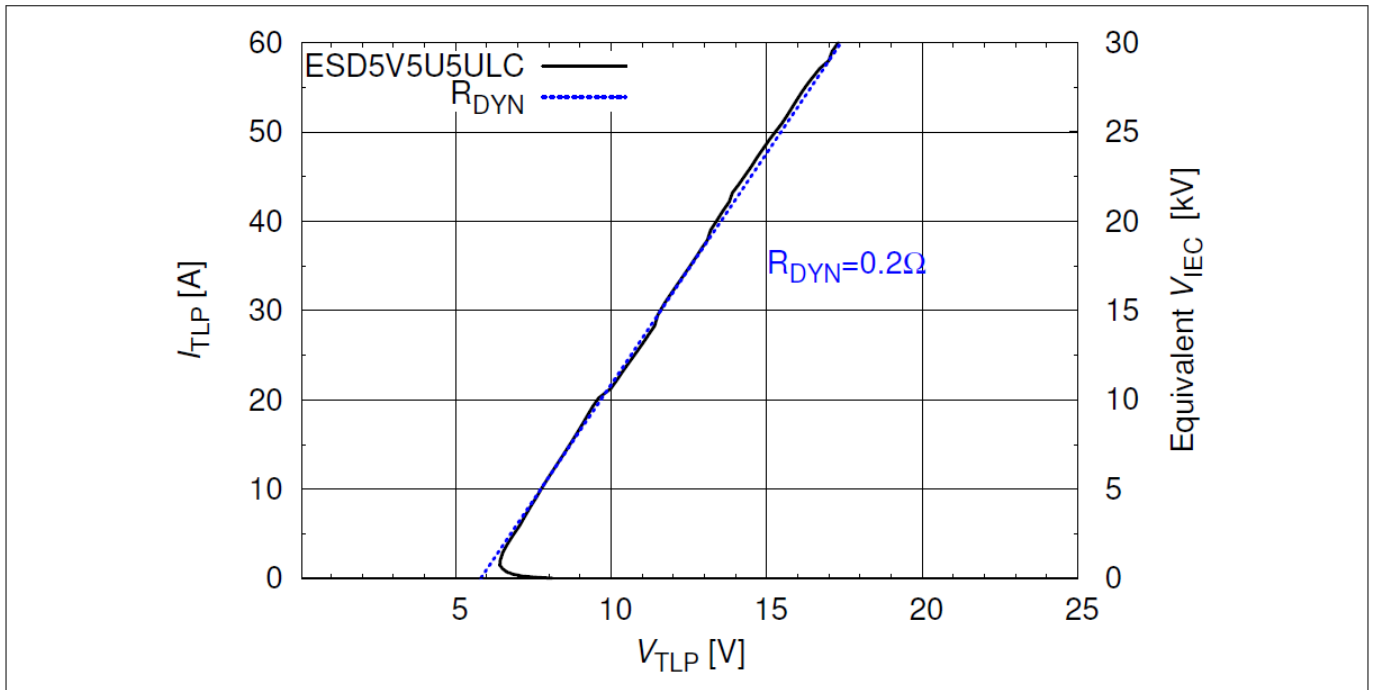


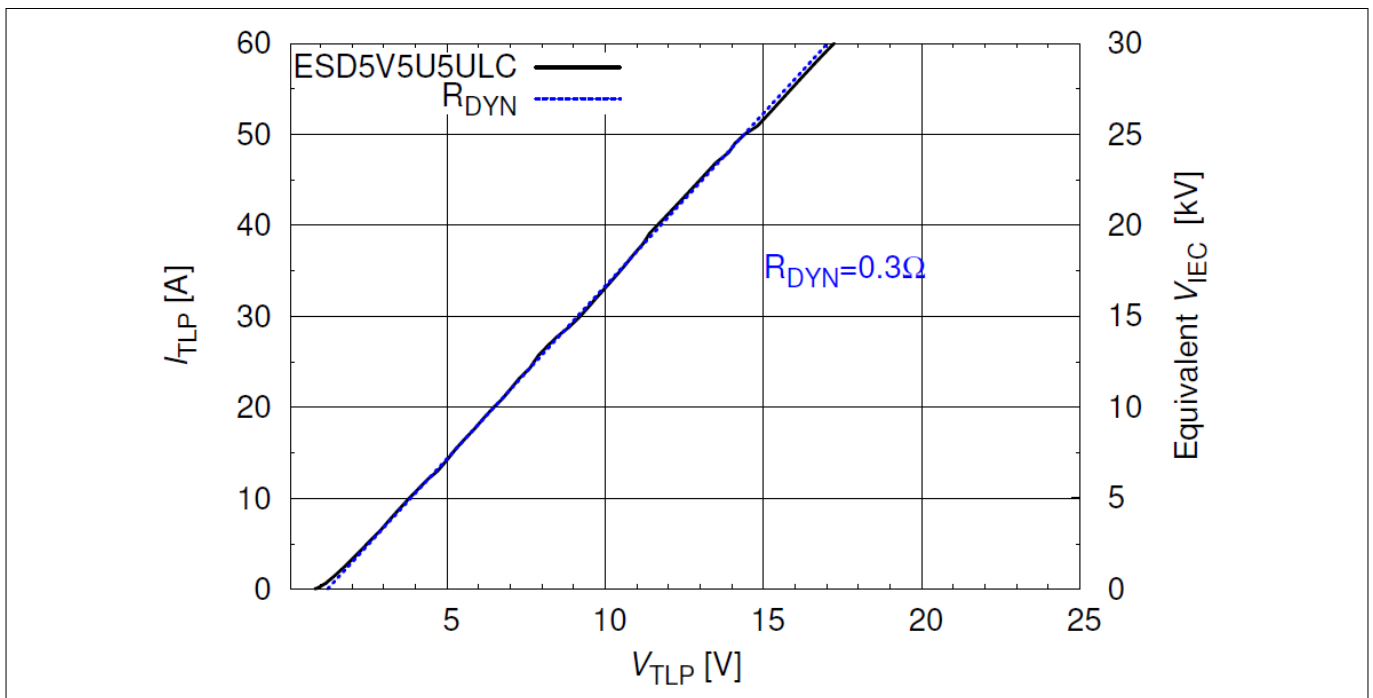
Figure 8 Reverse characteristic,  $I_R = f(V_R)$ , voltage forced



**Typical characteristic diagrams**



**Figure 9** TLP characteristic I/O to GND <sup>1)</sup> [1]



**Figure 10** TLP characteristic GND to I/O <sup>1)</sup> [1]

<sup>1</sup> TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10 \text{ A}$  and  $I_{PP2} = 40 \text{ A}$ . The equivalent stress level  $V_{IEC}$  according IEC61000-4-2 ( $R = 330 \Omega$ ,  $C = 150 \text{ pF}$ ) is calculated at the broad peak of the IEC waveform at  $t = 30 \text{ ns}$  with  $2 \text{ A/kV}$ .

Application information

4 Application information

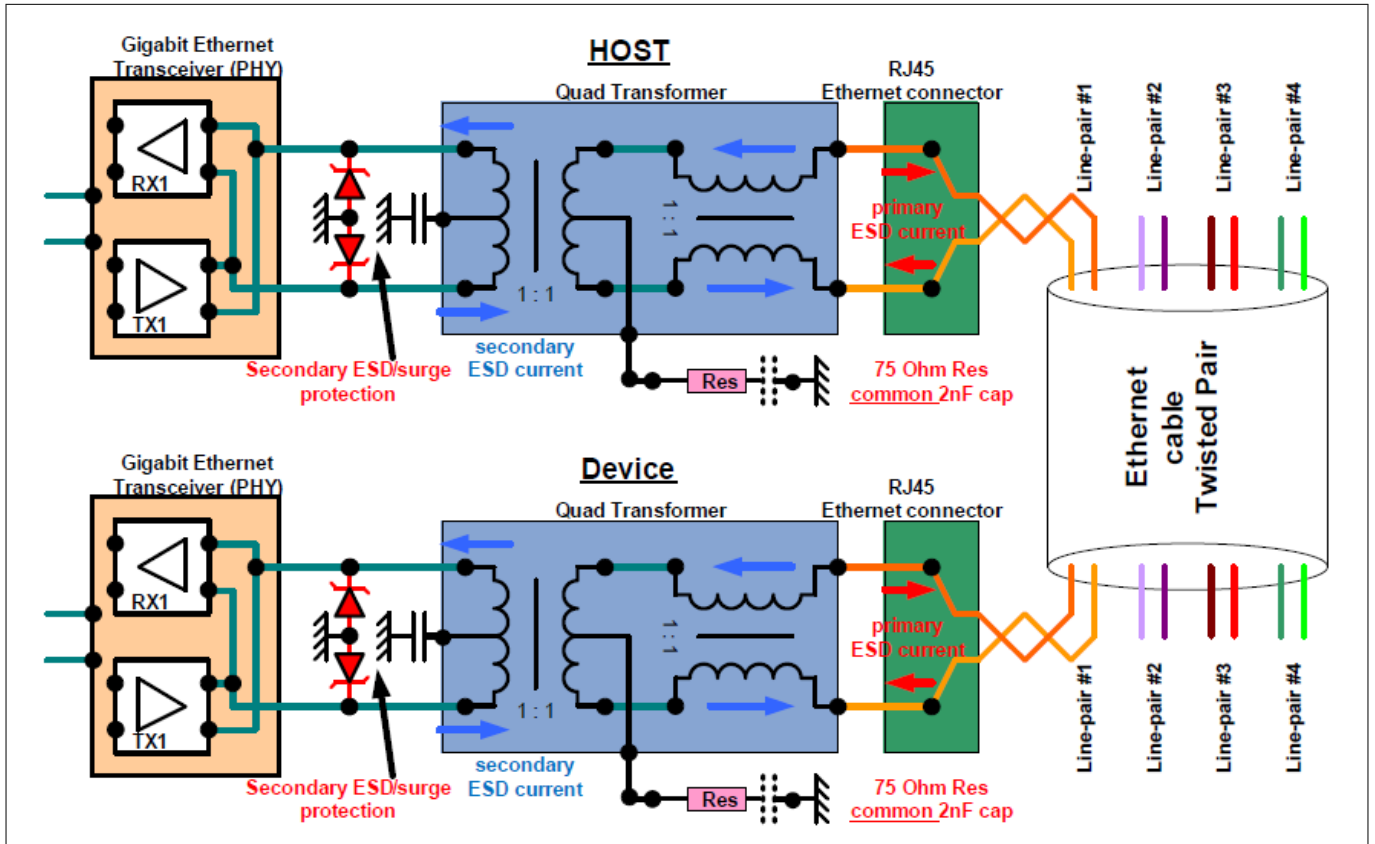


Figure 11 Ethernet

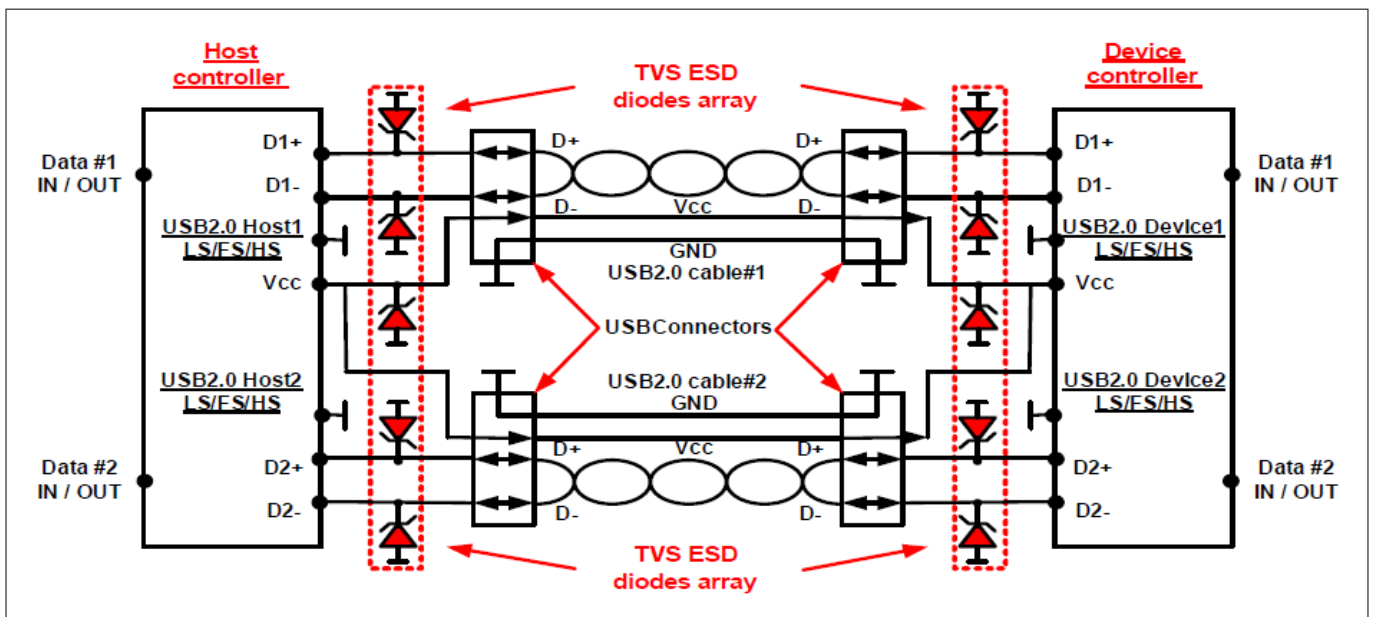


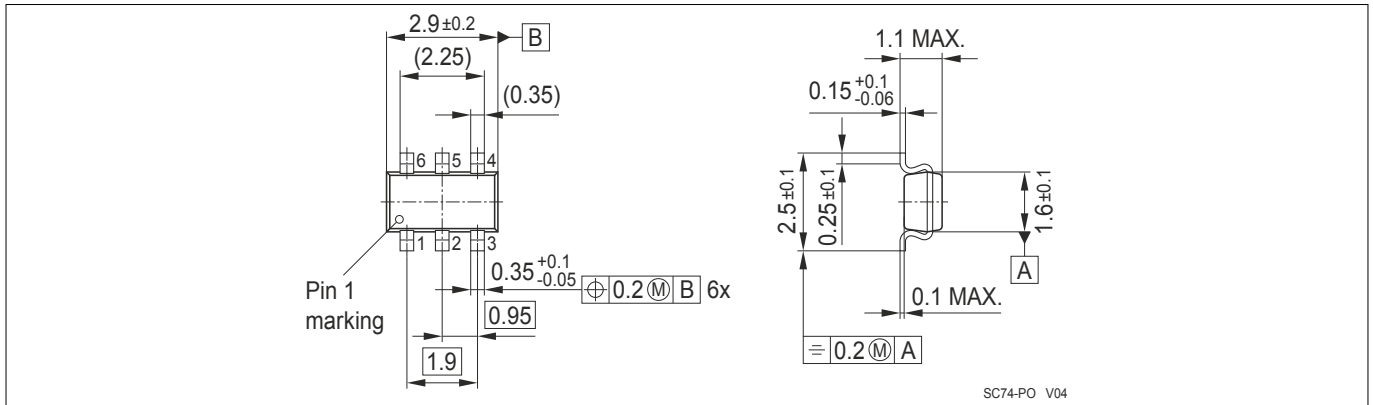
Figure 12 USB2.0

**Package information**

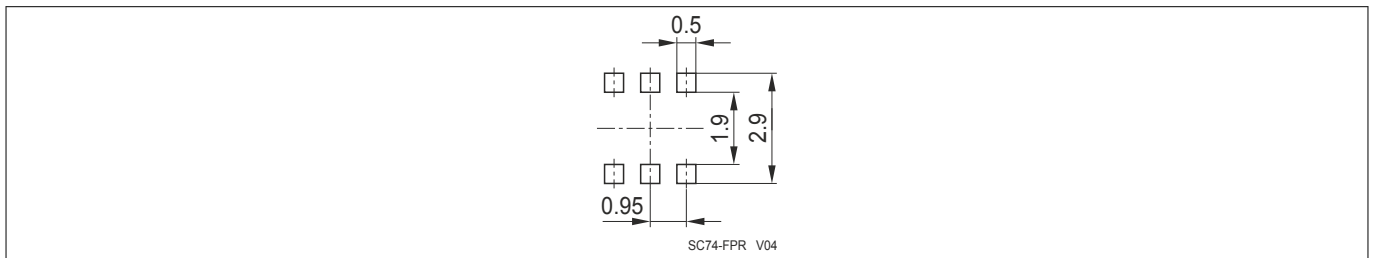
**5 Package information**

Note: Dimensions in mm.

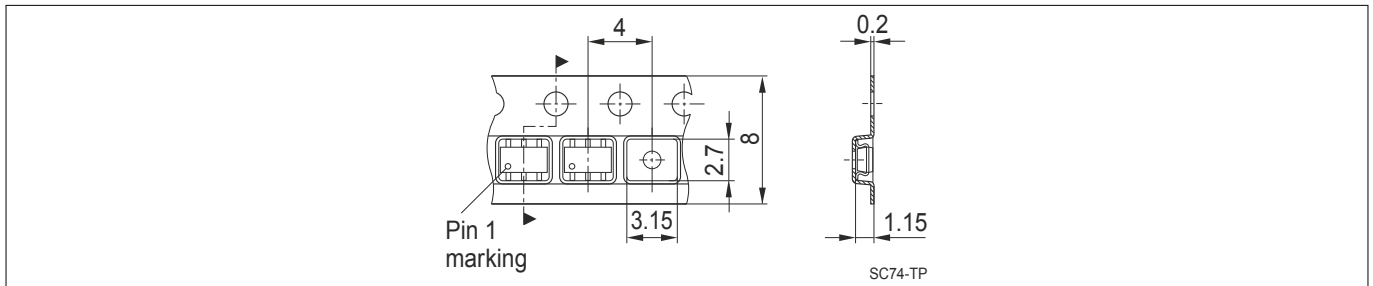
**5.1 PG-SC74-6-2 package**



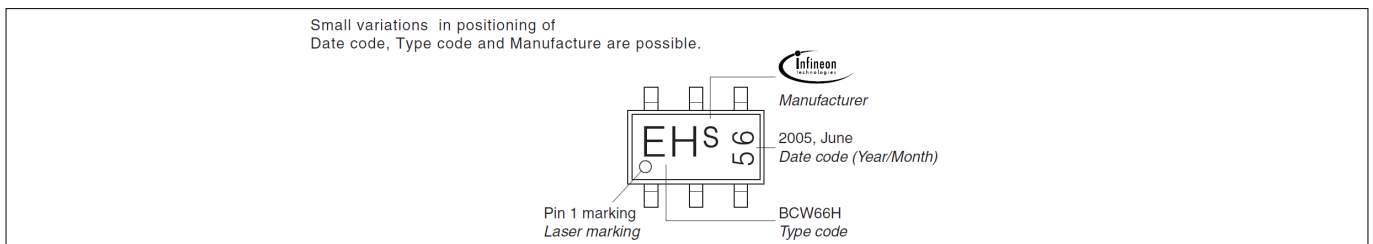
**Figure 13 PG-SC74-6-2 package overview**



**Figure 14 PG-SC74-6-2 footprint**



**Figure 15 PG-SC74-6-2 packing**



**Figure 16 PG-SC74-6-2 marking example (see [Device information](#))**

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References

## 6 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD protection design at system level using VF-TLP characterization methodology

## Revision history

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**Revision history: Rev. 1.4. 2016-04-21**

Page or Item	Subjects (major changes since previous revision)
Revision 1.5, 2018-06-12	
All	Data sheet layout changed, references updated, ordering information scheme deleted

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