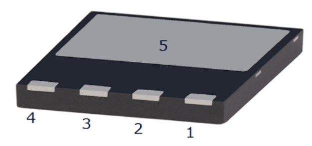
MOSFET

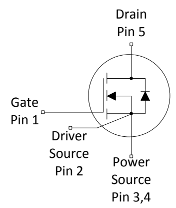
650V CoolMOS™ CFD2 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.

ThinPAK 8x8



ThinPAK
ThinPAK is a a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm² (vs. 150mm² for the D²PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D²PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.



Features

• Reduced board space consumption
• Increased power density
• Short commutation loop
• Smooth switching waveform
• Ultra-fast body diode
• Very high commutation ruggedness
• Extremely low losses due to very low FOM Rdson*Qg and Eoss
• Easy to use/drive
• Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
• Pb-free plating, Halogen free mold compound

Potential applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{ds} @ T_{jmax}	700	V
$R_{DS(on),max}$	0.165	Ω
$Q_{g,typ}$	86	nC
$I_{D,pulse}$	67	A
E_{oss} @ 400V	6.8	µJ
Body diode di_F/dt	900	A/µs
Q_{rr}	0.7	µC
t_r	140	ns
I_{rrm}	8.8	A

Type / Ordering Code	Package	Marking	Related Links
IPL65R165CFD	PG-VSON-4	65F6165	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	21.3 13.5	A	T_C = 25°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	67	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	614	mJ	I_D =4.3 A; V_{DD} = 50 V
Avalanche energy, repetitive	E_{AR}	-	-	0.93	mJ	I_D =4.3 A; V_{DD} = 50 V
Avalanche current, repetitive	I_{AR}	-	-	4.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS} =0...400 V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	195	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	21.3	A	T_C=25 °C
Diode pulse current[2]	$I_{S,pulse}$	-	-	67	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt	-	-	50	V/ns	V_{DS} =0...400 V, I_{SD}<= I_D, T_j=25 °C see table 8
Maximum diode commutation speed	di_F/dt	-	-	900	A/µs	V_{DS} =0...400 V, I_{SD}<= I_D, T_j=25 °C see table 8

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.64	°C/W	-
Thermal resistance, junction - ambient[4] 4)	R_{thJA}	- -	- -	62 45	°C/W	SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL2a

1) Limited by $T_{j\,max}$
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch with identical R_G
4) Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air steam cooling.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=0.9 mA
Zero gate voltage drain current	I_{DSS}	- -	- 300	1 -	µA	V_{DS}=650 V, V_{GS}=0 V, T_j=25 °C V_{DS}=650 V, V_{GS}=0 V, T_j=150 °C
Gate-source leakage curent	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.149 0.386	0.165 -	Ω	V_{GS}=10 V, I_D=9.3A, T_j=25 °C V_{GS}=10 V, I_D=9.3 A, T_j=150 °C
Gate resistance	R_G	-	1.5	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2340	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	110	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	90	-	pF	V_{GS}=0 V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	420	-	pF	I_D=constant, V_{GS}=0 V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	12.4	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=14 A, R_G=1.8Ω; see table 9
Rise time	t_r	-	7.6	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=14 A, R_G=1.8Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	52.8	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=14 A, R_G=1.8Ω; see table 9
Fall time	t_f	-	5.6	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=14 A, R_G=1.8Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	15	-	nC	V_{DD}=480 V, I_D=14 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	47	-	nC	V_{DD}=480 V, I_D=14 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	86	-	nC	V_{DD}=480 V, I_D=14 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	V_{DD}=480 V, I_D=14 A, V_{GS}=0 to 10 V

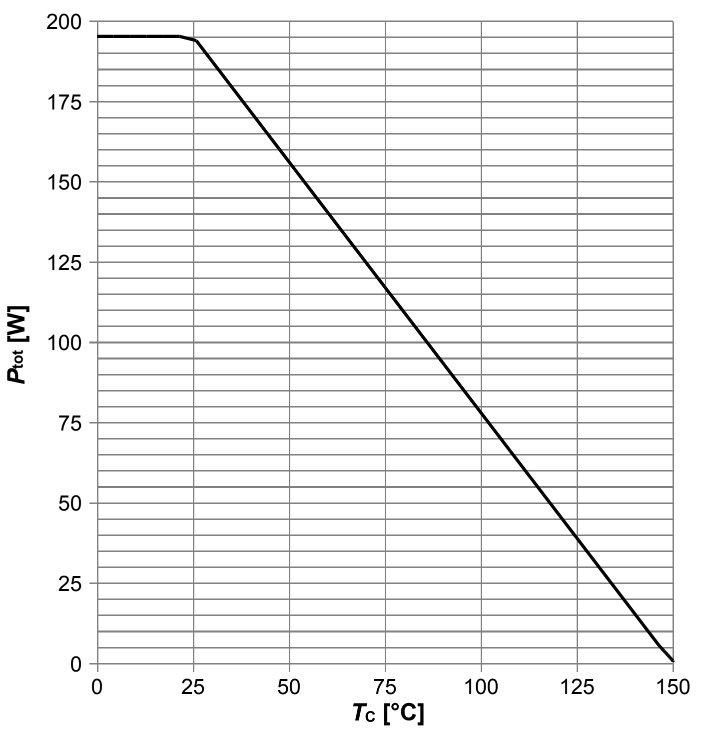
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0 V, I_F=14 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	140	-	ns	V_R=400 V, I_F=14A di_F/dt=100 A/µs see table 8
Reverse recovery charge	Q_{rr}	-	0.7	-	µC	V_R=400 V, I_F=14A di_F/dt=100 A/µs see table 8
Peak reverse recovery current	I_{rrm}	-	8.8	-	A	V_R=400 V, I_F=14A di_F/dt=100 A/µs see table 8

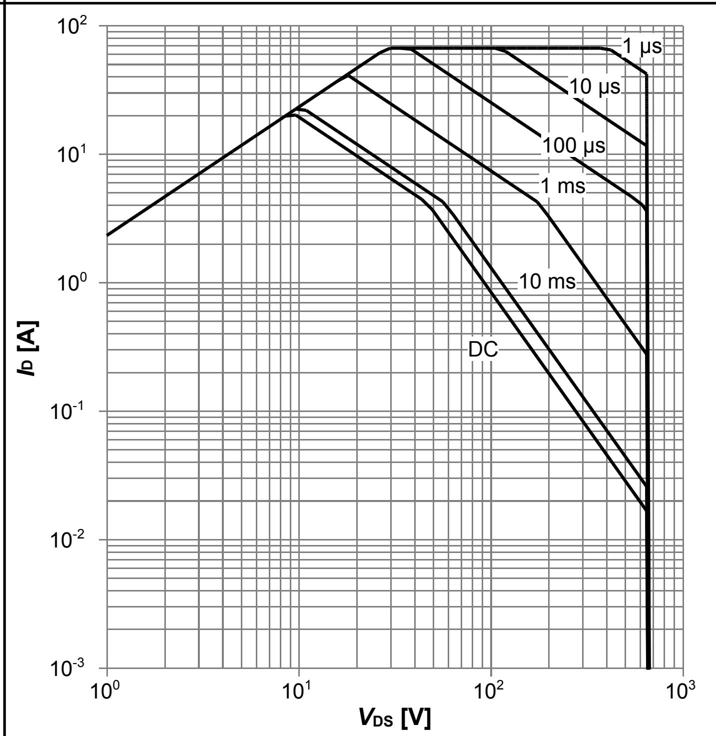
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



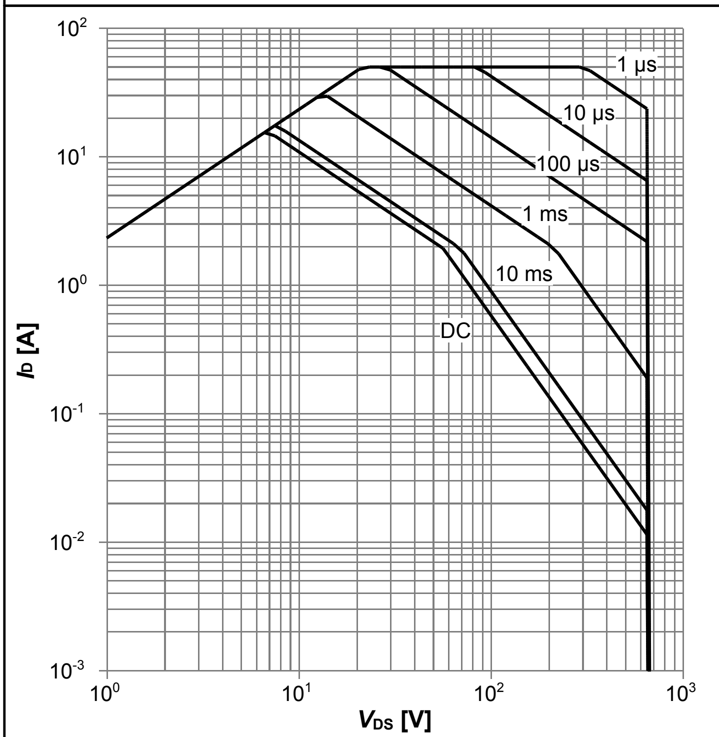
P_{tot}=f(T_C)

Diagram 2: Safe operating area



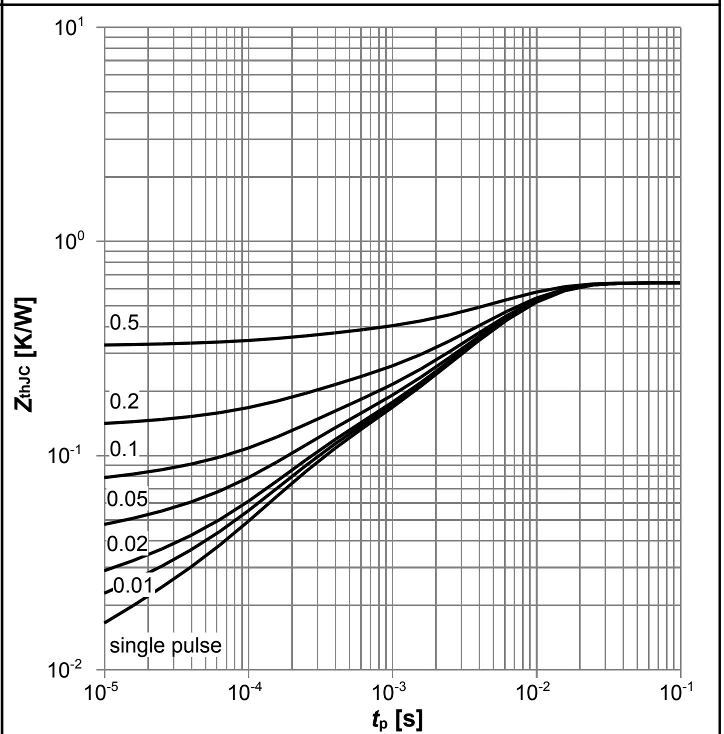
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



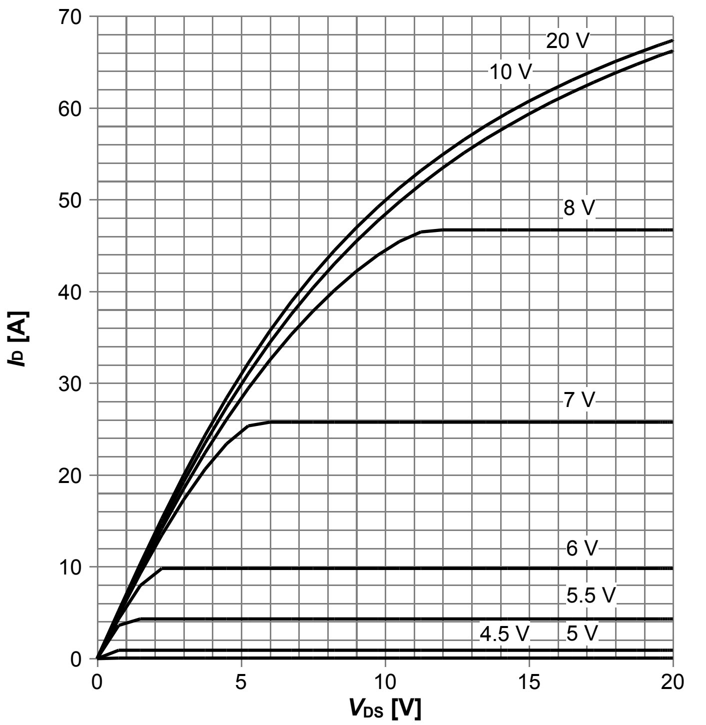
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



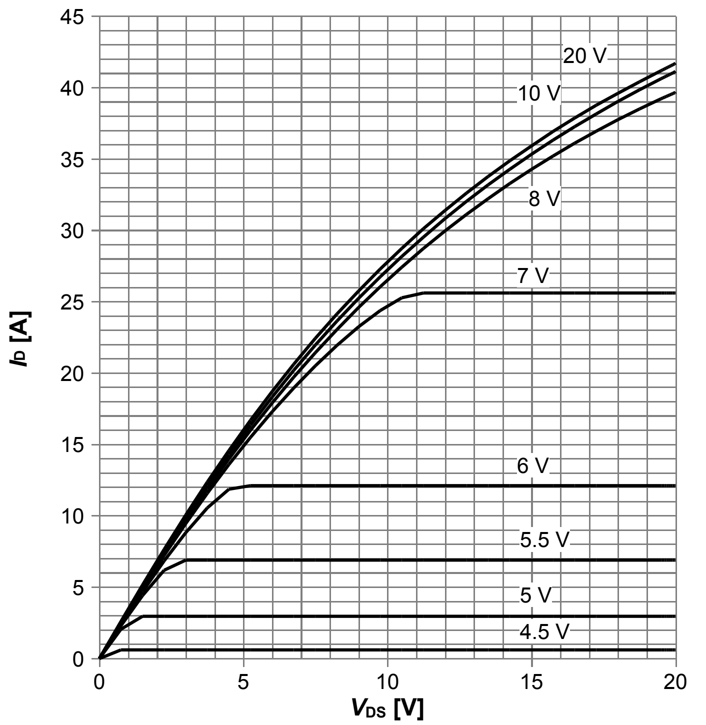
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



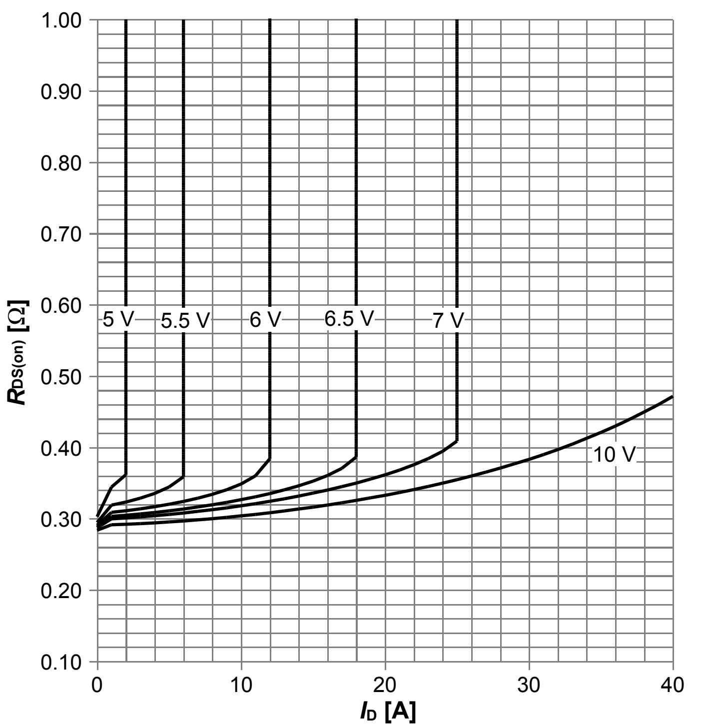
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



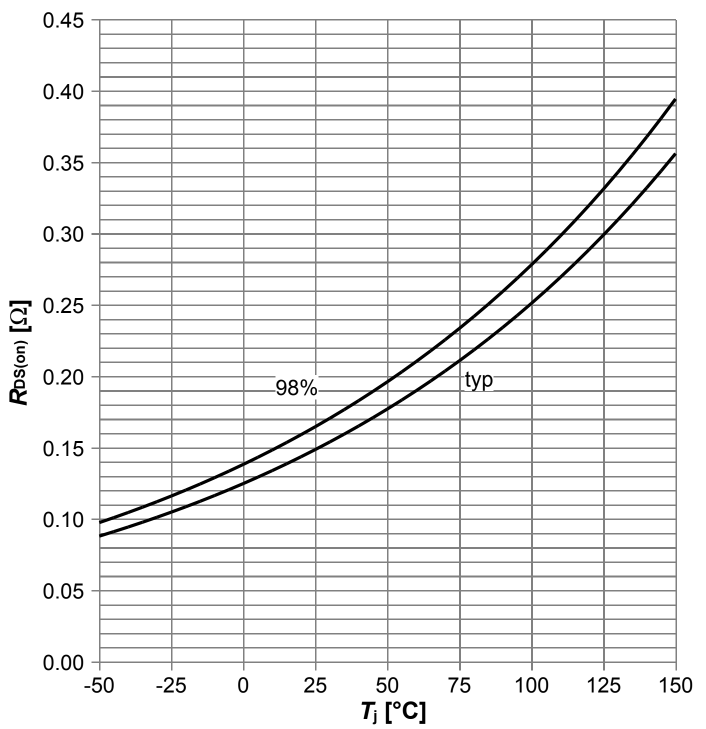
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



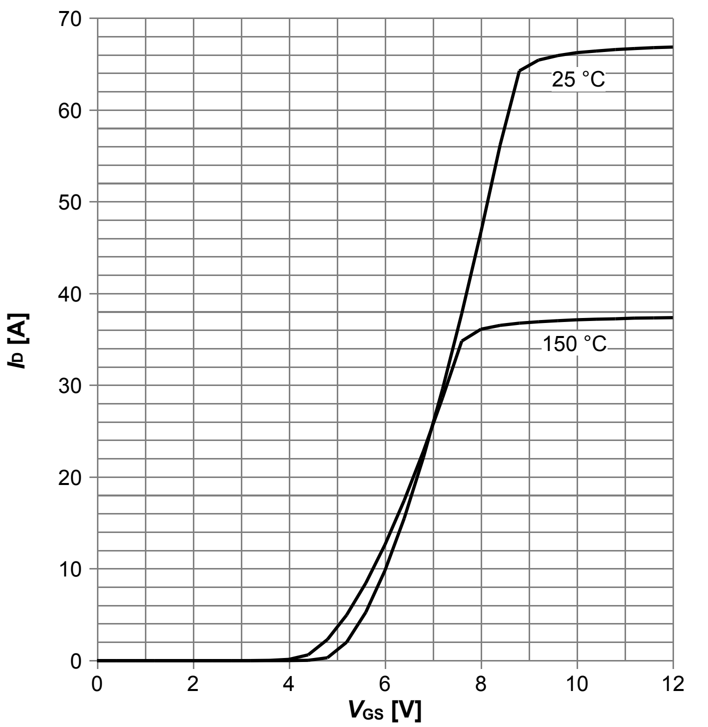
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



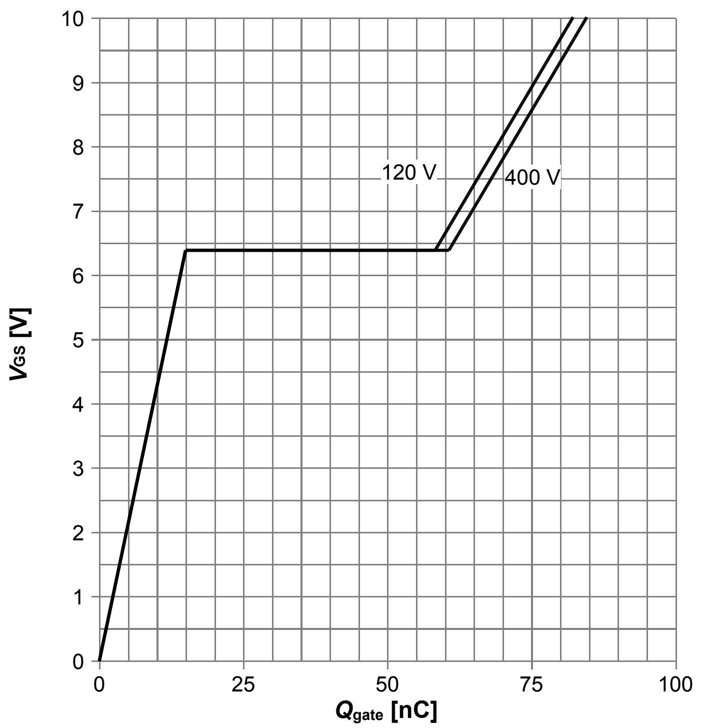
$R_{DS(on)}$=f(T_j); I_D=9.3 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



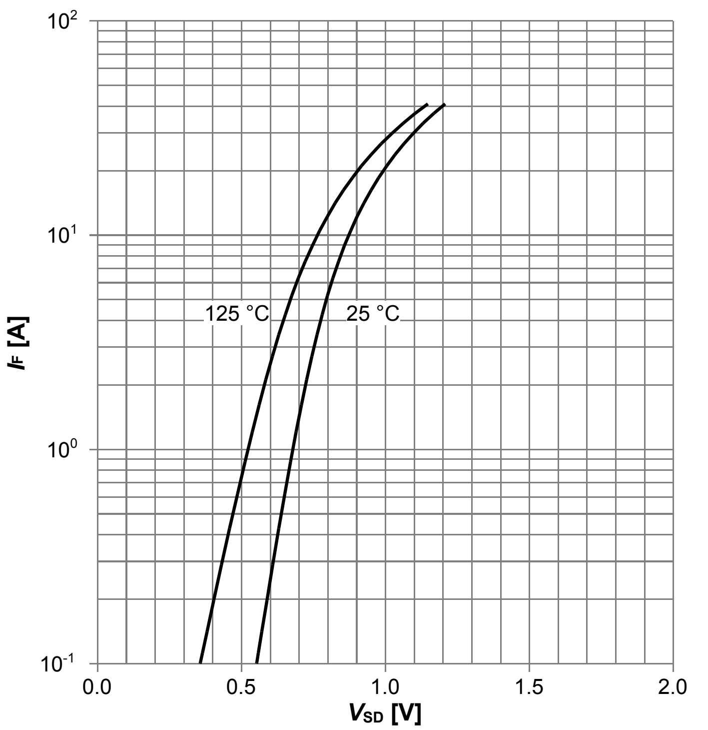
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



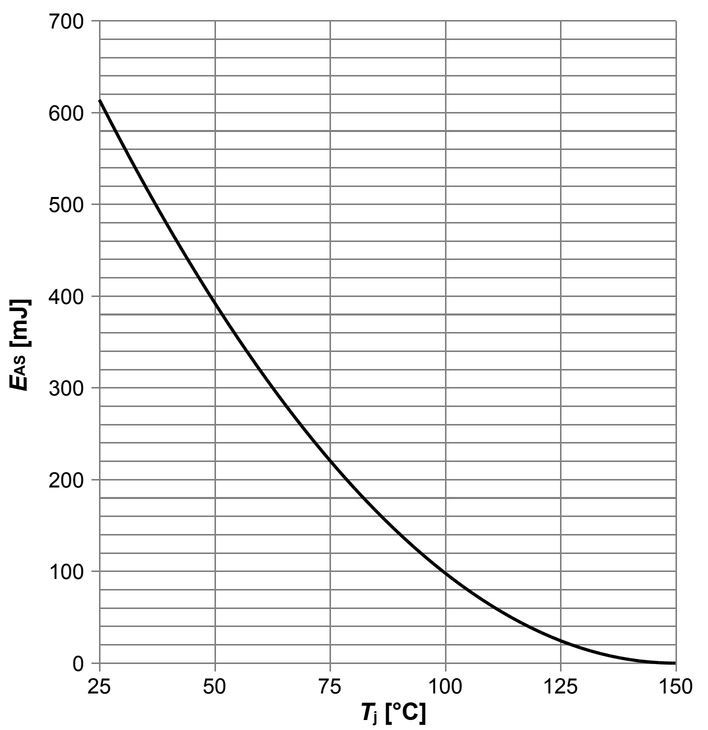
V_{GS}=f(Q_{gate}); I_D=14 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



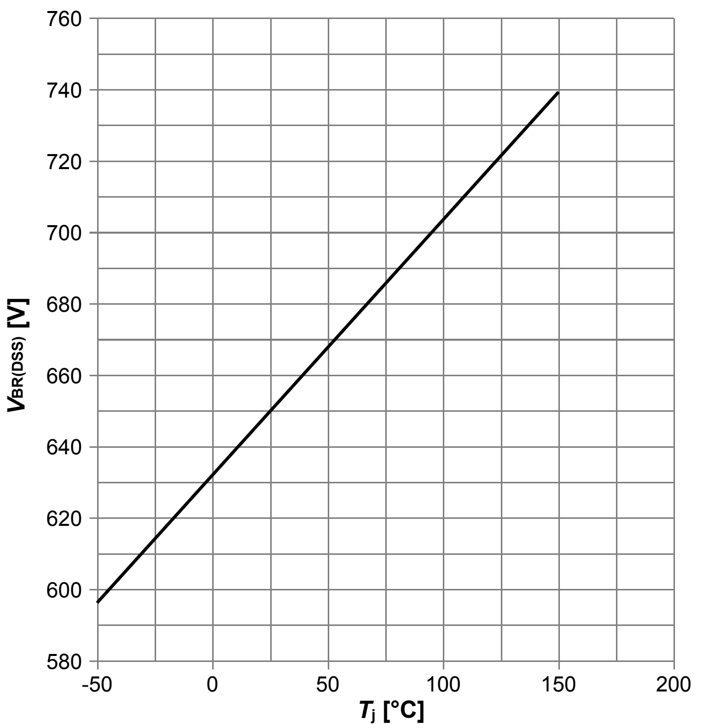
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



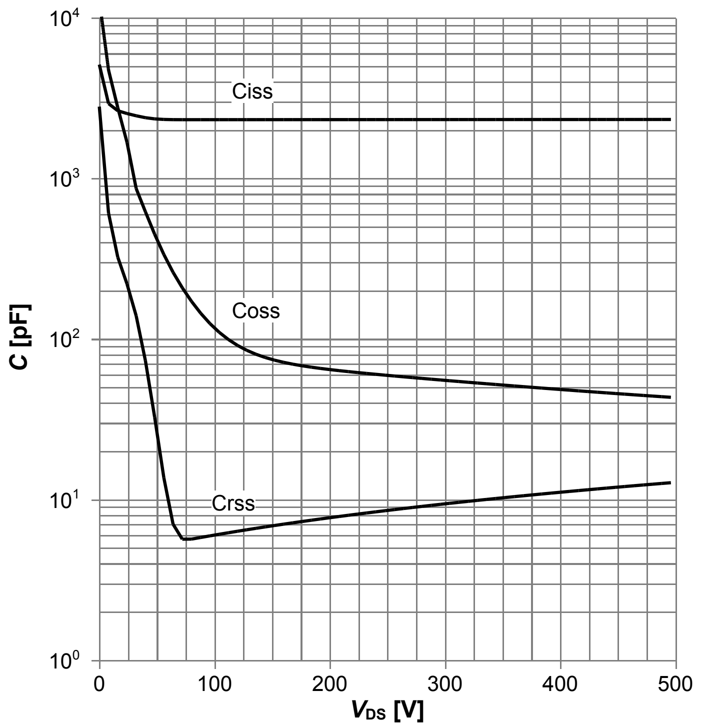
E_{AS}=f(T_j); I_D=4.3 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



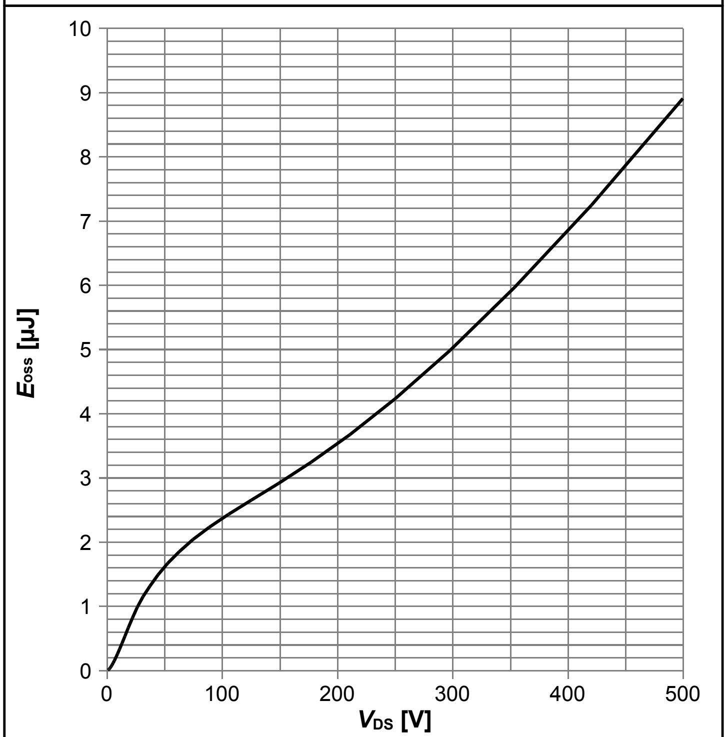
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1MHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

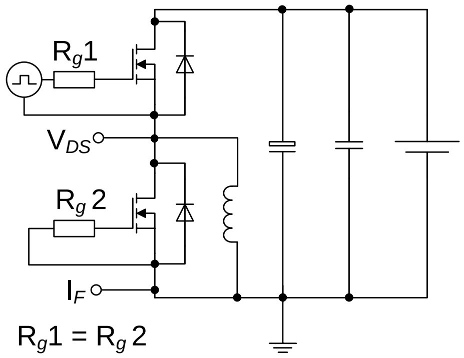
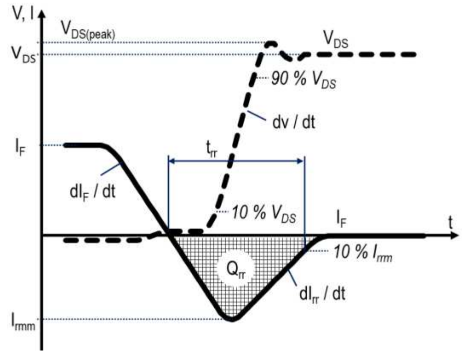
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 switching times (ss)

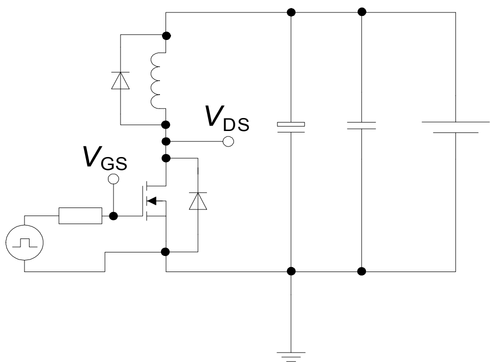
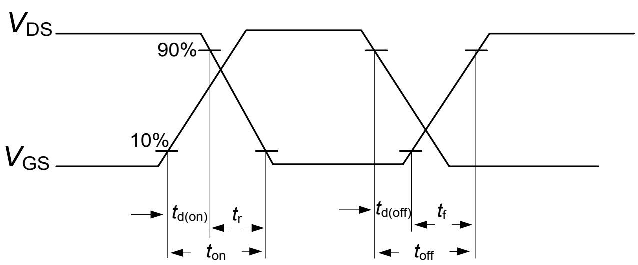
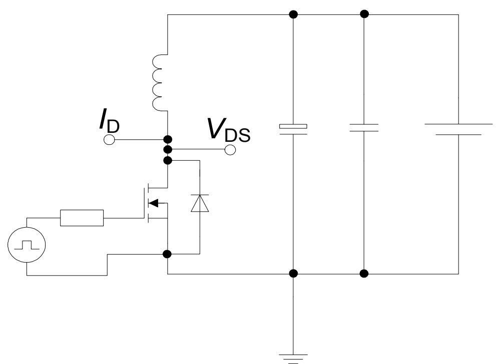
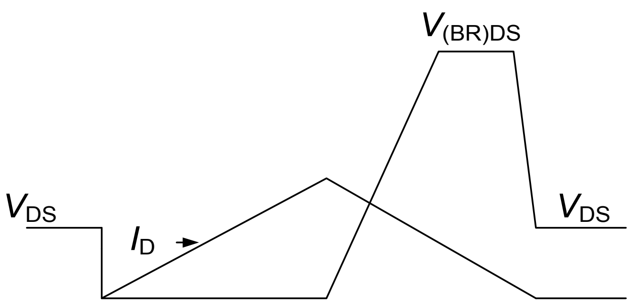
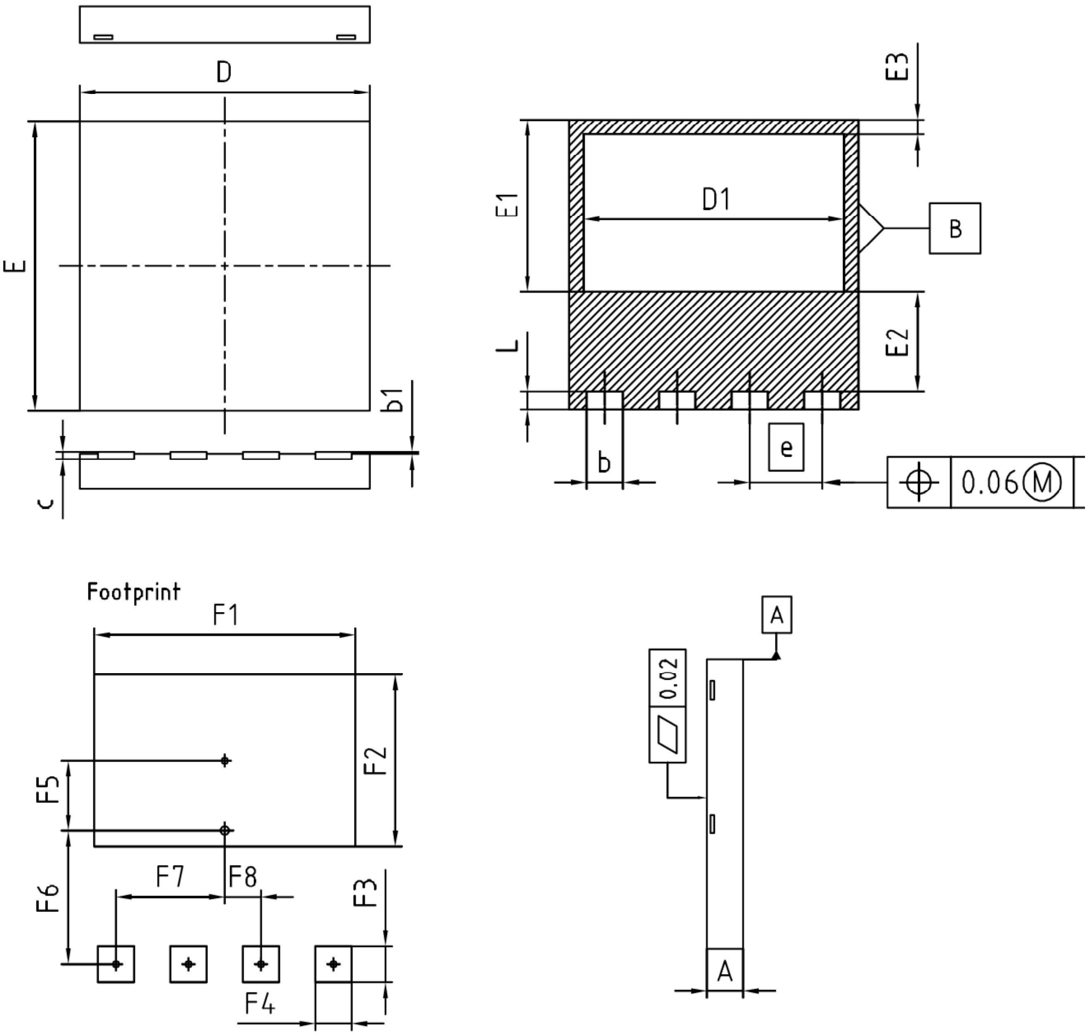
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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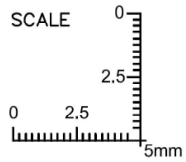
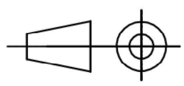


EUROPEAN PROJECTION



ISSUE DATE
05-04-2010

REVISION
01

Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL65R165CFD

Revision: 2017-09-07, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-03-19	Release of final version
2.1	2017-09-07	Updated MSL; style updated

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Published by
Infineon Technologies AG
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