

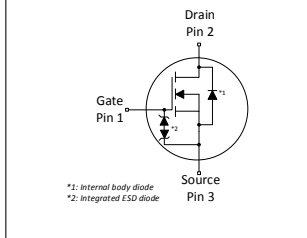
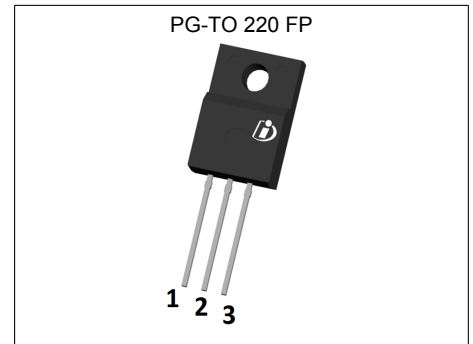
# MOSFET

## 600V CoolMOS™ PFD7 SJ Power Device

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

The latest CoolMOS™ PFD7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, motor drive, lighting, etc.

The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} * Q_g$  and  $R_{DS(on)} * E_{oss}$
- Low switching losses  $E_{oss}$ , excellent thermal behavior
- Fast body diode
- Wide range portfolio of  $R_{DS(on)}$  and package variations
- Integrated zener diode

### Benefits

- Enables high power density designs and small form factors
- Enables efficiency gains at higher switching frequencies
- Excellent commutation ruggedness
- Easy to select right parts and optimize the design
- High ESD ruggedness



### Potential applications

Recommended for ZVS topologies used in high density chargers, adapters, lighting and motor drives applications, etc.

### Product validation

Qualified according to JEDEC Standard

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	360	mΩ
$Q_{g,typ}$	12.7	nC
$I_{D,pulse}$	24	A
$E_{oss} @ 400V$	1.6	μJ
Body diode $di_f/dt$	1300	A/μs
ESD Class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPAN60R360PFD7S	PG-TO 220 FullPAK - Narrow Lead	60S360D7	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	10 6	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	29	mJ	$I_D=2.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.14	mJ	$I_D=2.1\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	2.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	23	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current <sup>1)</sup>	$I_S$	-	-	10	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	24	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 7.2\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>f</sub> /dt	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 7.2\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	2500	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$ ; DPAK / IPAK equivalent

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	5.54	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

**3 Electrical characteristics**  
 at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=0.14mA$
Zero gate voltage drain current <sup>1)</sup>	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=600V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=600V, V_{GS}=0V, T_j=125^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	1000	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.303 0.714	0.360	$\Omega$	$V_{GS}=10V, I_D=2.9A, T_j=25^\circ C$ $V_{GS}=10V, I_D=2.9A, T_j=150^\circ C$
Gate resistance	$R_G$	-	11.0	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	534	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	12	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>2)</sup>	$C_{o(er)}$	-	20	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>3)</sup>	$C_{o(tr)}$	-	187	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	13.5	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=2.9A, R_G=10.2\Omega; \text{see table 9}$
Rise time	$t_r$	-	11	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=2.9A, R_G=10.2\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	46	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=2.9A, R_G=10.2\Omega; \text{see table 9}$
Fall time	$t_f$	-	13	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=2.9A, R_G=10.2\Omega; \text{see table 9}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	3.0	-	nC	$V_{DD}=400V, I_D=2.9A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	4.4	-	nC	$V_{DD}=400V, I_D=2.9A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	12.7	-	nC	$V_{DD}=400V, I_D=2.9A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.6	-	V	$V_{DD}=400V, I_D=2.9A, V_{GS}=0 \text{ to } 10V$

<sup>1)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.0	-	V	$V_{GS}=0V, I_F=2.9A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	60	90	ns	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	0.14	0.28	$\mu C$	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	4.1	-	A	$V_R=400V, I_F=2.9A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

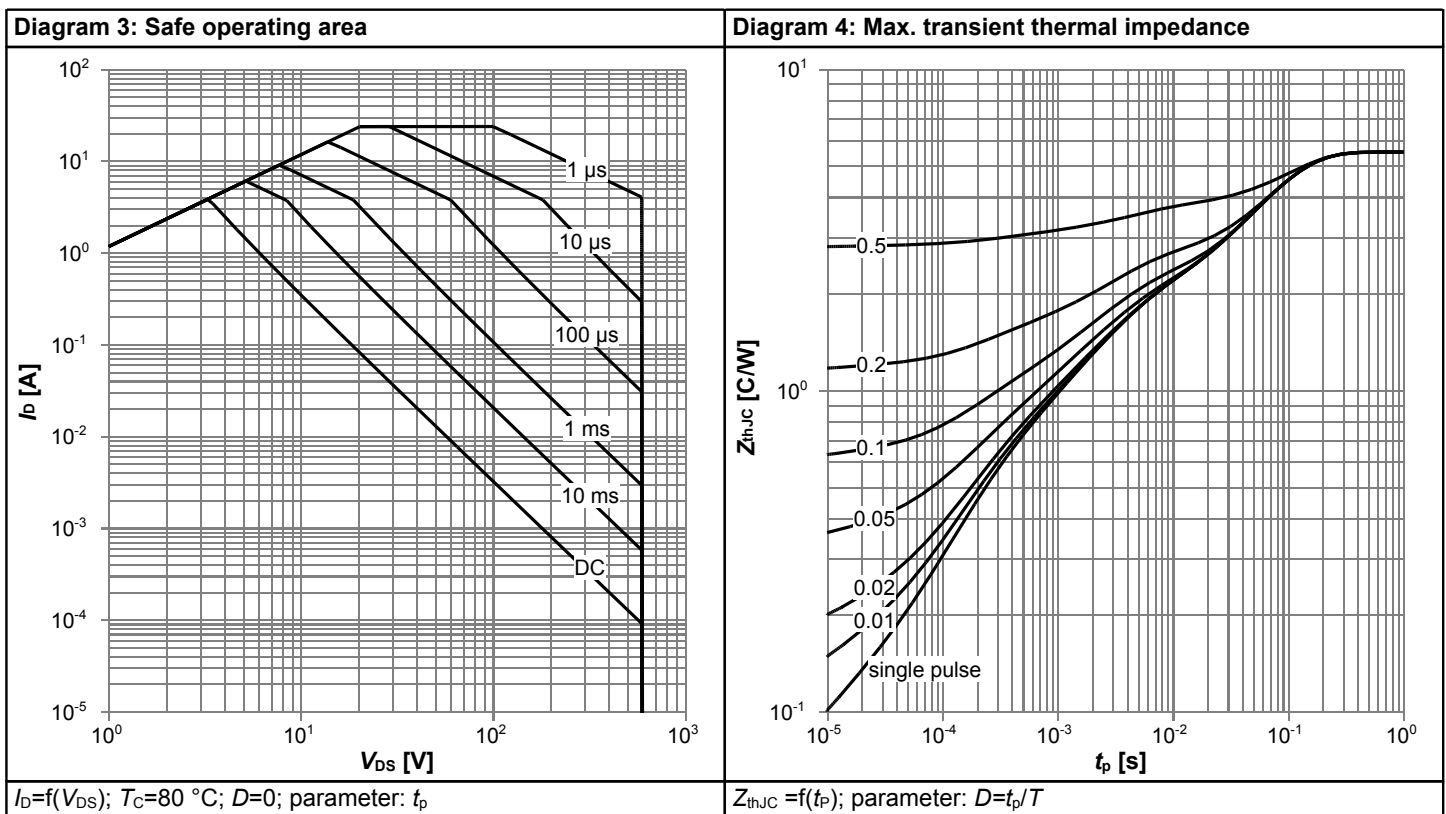
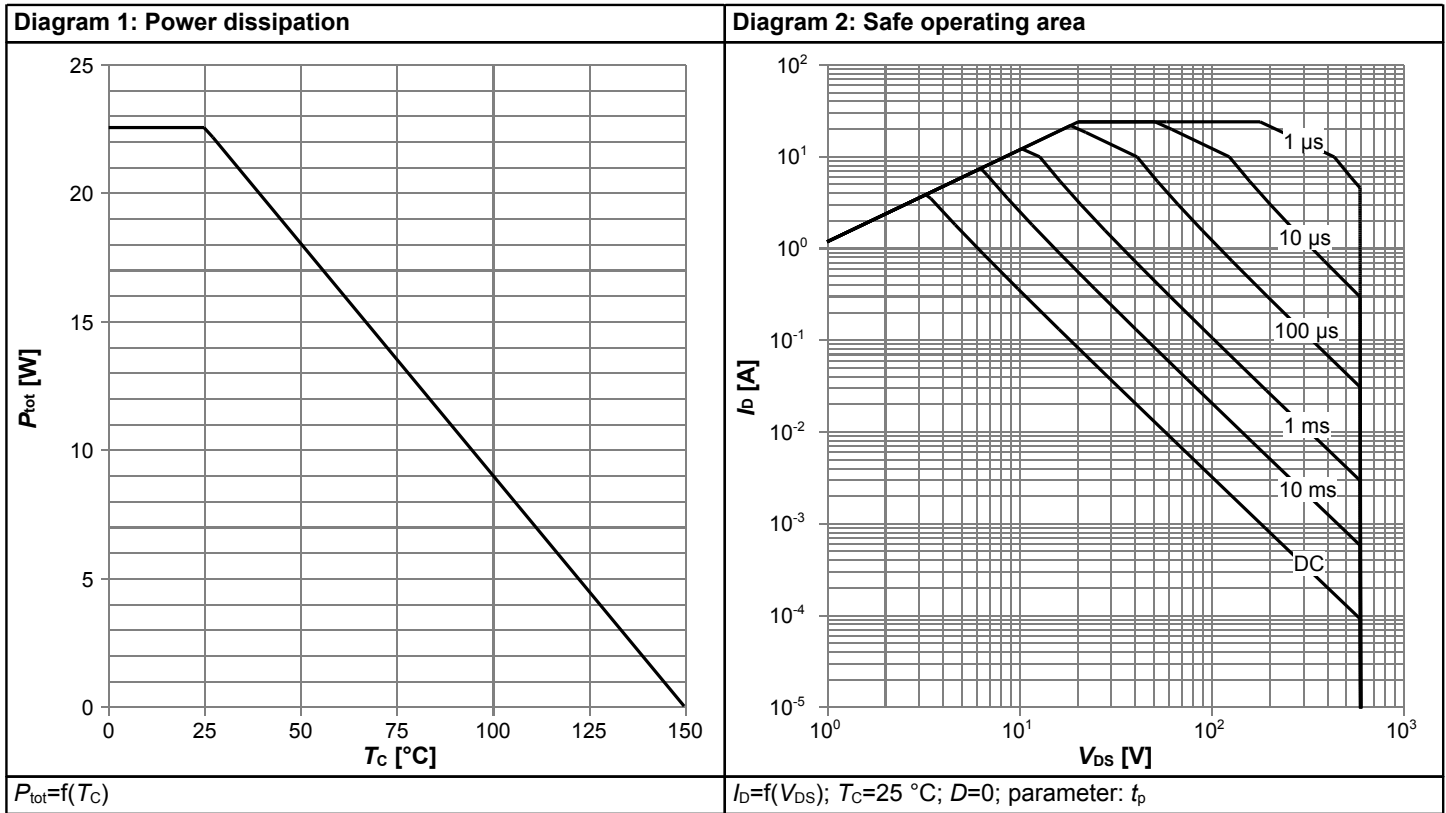
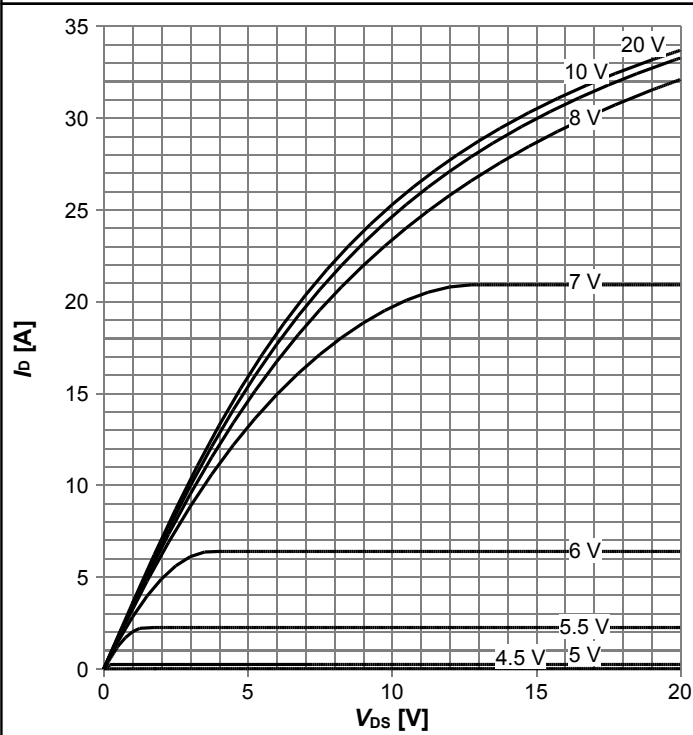
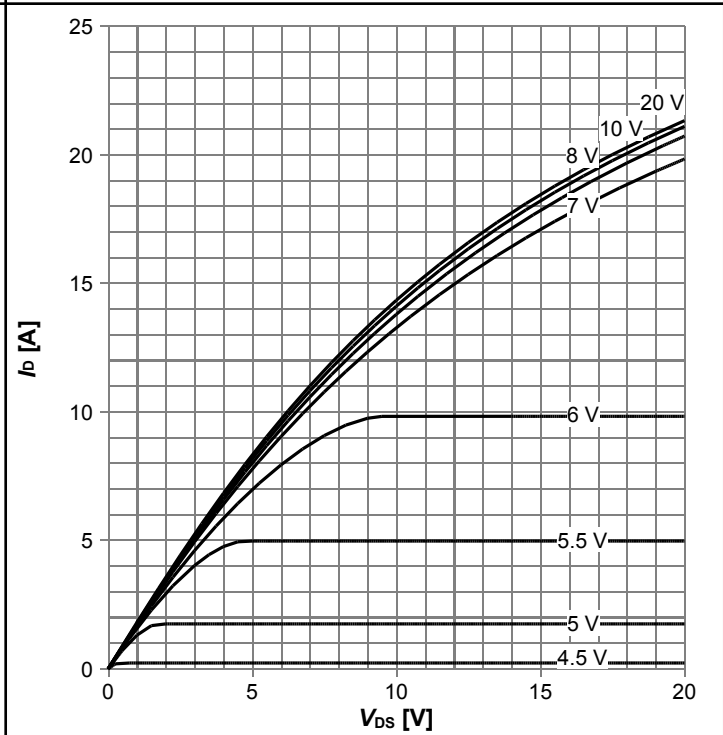


Diagram 5: Typ. output characteristics



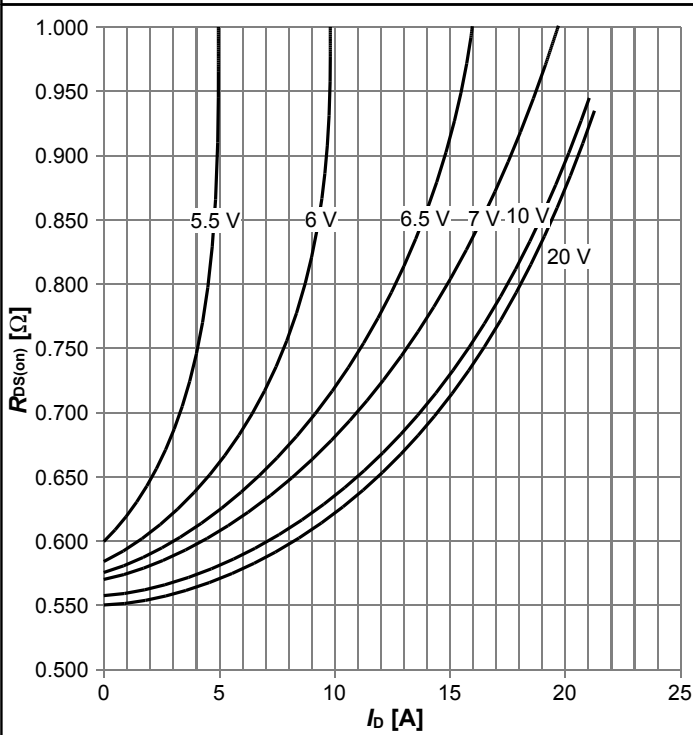
$I_D=f(V_{DS})$ ;  $T_j=25\text{ }^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



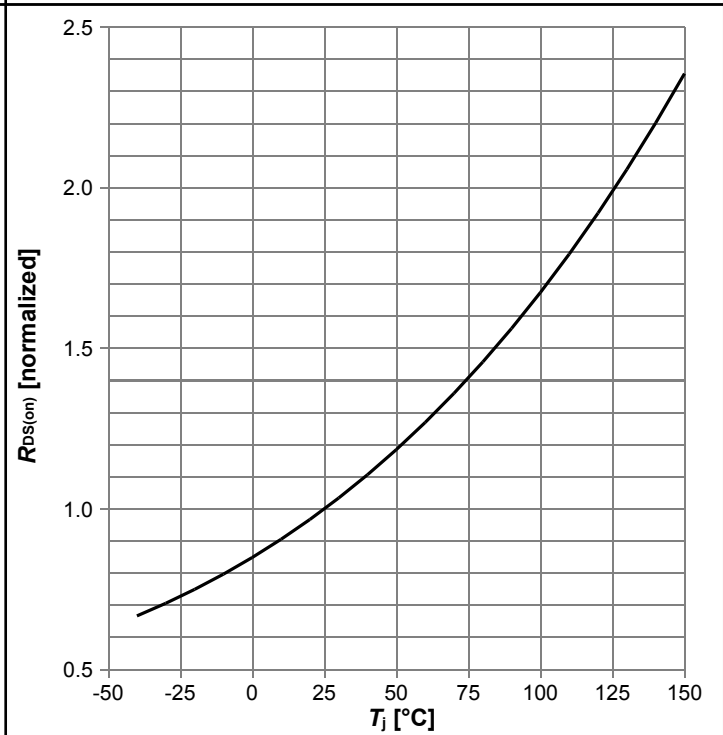
$I_D=f(V_{DS})$ ;  $T_j=125\text{ }^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ }^\circ\text{C}$ ; parameter:  $V_{GS}$

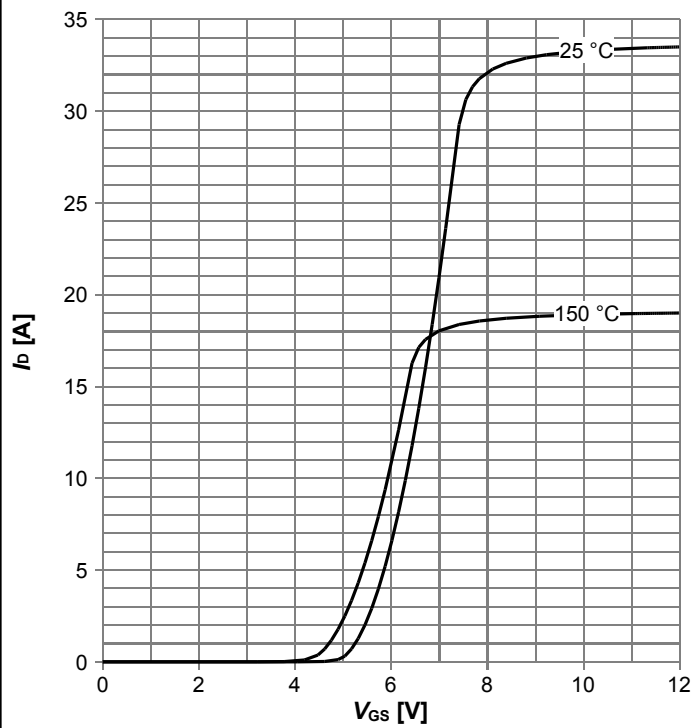
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$ ;  $I_D=2.9\text{ A}$ ;  $V_{GS}=10\text{ V}$

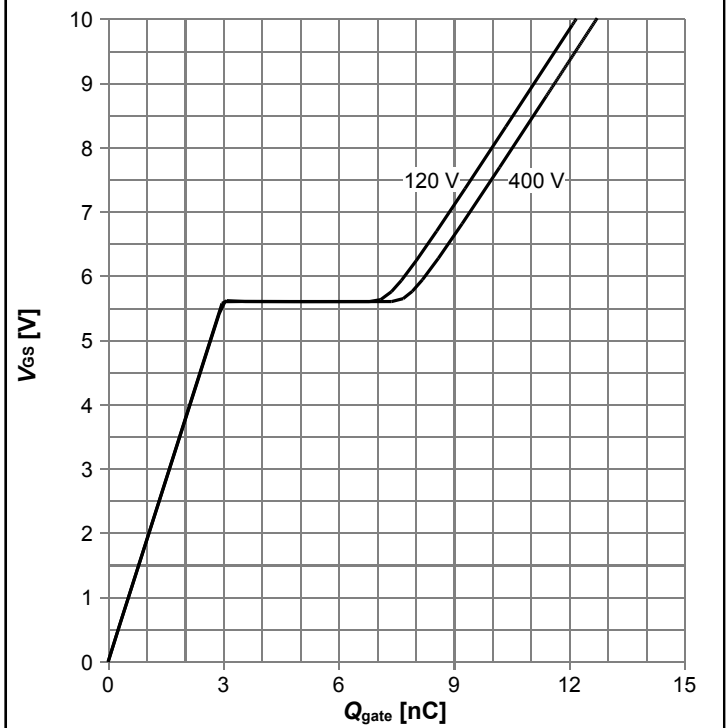


Diagram 9: Typ. transfer characteristics



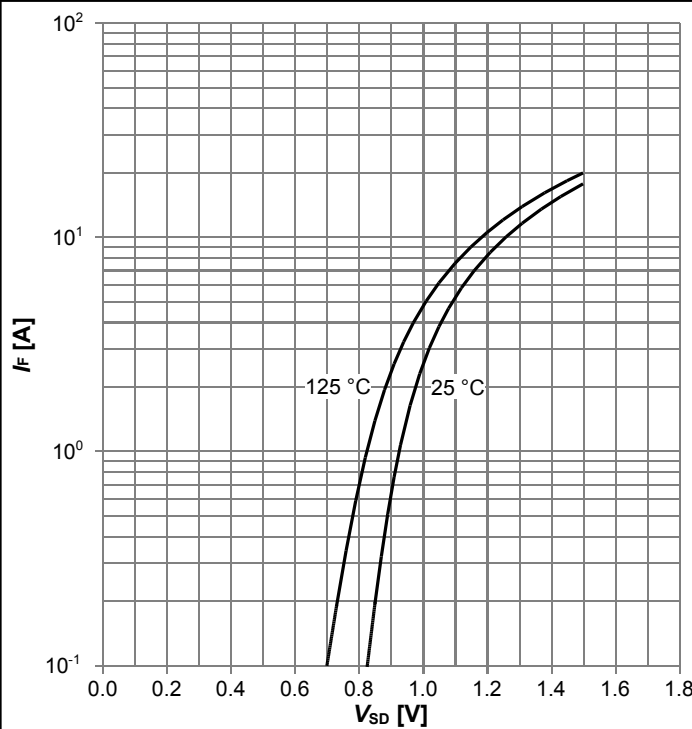
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



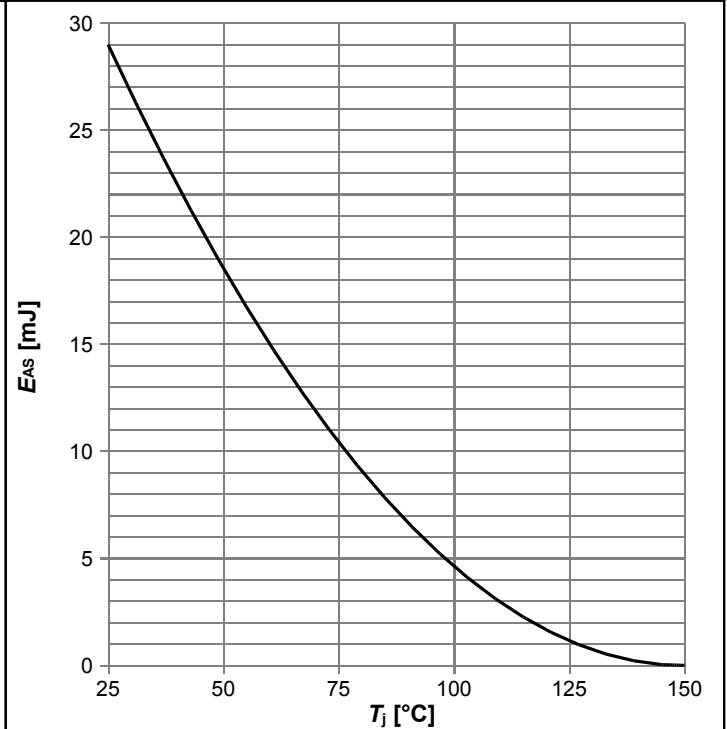
$V_{GS} = f(Q_{gate}); I_D = 2.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



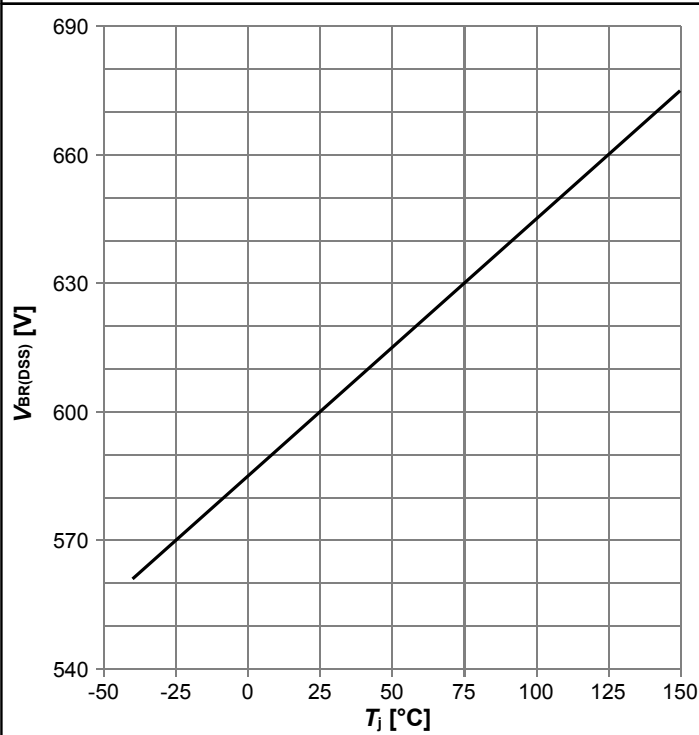
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



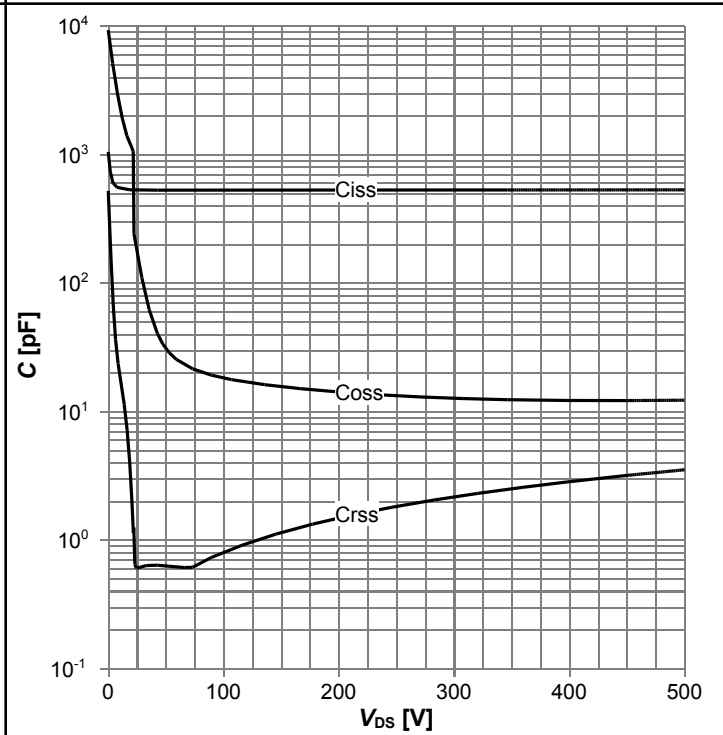
$E_{AS} = f(T_j); I_D = 2.1 \text{ A}; V_{DD} = 50 \text{ V}$

**Diagram 13: Drain-source breakdown voltage**



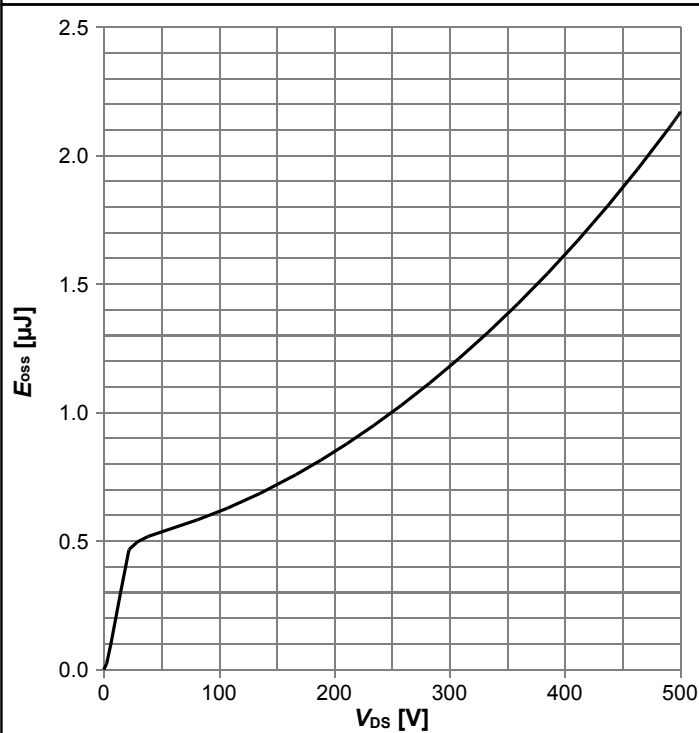
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**



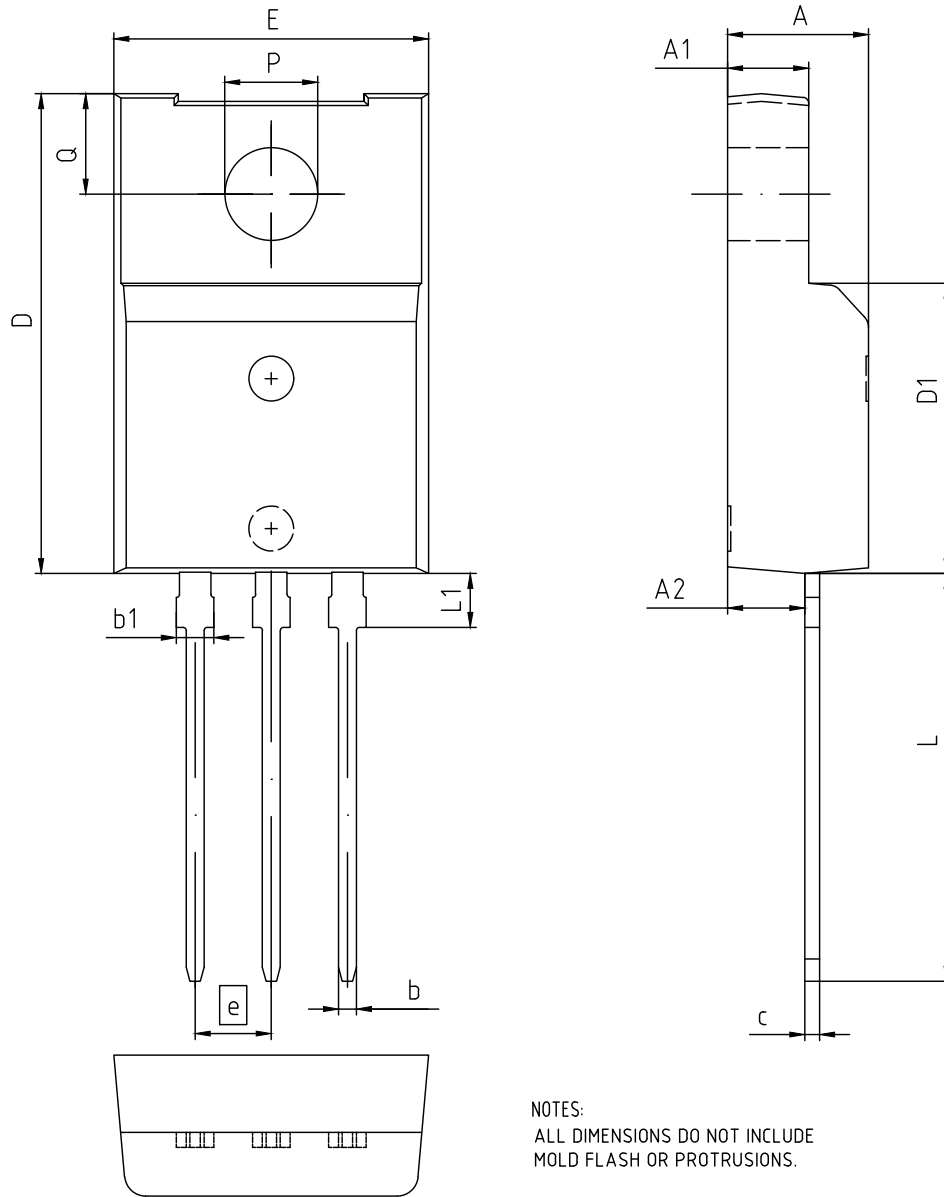
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.60	4.80
A1	2.60	2.80
A2	2.47	2.67
b	0.56	0.69
b1	1.01	1.15
c	0.46	0.59
D	15.90	16.10
D1	9.58	9.78
E	10.40	10.60
e	2.54	
N	3	
L	13.45	13.75
L1	1.70	1.91
øP	3.00	3.20
Q	3.25	3.45

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Figure 1 Outline PG-TO 220 FullPAK - Narrow Lead, dimensions in mm

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS PFD7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS PFD7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS PFD7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPAN60R360PFD7S

**Revision: 2019-11-29, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-09-27	Release of final version
2.1	2019-11-29	Modified current Id and Is ratings

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